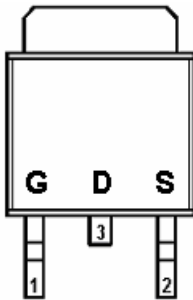


DESCRIPTION

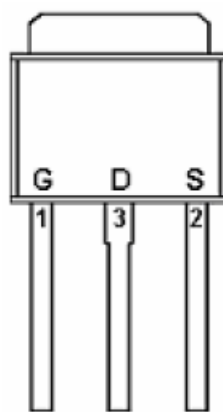
STN8882D is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The STN8882D has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

PIN CONFIGURATION (D-PAK)

TO-252



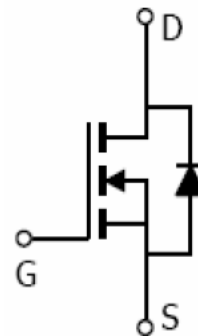
TO-251



FEATURE

- 30V/ 35A, $R_{DS(ON)} = 5m\Omega$
- @ $V_{GS} = 10V$
- 30V/35A, $R_{DS(ON)} = 7m\Omega$
- @ $V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252, TO-251 package design

PART MARKING



Y: Year Code A: Process Code



60.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	30	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	60	A
		40	
Pulsed Drain Current	IDM	100	A
Continuous Source Current (Diode Conduction)	IS	50	A
Power Dissipation	PD	40	W
		55	
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	100	°C/W



STN8882D



N Channel Enhancement Mode MOSFET

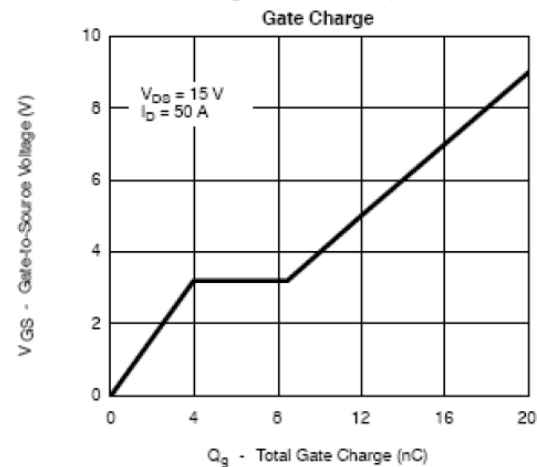
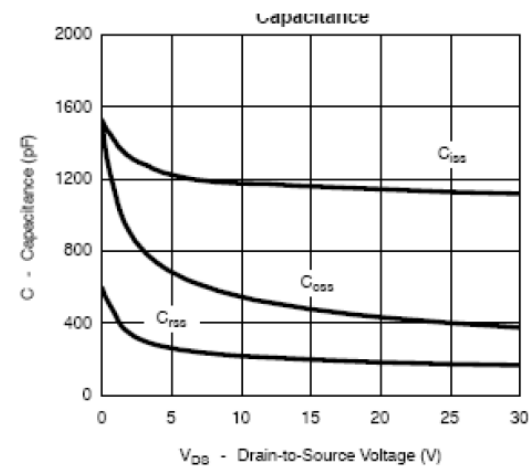
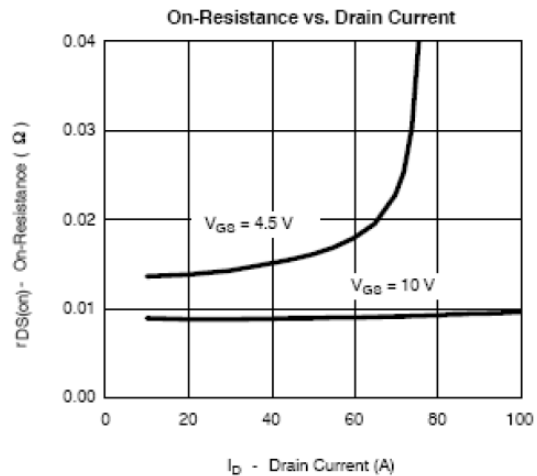
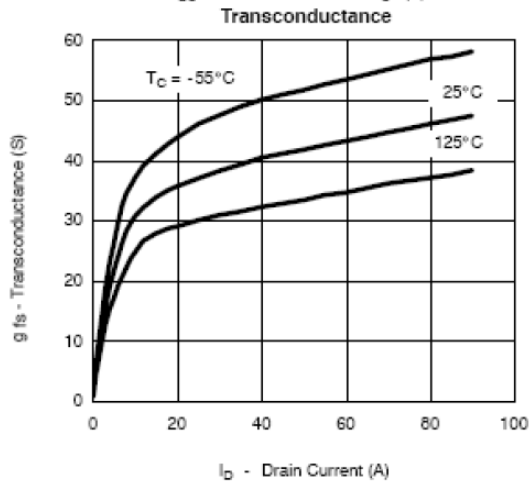
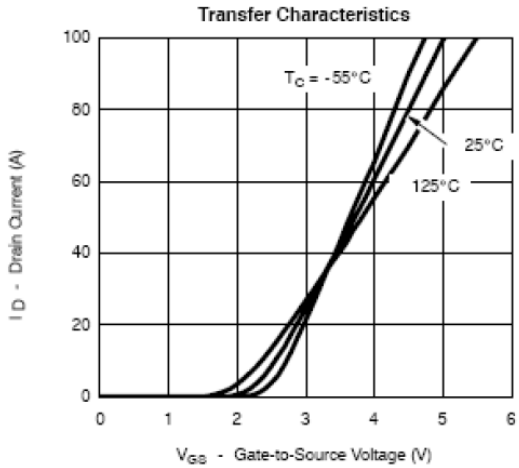
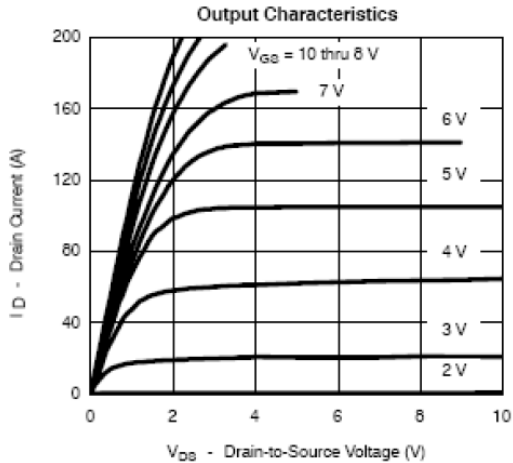
60.0A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

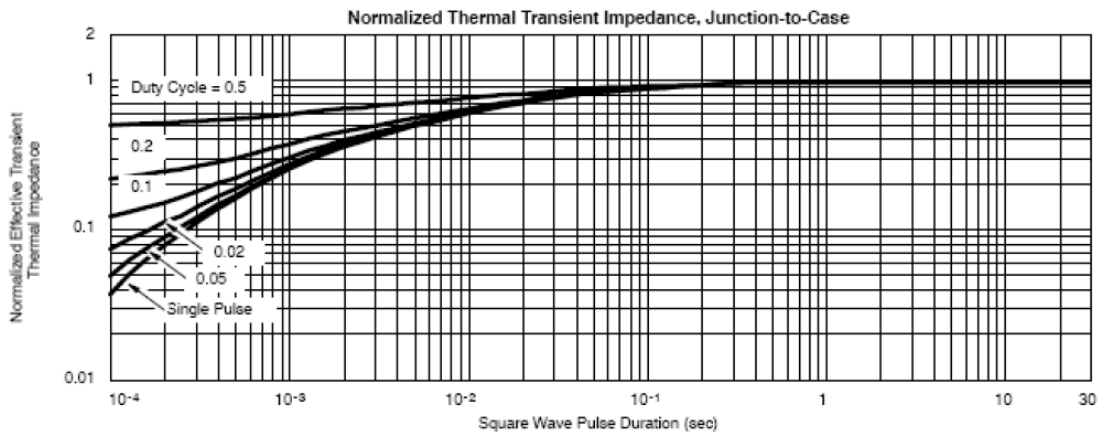
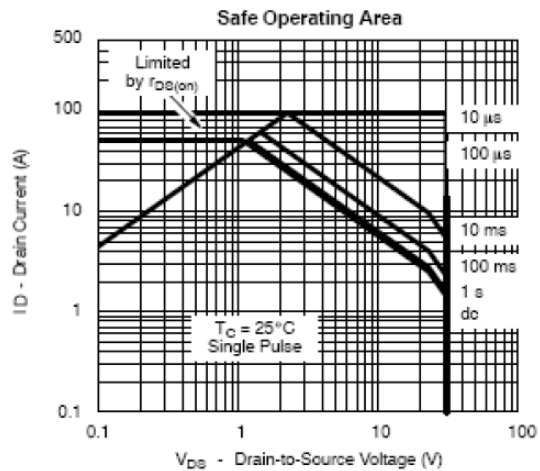
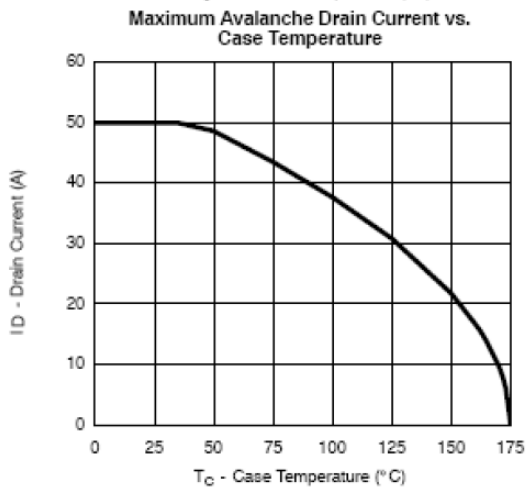
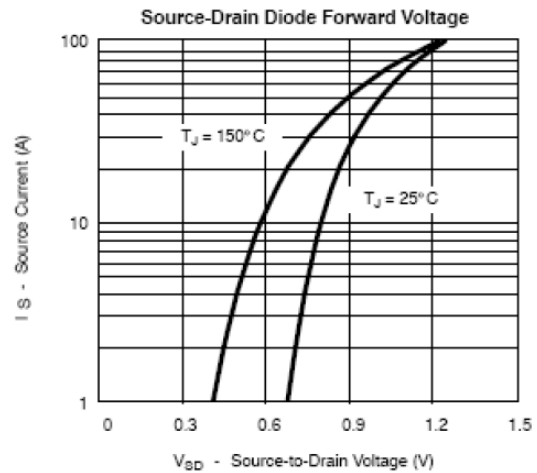
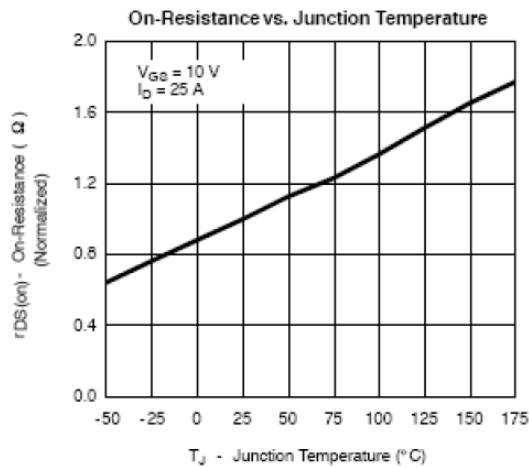
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250mA$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$			1	uA
		$V_{DS}=30V, V_{GS}=0V$ $T_J=120^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	100			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=35A$ $V_{GS}=4.5V, I_D=35A$			5 7	mΩ
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=12A$		110		S
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$			1.5	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V$ $I_D=20A$		41.3	54	nC
Gate-Source Charge	Q_{gs}			18	23	
Gate-Drain Charge	Q_{gd}			13	17	
Input Capacitance	C_{iss}	$V_{DS} = 15V, V_{GS}=0V$ $F=1MHz$		4826		pF
Output Capacitance	C_{oss}			683.3		
Reverse Transfer Capacitance	C_{rss}			374.9		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=15V, R_L= 15\Omega$ $I_D=1.0A, V_{GEN}=10V$ $R_G=6\Omega$		23.6	47	nS
				12	24	
Turn-Off Time	$t_{d(off)}$ t_f			114	227	
				97.2	195	

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

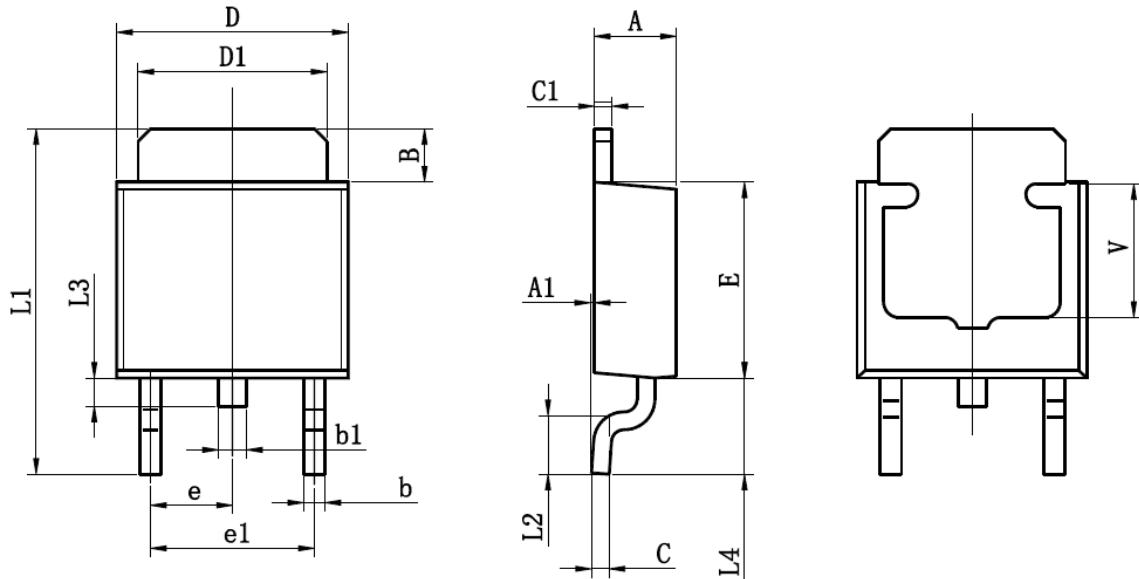
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

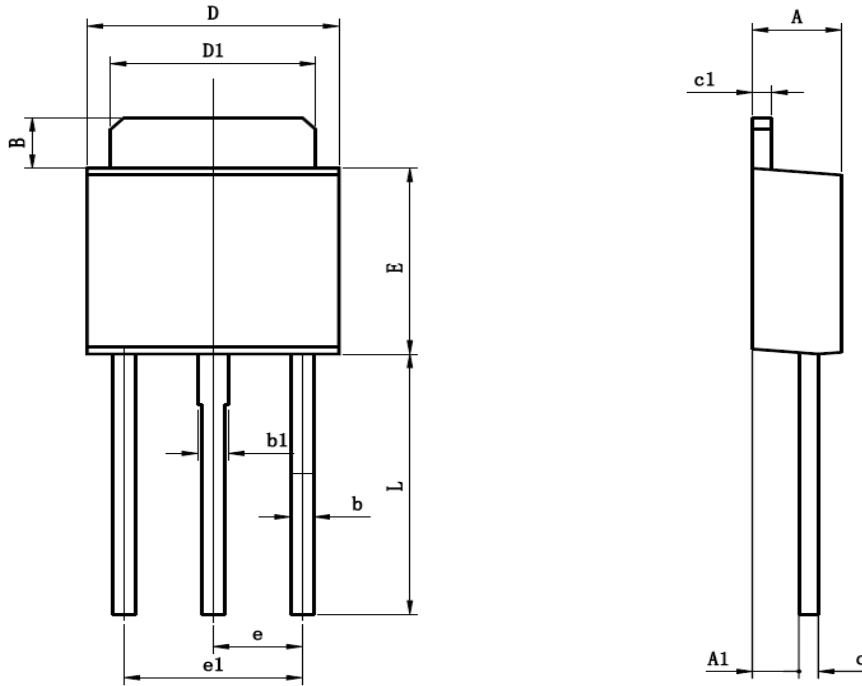


TO-252-2L PACKAGE OUTLINE SOP-8P



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	

TO-251 PACKAGE OUTLINE SOP-8P



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	1.020	1.270	0.040	0.050
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311