

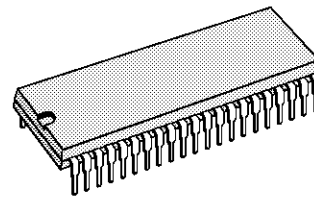
PAL-SECAM LUMA-CHROMA & DEFLECTION PROCESSOR

PRELIMINARY DATA

- RGB AND FAST BLANKING INPUTS
- AUTOMATIC CUT-OFF CONTROL
- DC-CONTROLLED BRIGHTNESS, CONTRAST AND SATURATION
- CERAMIC 500kHz VCO FOR LINE DEFLECTION
- CHROMA STANDARD AUTOMATIC IDENTIFICATION
- BIDIRECTIONAL I/O FOR CHROMA STANDARD
- PHASE-LOCKED REFERENCE OSCILLATOR USING A STANDARD 4.43MHz
- OSD CAPABILITY ON OUTPUTS
- VIDEO IDENTIFICATION GENERATOR

Used with the TDA8222, this IC permits a complete low cost solution with external output stages.

It is pin compatible with STV2102 PAL only processor.



SHRINK 42
(Plastic Package)

ORDER CODE : STV2110A

DESCRIPTION

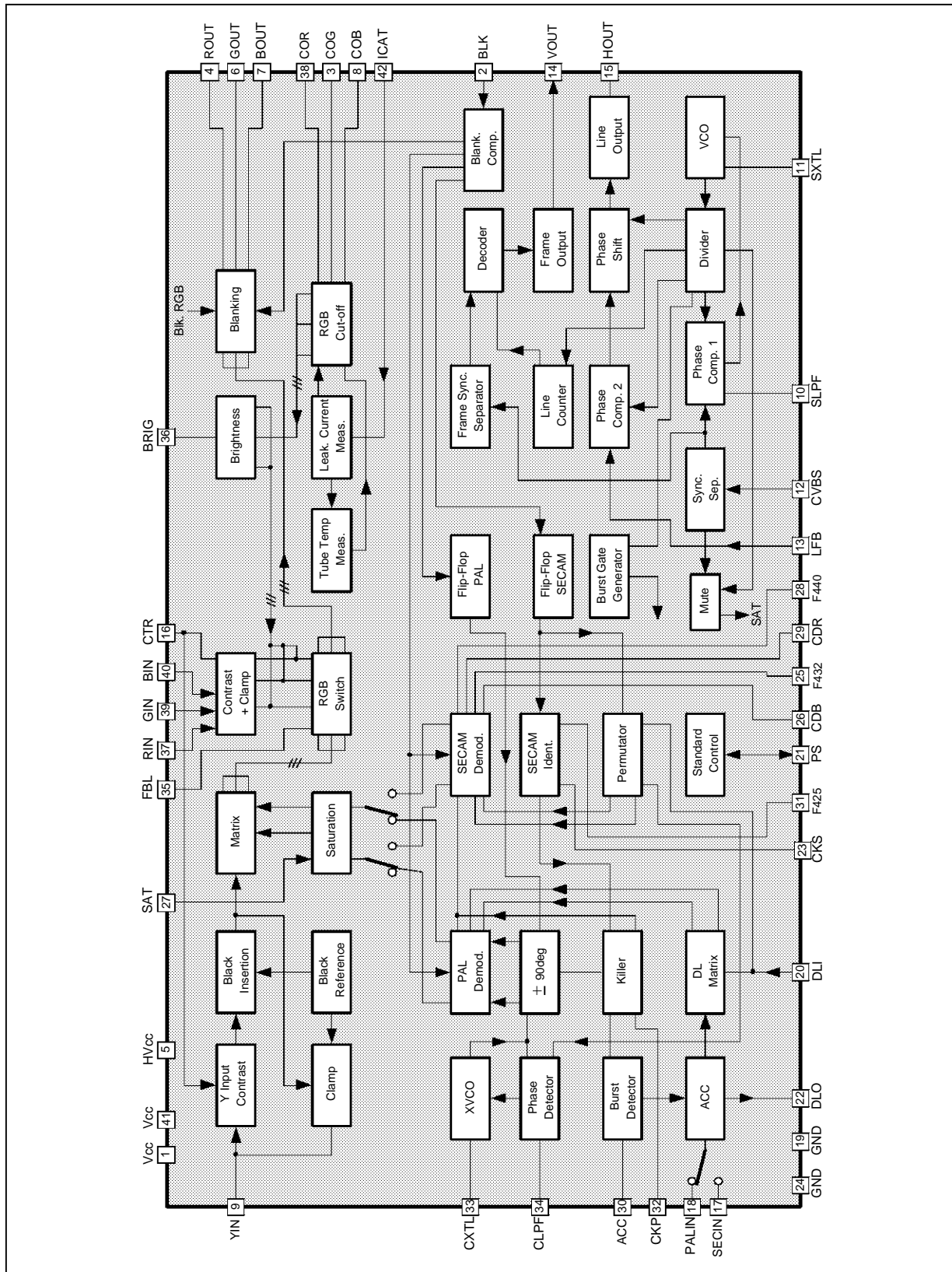
The STV2110A is a PAL-SECAM chroma decoder, video and H/V deflection processor for CTV.

PIN CONNECTIONS

| | | | | | |
|-------------------------|-------|----|----|------|---------------------------|
| SUPPLY VOLTAGE | Vcc | 1 | 42 | ICAT | CATHODE CURRENT |
| BLANKING INPUT | BLK | 2 | 41 | Vcc | SUPPLY VOLTAGE INPUT |
| GREEN CUT-OFF CAPACITOR | COG | 3 | 40 | BIN | BLUE INPUT |
| RED OUTPUT | ROUT | 4 | 39 | GIN | GREEN INPUT |
| HORIZONTAL Vcc | HVcc | 5 | 38 | COR | RED CUT-OFF CAPACITOR |
| GREEN OUTPUT | GOUT | 6 | 37 | RIN | RED INPUT |
| BLUE OUTPUT | BOUT | 7 | 36 | BRIG | BRIGHTNESS CONTROL |
| BLUE CUT-OFF CAPACITOR | COB | 8 | 35 | FBL | FAST BLANKING INPUT |
| LUMINANCE SIGNAL INPUT | YIN | 9 | 34 | CLPF | CHROMA LOOP FILTER |
| SCANNING LOOP FILTER | SLPF | 10 | 33 | CXTL | CHROMA XTAL |
| SCANNING XTAL | SXTL | 11 | 32 | CKP | PAL KILLER CAPACITOR |
| COMPOSITE VIDEO SIGNAL | CVBS | 12 | 31 | F425 | 4.25MHz FILTER |
| LINE FLYBACK INPUT | LFB | 13 | 30 | ACC | ACC CONTROL CAPACITOR |
| VERTICAL OUTPUT | VOUT | 14 | 29 | CDR | RED DEEMPHASIS CAPACITOR |
| HORIZONTAL OUTPUT | HOUT | 15 | 28 | F440 | 4.40MHz FILTER |
| CONTRAST CONTROL | CTR | 16 | 27 | SAT | SATURATION CONTROL |
| SECAM CHROMA INPUT | SECIN | 17 | 26 | CDB | BLUE DEEMPHASIS CAPACITOR |
| PAL CHROMA INPUT | PALIN | 18 | 25 | F432 | 4.32MHz FILTER |
| GROUND | GND | 19 | 24 | GND | GROUND |
| DELAY CHROMA INPUT | DLI | 20 | 23 | CKS | SECAM KILLER CAPACITOR |
| CHROMA STANDARD I/O | PS | 21 | 22 | DLO | CHROMA OUTPUT |

2110A-01.EPS

BLOCK DIAGRAM



2110A-02.EPS

FUNCTIONAL DESCRIPTION

DEFLECTION

Synchronization Separator

The synchronization separator is based on the bottom of synchronization pulses alignment to an internal reference voltage. An external capacitor permits to align synchro. pulses, two external resistors determines the detection threshold of synchro pulses. The frame synchronization pulses are locked to a 32 μ s reference signal to perfect interlacing.

Horizontal Scanning

The horizontal scanning frequency is obtained from a 500kHz VCO. The circuit uses two phase-locked loops (PLL). The first one controls the frequency; the second one, fully integrated, controls the relative phase of the synchronization and the line fly-back signals.

The first PLL has two time constants: a long time constant during the picture to have a good noise immunity, a short time constant at the beginning of the frame to recapture faster the phase in case of VCR video signal. Moreover, the PLL is in short time constant three lines before frame pulses occurred, it permits to ensure good interlacing when the video signal comes from a VCR tape with high phase error.

The horizontal output signal is 28 μ s width. On starting up, horizontal pulses are enabled at $V_{CC} = 6.8V$. On shutting down, horizontal pulses are inhibited for $V_{CC} = 6.2V$.

Vertical Scanning

The windows for the frame sync detection are generated by a count down system. The selection of the windows is determined by the IC status:

- video identification off - window : 248/314
- video identification on - window : 248/352

When a sync pulse is detected inside the window a 10.5 lines long pulse is provided to V_{OUT} pin.

The count down system provides also the needed signals for the time constant switch, the line PLL inhibition and service signals to the rest of the IC.

CHROMA

ACC Amplifier, DL Matrix, Permutator and Demodulator

The correct chroma subcarrier input, issued from bandpass or bell filter, is internally selected with the standard. The ACC amplifier involves three stages: the first one selects the correct input, the second one the -6dB in picture (PAL mode), the

third one is controlled by the ACC voltage.

The dynamic range is over than 30dB.

The chrominance output signal is fed to the delay line.

- PAL mode :
 - the adding and subtracting direct and delayed signals are performed by the DL matrix function.
 - Two synchronous demodulators multiply the (B-Y) signal with the 0 degree phase 4.43MHz reference signal and the (R-Y) signal with the alternate ± 90 deg. 4.43MHz phase reference signal.
- SECAM mode :
 - the permutator separates the two (B-Y) and (R-Y) subcarriers. These signals are demodulated by two FM demodulators with two external L, C centered on $f_{O(\text{blue})} = 4.25\text{MHz}$ and $f_{O(\text{red})} = 4.406\text{MHz}$.

4.43MHz Phase Locked Loop

The oscillating frequency of the 4.43MHz crystal oscillator is controlled by the output voltage of the loop filter. The phase detector will lock the 90 degree reference signal to the direct burst signal. A 90 degree phase shifter permits to recover the 0 degree reference signal. A flip-flop driven by line pulses permits to generate the alternate ± 90 degree signal.

ACC Control and Color Killer

PAL mode :

the direct burst signal is demodulated with the ± 90 degree reference signal. The demodulation result is used by ACC control and killer function.

SECAM mode :

ACC control is done by a X^2 demodulator. For identification the burst signals of the red and blue lines are demodulated by the external LC connected on Pin 31, it is centered at 4.32MHz. This gives positive and negative signals which are inverted by the signal coming out of the SECAM flip-flop.

In both standards, if the demodulation result is always positive, the killer capacitor is charged and the standard is identified (color ON). When demodulation result is always negative, the killer capacitor voltage reaches the flip-flop inhibition level, so the alternate sequence is reversed and the capacitor is charged again.

In case of no video signal, both killer capacitor voltages are maintained about $V_{CC}/2$, below the color off threshold.

In PAL or SECAM, the ACC control voltage is obtained by the peak detection of the demodulated burst.

Automatic Standard Identification

The circuit is alternately forced in each mode during two fields (PAL mode, SECAM mode disabled or SECAM mode, PAL mode disabled).

If PAL signal is identified, the alternate PAL/SECAM sequency is locked in PAL mode.

To have a SECAM identification, the circuit must memorizes a first SECAM identification, than test the PAL mode and confirm a second SECAM identification. The SECAM identification will take from four to six fields.

Output Pin 21, named PS, is high level in PAL mode and low level in SECAM mode.

Forced standard : Pin 21 can be used for the purpose :

- Pin 21 to HVCC : PAL mode
- Pin 21 to ground : SECAM mode

VIDEO

Input Stage

The luminance input is controlled by the contrast control stage which range is 20dB.

The luminance and color difference signals are added in the video matrix circuit to obtain the color signals.

The color signals are sent to an RGB switch which will drive to the outputs either internal RGB signals or external RGB signals.

Automatic Cut-off Control

The black levels of the RGB outputs are controlled with the cut-off loops during three line periods after the frame retrace. The cut-off measurements are sequentially achieved during these three lines. The leakage current measurement is achieved during the frame retrace and memorized on an internal capacitor, thus the circuit is able to extract the cut-off current from the total current measurement.

Warm-up Detector

At the start-up, the cut-off loops are switch off, a white level is inserted on the luminance signal until a cathode current is detected. Then the cut-off loops are released.

RGB Inputs

To avoid the black level of the inserted signal differing from the black level of the normal video signal, the external RGB are clamped to the black level of the luminance signal. Therefore, an AC coupling is required for the RGB inputs.

The RGB inputs are controlled by a 12dB range contrast control stage.

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|------|
| HV _{CC} | Horizontal Supply Voltage (Pin 5) | 12 | V |
| V _{CC} | Video & Chroma Supply Voltage (Pins 1-41) | HV _{CC} + 0.5 | V |
| H _{OUT} | Horizontal Output (Pin 15) | 12 | V |
| T _{stg} | Storage Temperature | -55, +150 | °C |
| T _{oper} | Operating Temperature | 0, +70 | °C |

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THERMAL DATA

| Symbol | Parameter | Value | Unit |
|----------------------|-------------------------------------|---------|------|
| R _{th(j-a)} | Junction-ambient Thermal Resistance | Max. 60 | °C/W |

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DC AND AC ELECTRICAL CHARACTERISTICS

(HV_{CC} = V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|------------------------|---|-----------------|------|------|------|------|
| HV _{CC} | Scanning Supply Voltage (Pin 5) | | 8.1 | 9 | 9.9 | V |
| V _{CC} | Video & Chroma Supply Voltage (Pins 1-41) | | 8.1 | 9 | 9.9 | V |
| I _{cch} | Scanning Supply Current (pin 5) | No load | | 25 | 35 | mA |
| I _{ccv&c} | Video & Chroma Supply Current (Pins 1-41) | No load | | 45 | 55 | mA |
| P _D | Total Power Dissipation | No load | | 630 | 890 | mW |

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DC AND AC ELECTRICAL CHARACTERISTICS (continued)(H_{VCC} = V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--|---|--|------|------------|------|------------------|
| LUMINANCE INPUT (Pin 9) | | | | | | |
| V _{BW9} | Input Voltage | | | 350 | 490 | mV _{PP} |
| V _{DC9} | DC Level | No input signal | | 2.6 | | V |
| I _g | Input Current | • During burst period • Out of burst period | | ±150 | 1 | μA μA |
| G ₉ | Luma Gain | | | 7.4 | | |
| BW467 | Bandwidth (Y to R, G, B outputs) | -3dB | | 6 | | MHz |
| CONTRAST CONTROL (Pin 16) | | | | | | |
| V ₁₆ | Contrast Control Voltage | | | 2 to 4 | | V |
| V _{16 (Max.)} | Allowed Control Voltage | | | | 5 | V |
| G ₁₆ | Contrast Control Range | | | 20 | | dB |
| I ₁₆ | Input Current | | | | 10 | μA |
| BRIGHTNESS CONTROL (Pin 36) | | | | | | |
| V ₃₆ | Brightness Control Voltage | | | 1.8 to 4.3 | | V |
| V _{36 (Max.)} | Allowed Control Voltage | | | | 5 | V |
| I ₃₆ | Input Current | | | | 10 | μA |
| SATURATION CONTROL INPUT (Pin 27) | | | | | | |
| V ₂₇ | Saturation Control Voltage | | | 2 to 4 | | V |
| V _{27 (Max.)} | Allowed Control Voltage | | | | 5 | V |
| G ₂₇ | Saturation Control Range | | | -50 | | dB |
| V _{27M} | Mute Level | | | | 0.5 | V |
| I ₂₇ | Input Current | | | | 10 | μA |
| RGB OUTPUTS (Pins 4-6-7) | | | | | | |
| V _{BW 4-6-7} | Output Signal Amplitude (black to white) | • 0.35V B to W @ Pin 9 • Contrast @ 4V • Sat. & Brig. @ 3V | | 2.6 | | V |
| I ₄₋₆₋₇ | Individual Output Sinking Current | | | 2 | | mA |
| VM ₄₋₆₋₇ | Maximum Peak White Level | | | 7.8 | | V |
| V _{blank 4-6-7} | Blanking Level | | | 0.5 | | V |
| V _{CO min.} | Minimum Level of Inserted Cut-off Lines | | | 2.5 | | V |
| V _{CO max.} | Maximum Level of Inserted Cut-off Lines | | | 4.5 | | V |
| | Relative Variation in Black Level with Various CONT. SAT. BRIG between the 3 channels | | | | 20 | mV |
| ΔV _{temp} | Black Level Thermal Drift | | | 0.5 | | mV/°C |
| | Tracking between Luminance and Chrominance Signals over 10dB Contrast Control | | | | 2 | dB |
| RGB INPUTS (Pins 37-39-40) | | | | | | |
| V _{BW37-39-40} | Input Amplitude (B to W) | | | 0.7 | 2 | V |
| V _{clamp 37-39-40} | Clamp Level | Contrast max | | 1.8 | | V |
| I ₃₇₋₃₉₋₄₀ | Control Current | | | ±150 | | μA |
| I _{l37-39-40} | Leakage Current | | | | 1 | μA |
| BW ₃₇₋₃₉₋₄₀ | Bandwidth | -3dB | | 8 | | MHz |
| G _{CTR} | RGB Contrast Control Range | | | 14 | | dB |
| G ₃₇₋₃₉₋₄₀ | RGB Gain | | | 3.7 | | |

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STV2110A

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

($HV_{CC} = V_{CC} = 9V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|------------------------------|-----------------------------|-----------------|------|------|------|------|
| FAST BLANKING INPUT (Pin 35) | | | | | | |
| V_{TH1-35} | First Threshold (switching) | | | 0.7 | | V |
| V_{TH2-35} | Second Threshold (blanking) | | | 2.1 | | V |
| T_{switch} | Switching Delay | | | 50 | | ns |
| T_{blank} | Blanking Delay | | | 100 | | ns |

CATHODE CURRENT INPUT (Pin 42)

| | | | | | | |
|--------------------|---|--|-----|------|--|---------|
| V_{REF42} | Leakage Current Reference Voltage | | | 1.75 | | V |
| ΔV_{REF42} | CO Reference refered to Leakage Current Reference | | | 250 | | mV |
| I_{42} | Output Current | | 150 | | | μA |
| V_{sb42} | Start-beam Current Detection Reference Voltage | | | 2.4 | | V |

AUTOMATIC CUT-OFF (Pin 3-8-38)

| | | | | | | |
|--|------------------------------------|--|--|-----------|--|---------|
| | Cut-off Capacitor Clamping Current | | | ± 100 | | μA |
|--|------------------------------------|--|--|-----------|--|---------|

PAL CHROMINANCE INPUT (Pin 18)

| | | | | | | |
|----------------|---|--|--|-----|-----|-----------|
| V_{18} | Input Level | | | 0.3 | 1.0 | V_{PP} |
| $V_{burst-18}$ | Minimum Burst Signal Amplitude within the ACC Control Range | | | 30 | | mV_{PP} |
| G_{ACC} | ACC Control Range | Change of burst over whole ACC Control Range < 1dB | | 30 | | dB |
| R_{18} | Input Impedance | | | 8 | | $k\Omega$ |
| V_{DC-18} | DC Level | No input signal | | 3.5 | | V |

SECAM CHROMINANCE INPUT (Pin 17)

| | | | | | | |
|----------------|---|-----------------|--|-----|-----|-----------|
| V_{17} | Input Level | | | 0.3 | 1.0 | V_{PP} |
| $V_{burst-17}$ | Minimum Burst Signal Amplitude within the ACC Control Range | | | 30 | | mV_{PP} |
| R_{17} | Input Impedance | | | 20 | | $k\Omega$ |
| V_{DC-17} | DC Level | No input signal | | 3.5 | | V |

ACC CAPACITOR (Pin 30)

| | | | | | | |
|----------|------------------|--------------------------|--|-----|---|---------|
| I_{30} | Charging Current | During burst gate period | | 250 | | μA |
| I_{30} | Leakage Current | Out of burst gate period | | | 1 | μA |

PLL LOOP FILTER (Pin 34)

| | | | | | | |
|----------|-----------------|--|--|-----|--|---------|
| I_{34} | Control Current | | | 400 | | μA |
|----------|-----------------|--|--|-----|--|---------|

CHROMAXTAL (Pin 33)

| | | | | | | |
|-----------|----------------|--|--|-----------|--|----|
| CR_{33} | Catching Range | | | ± 700 | | Hz |
|-----------|----------------|--|--|-----------|--|----|

SUBCARRIER OUTPUT (Pin 22)

| | | | | | | |
|----------------|-----------------------------------|--------------------------|--|---|--|----------|
| $V_{burst-22}$ | Output Burst Amplitude (PAL mode) | Within ACC Control Range | | 2 | | V_{pp} |
|----------------|-----------------------------------|--------------------------|--|---|--|----------|

PAL KILLER CAPACITOR (Pin 32)

| | | | | | | |
|--------------|-----------------------------------|--|--|-----|--|---------|
| V_{OFF-32} | Color off Threshold | | | 5.0 | | V |
| V_{ON-32} | Color on Threshold | | | 5.4 | | V |
| V_{INH-32} | PAL Flip-flop Inhibition Level | | | 3.2 | | V |
| I_{32} | Control Current | | | 250 | | μA |
| V_{nom-32} | Voltage with Nominal Input Signal | | | 6.0 | | V |

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DC AND AC ELECTRICAL CHARACTERISTICS (continued)(HV_{CC} = V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--|---------------------------------------|--------------------------------|------------|-------------------------|------------------|-----------------|
| SECAM KILLER CAPACITOR (Pin 23) | | | | | | |
| V _{OFF-23} | Color off Threshold | | | 5.6 | | V |
| V _{ON-23} | Color on Threshold | | | 6 | | V |
| V _{INH-23} | SECAM Flip-flop Inhibition Level | | | 3.2 | | V |
| I ₂₃ | Control Current | | | 250 | | μA |
| V _{nom-23} | Voltage with Nominal input Signal | | | 7.3 | | V |
| DELAYED CHANNEL INPUT (Pin 20) | | | | | | |
| V _{DC-20} | DC Level | No input Signal | | 2.2 | | V |
| R ₂₀ | Input Impedance | PAL standard SECAM standard | | 8 20 | | kΩ kΩ |
| 4.25MHz AND 4.40MHz FILTER (Pins 28-31) | | | | | | |
| V _{DC-28-31} | DC Level | No input signal | | 2.3 | | V |
| R ₂₈₋₃₁ | Input Impedance | | | 20 | | kΩ |
| RED AND BLUE DEEMPHASIS CAPACITORS (Pins 26-29) | | | | | | |
| V _{DC-26-29} | DC Level | No input signal | | 6.4 | | V |
| R ₂₆₋₂₉ | Input Impedance | | | 6 | | kΩ |
| 4.32MHz FILTER (Pin 25) | | | | | | |
| V _{DC-25} | DC Level | No input signal | | 3.5 | | V |
| R ₂₅ | Input Impedance | | | 40 | | kΩ |
| FORCING/STANDARD IDENTIFICATION (Pin 21) | | | | | | |
| | Max.Current on PS Output | PAL SECAM | + 5 - 5 | | | mA mA |
| | DC Output Voltage | PAL SECAM | | 7.5 1.5 | | V V |
| | DC input Voltage | PAL SECAM | | HV _{CC} 0.0 | | V V |
| COMPOSITE VIDEO BASE BAND SIGNAL (Pin 12) | | | | | | |
| V _{REF-12} | Clamp Voltage | I ₁₂ = - 1μA | 1.6 | 1.85 | 2.1 | V |
| V ₁₂ | Video Input Signal (sync to white) | | | 1 | | V _{PP} |
| I ₁₂ | Sync Threshold | | | 12 | | μA |
| SCANNING XTAL (Pin 11) | | | | | | |
| F ₁₁ | Frequency after Divider | | | 15.625 | | kHz |
| CR ₁₁ | Frequency Control Range after Divider | | | ±700 | | Hz |
| PLL LOOP FILTER (Pin 10) | | | | | | |
| I _{low-10} | Output Current | Long time constant | | 0.15 | | mA |
| I _{high-10} | Output Current | Short time constant | | 0.40 | | mA |
| DELAYED LINE FLYBACK INPUT (Pin 13) | | | | | | |
| V _{TH-13} | Threshold | | | 0.6 | | V |
| V ₁₃ | Allowed Voltage Range | | - 0.4 | | HV _{CC} | V |
| I ₁₃ | Input Current | V ₁₃ < 0.6V | | | 5 | μA |

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STV2110A

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

($HV_{CC} = V_{CC} = 9V$, $T_{amb} = 25^{\circ}C$ unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|-----------------------|-----------------|------|------|-----------|---------|
| DIRECT BLANKING INPUT (Pin 2) | | | | | | |
| V_{TH-2} | Threshold | | | 0.6 | | V |
| V_2 | Allowed Voltage Range | | -0.4 | | HV_{CC} | V |
| I_2 | Input Current | $V_2 < 0.6V$ | | | 5 | μA |

HORIZONTAL OUTPUT (Pin 15)

| | | | | | | |
|-----------------|---------------------------------|-----------------|----|-----|----|---------|
| T_{15} | Output Pulse Width | | 26 | 28 | 29 | μs |
| V_{low-15} | Output Voltage (open collector) | $I_{15} = 10mA$ | | 1.5 | | V |
| $V_{5\ start}$ | HV_{CC} Start Threshold | | | 6.8 | | V |
| $V_{5\ stop}$ | HV_{CC} Stop Threshold | | | 6.2 | | V |
| Δt_{15} | $\phi 2$ Phase Range | | | 12 | | μs |

VERTICAL OUTPUT (Pin 14)

| | | | | | | |
|--------------|---------------------------------|--|--|------------|--|------|
| T_{14} | Output Pulse Width | | | 10.5 | | line |
| T_{sync1} | Frame Synchro. Window (search) | | | 248 to 352 | | line |
| V_{low-14} | Output Voltage (open collector) | | | 1 | | V |

2110A-07.TBL

Figure 1 : Contrast Control Curve

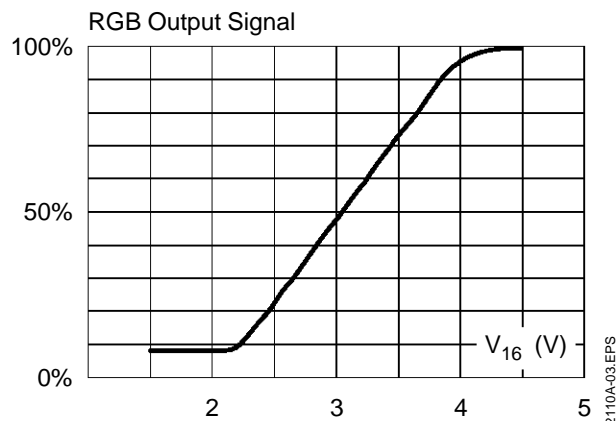


Figure 2 : Saturation Control Curve

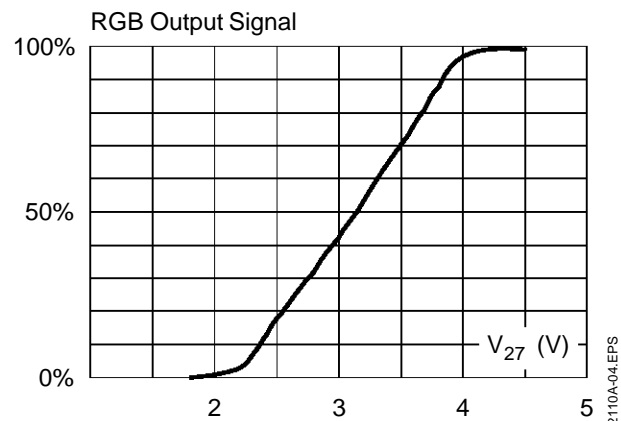


Figure 3 : Difference between Black Level and measuring Level at RGB Outputs as a function of the Brightness Control Input

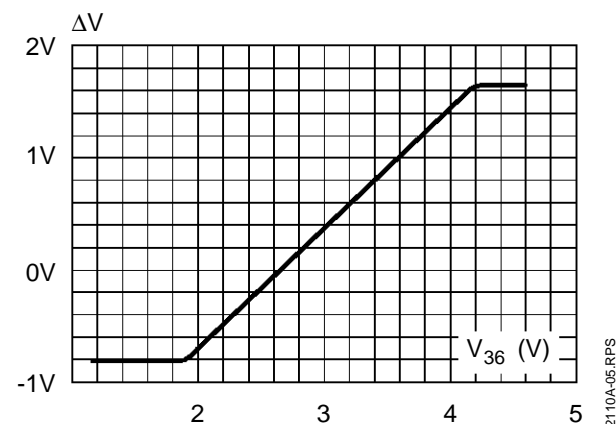
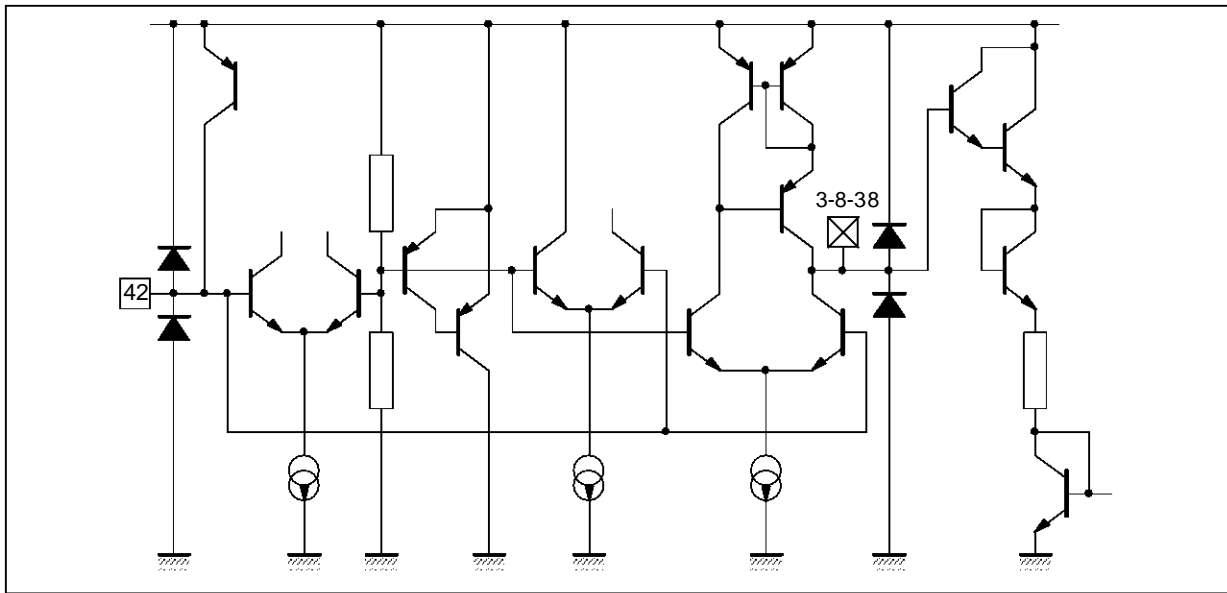
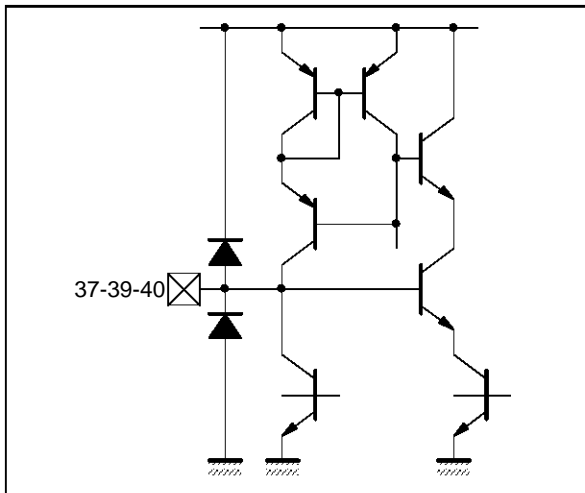


Figure 4 : Pins 3-8-38-42 (COG, COB, COR, ICAT)



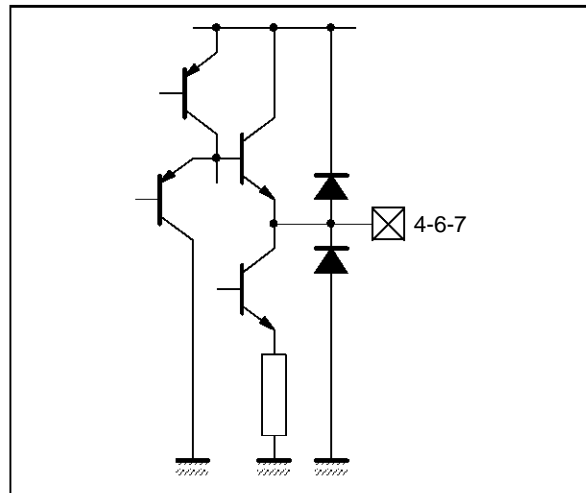
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Figure 5 : Pins 37-39-40 (RIN, GIN, BIN)



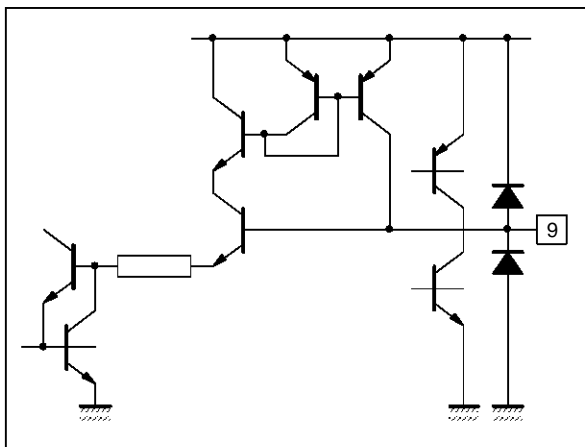
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Figure 6 : Pins 4-6-7 (ROUT, GOUT, BOUT)



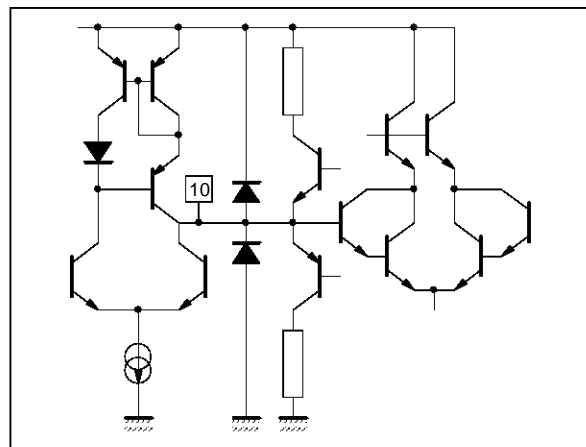
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Figure 7 : Pin 9 (YIN)



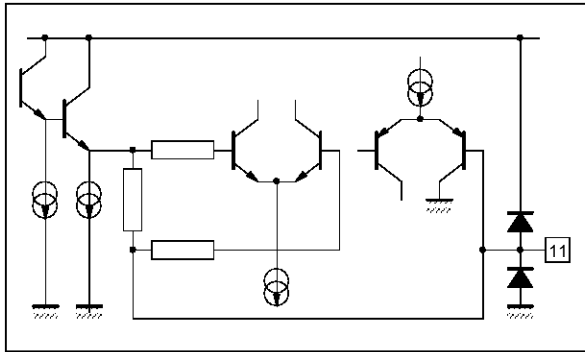
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Figure 8 : Pin 10 (SLPF)



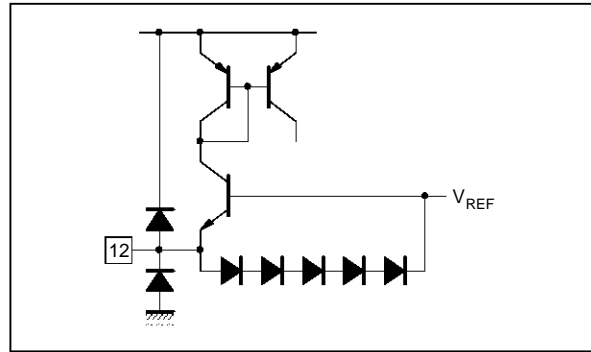
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Figure 9 : Pin 11 (SXTL)



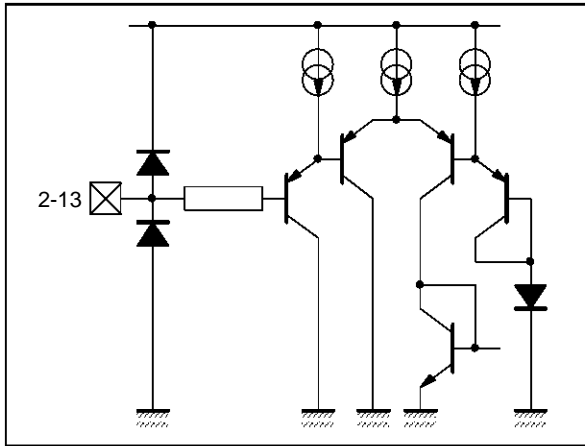
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Figure 10 : Pin 12 (CVBS)



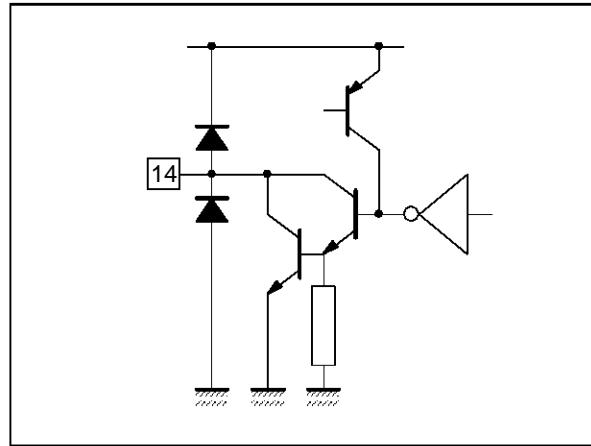
2110A-12.EPS

Figure 11 : Pins 2-13 (BLK, LFB)



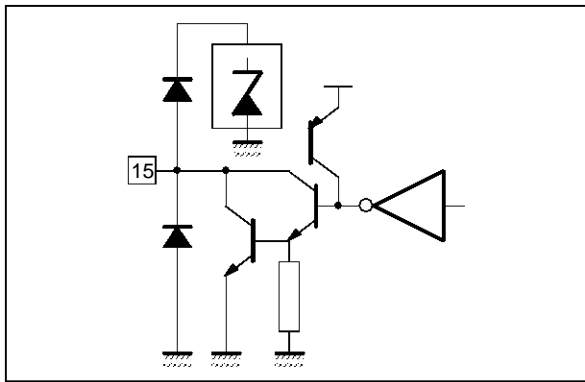
2110A-13.EPS

Figure 12 : Pins 14 (VOUT)



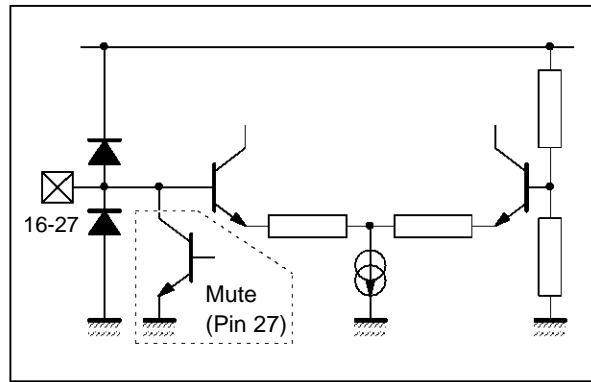
2110A-14.EPS

Figure 13 : Pin 15 (HOUT)



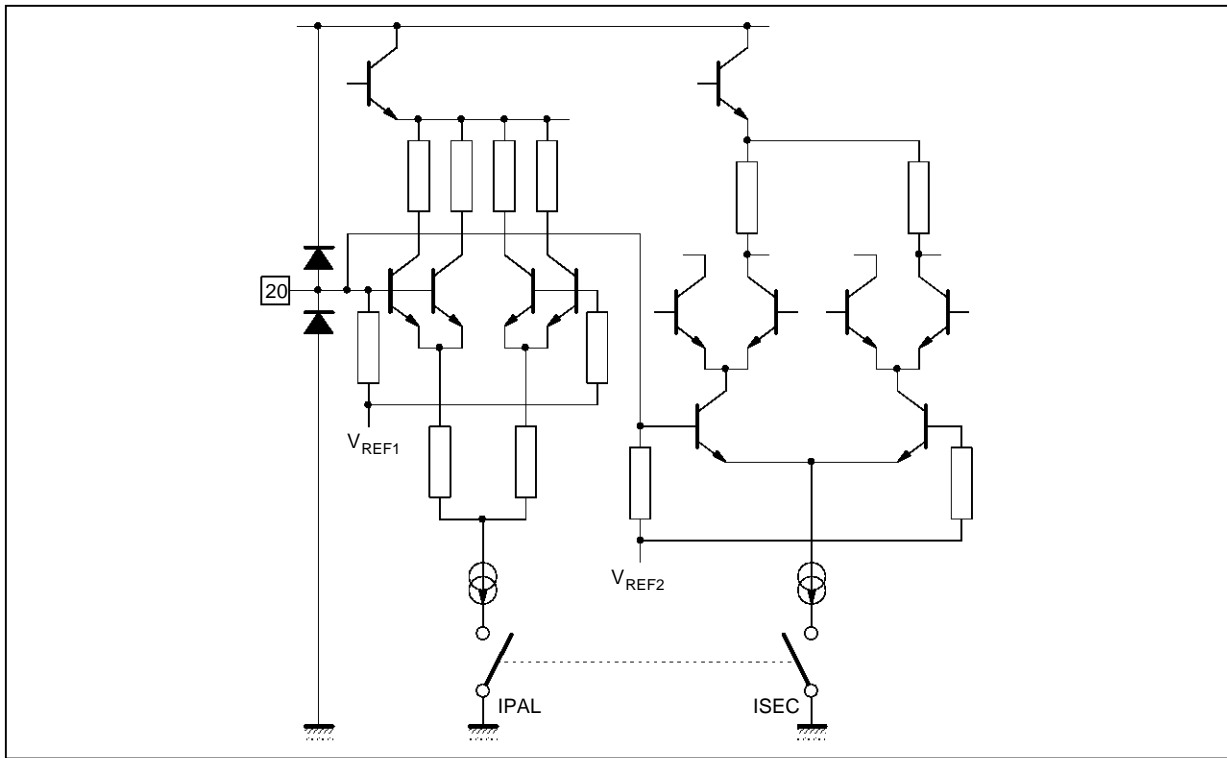
2110A-15.EPS

Figure 14 : Pins 16-27 (CTR, SAT)



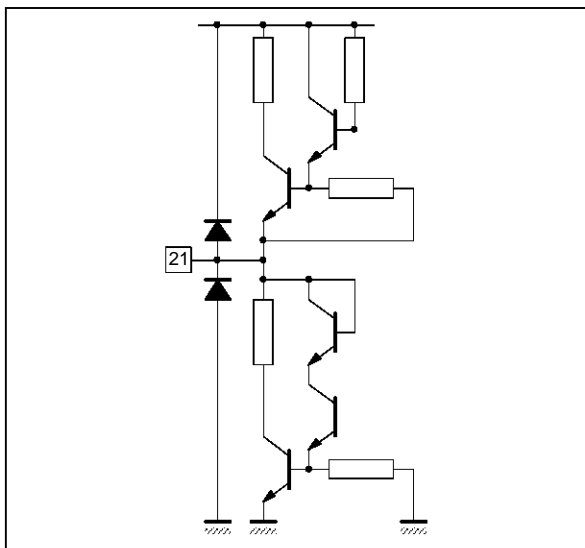
2110A-16.EPS

Figure 15 : Pin 20 (DLI)



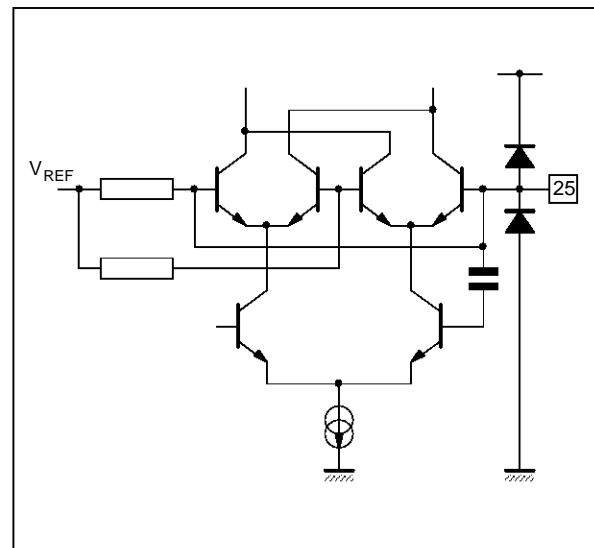
2110A-17.EPS

Figure 16 : Pin 21 (PS)



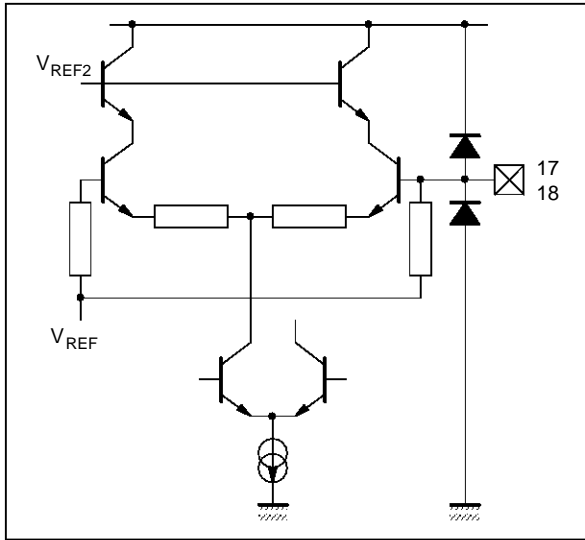
2110A-18.EPS

Figure 17 : Pin 25 (F432)



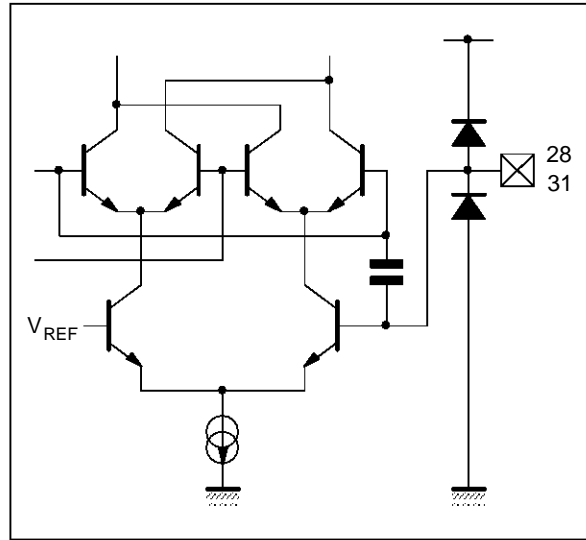
2110A-19.EPS

Figure 18 : Pins 17-18 (SECIN, PALIN)



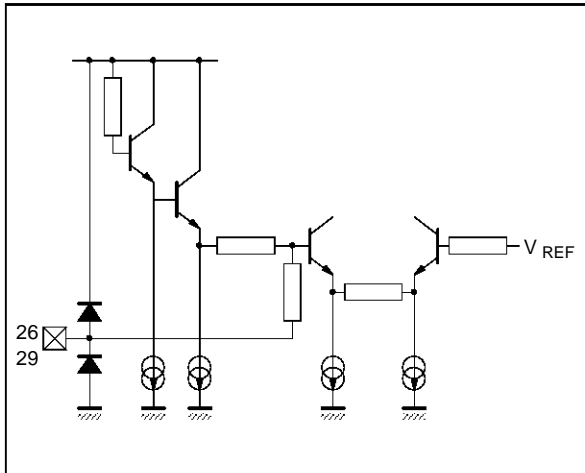
2110A-20.EPS

Figure 19 : Pins 28-31 (F440, F425)



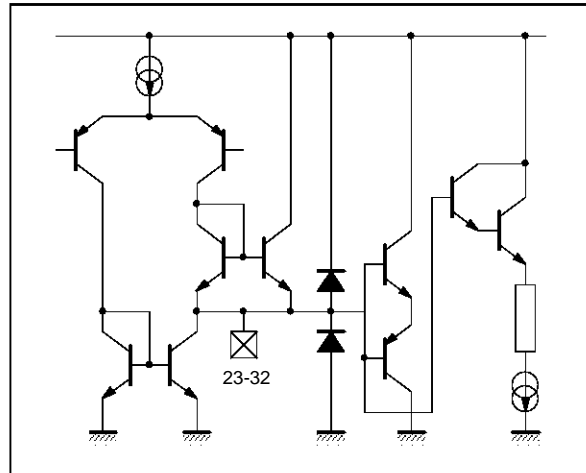
2110A-21.EPS

Figure 20 : Pins 26-29 (CDB, CDR)



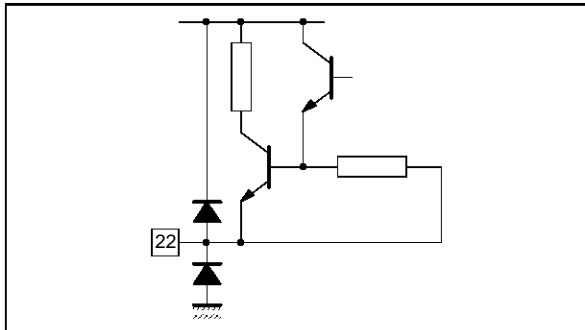
2110A-22.EPS

Figure 21 : Pins 23-32 (CKS, CKP)



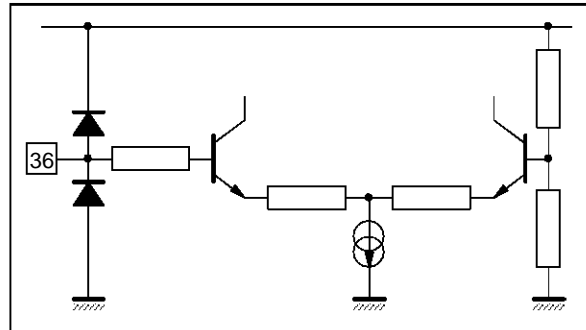
2110A-23.EPS

Figure 22 : Pin 22 (DLO)



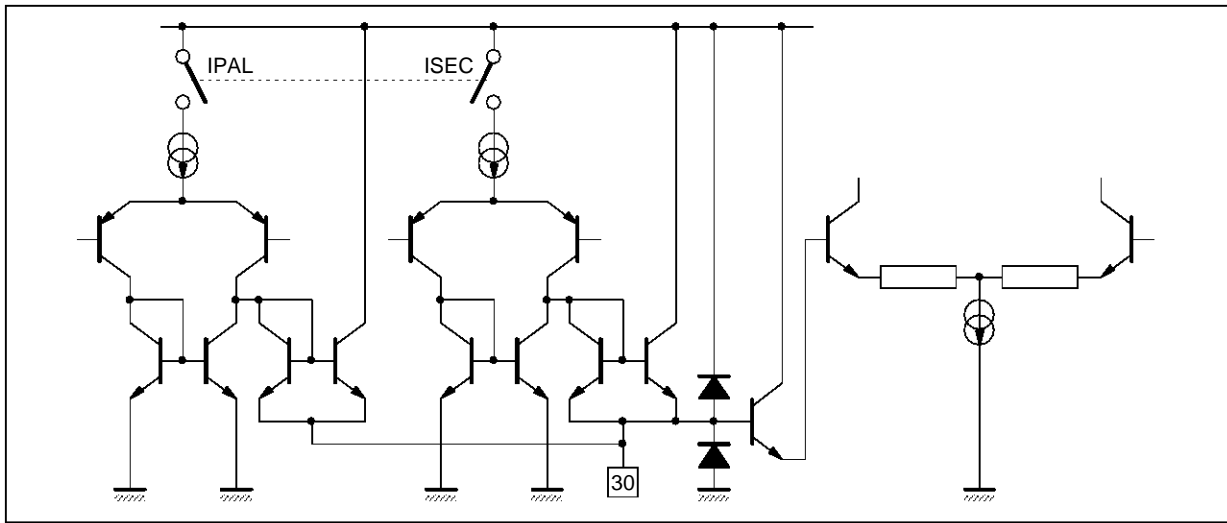
2110A-24.EPS

Figure 23 : Pin 36 (BRIG)



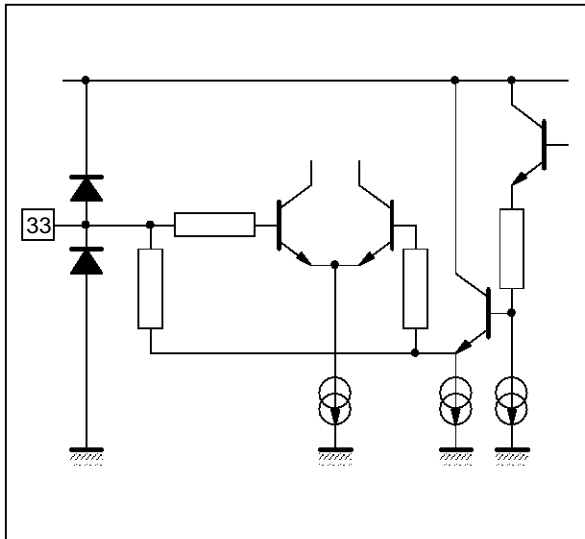
2110A-25.EPS

Figure 24 : Pin 30 (ACC)



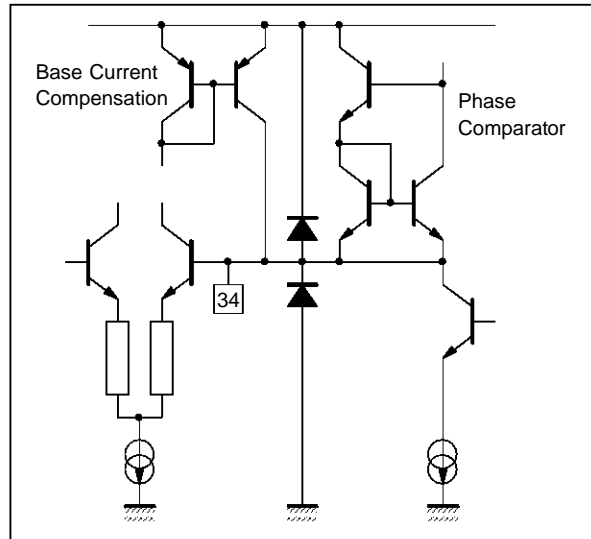
2110A-26.EPS

Figure 25 : Pin 33 (CXTL)



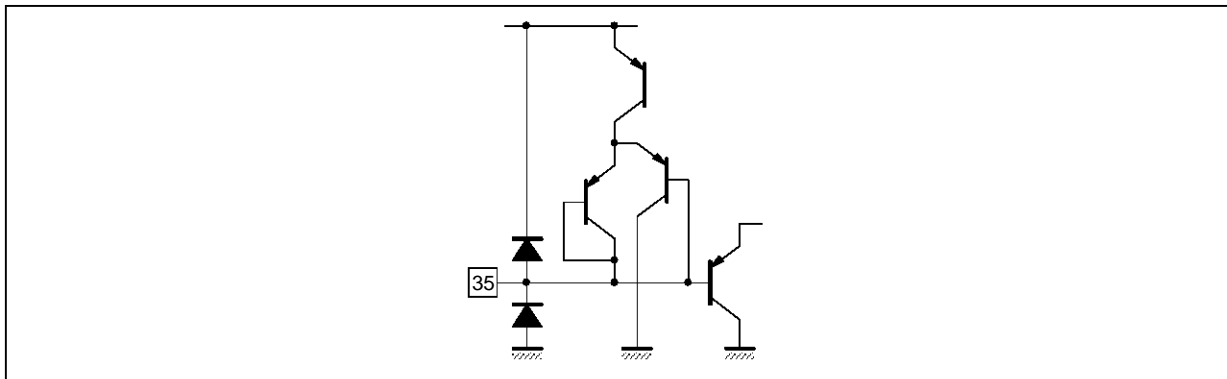
2110A-27.EPS

Figure 26 : Pin 34 (CLPF)



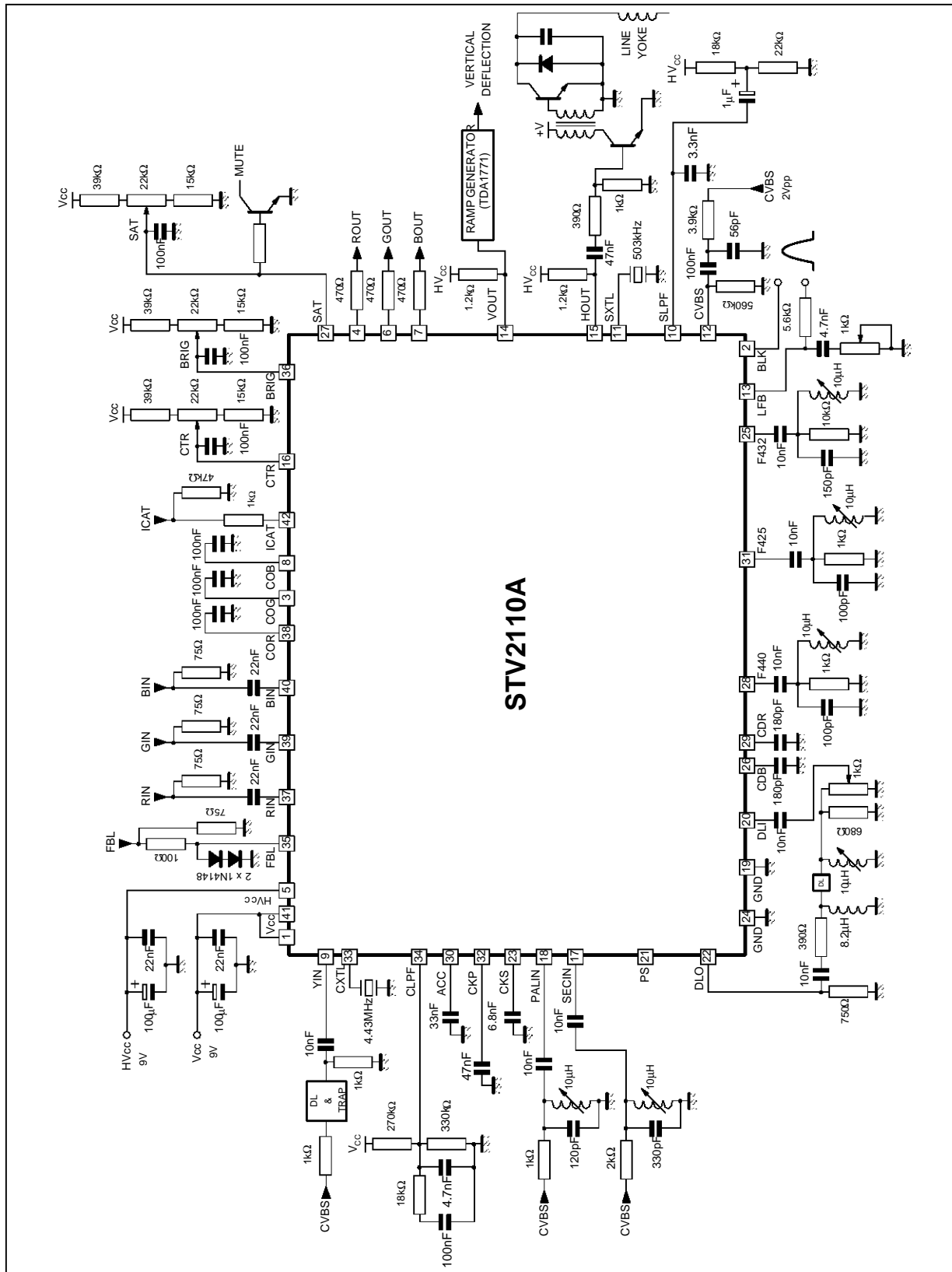
2110A-28.EPS

Figure 27 : Pin 35 (FBL)



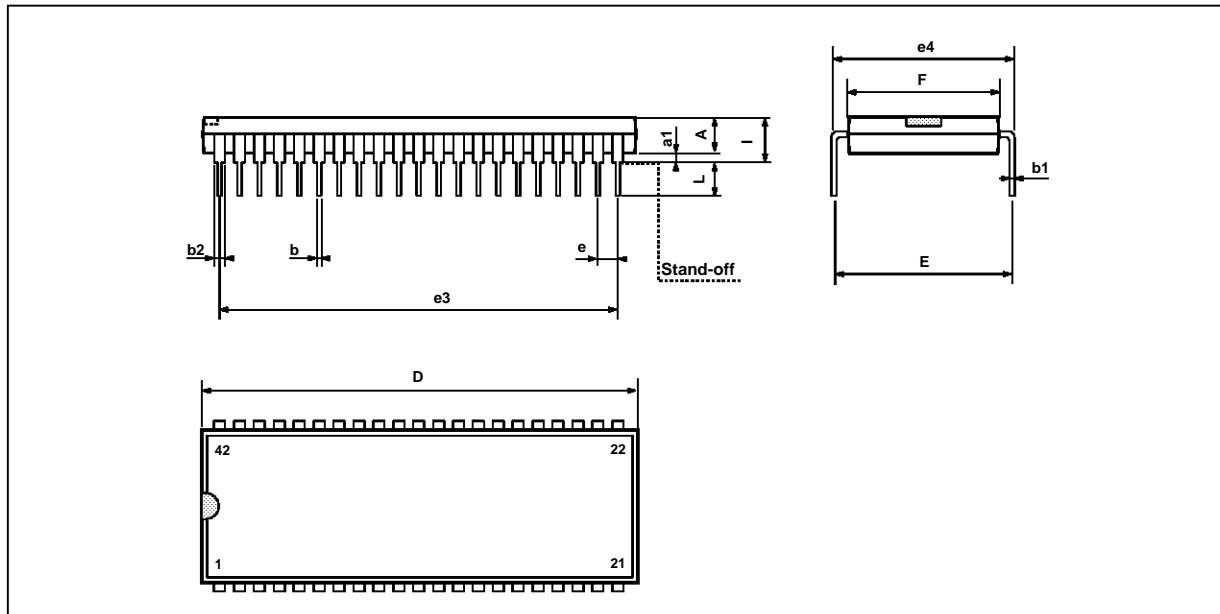
2110A-29.EPS

APPLICATION DIAGRAM



2110A-30.EPS

PACKAGE MECHANICAL DATA
42 PINS - PLASTIC SHRINK DIP



PMSDIP42.EPS

| Dimensions | Millimeters | | | Inches | | |
|------------|-------------|-------|-------|--------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 3.30 | | | 0.130 | | |
| a1 | | 0.51 | | | 0.020 | |
| b | | 0.35 | 0.59 | | 0.014 | 0.023 |
| b1 | | 0.20 | 0.36 | | 0.008 | 0.014 |
| b2 | | 0.75 | 1.42 | | 0.030 | 0.056 |
| b3 | | 0.75 | | | 0.030 | |
| D | | | 39.12 | | | 1.540 |
| E | | 15.57 | 17.35 | | 0.613 | 0.683 |
| e | 1.778 | | | 0.070 | | |
| e3 | 35.56 | | | 1.400 | | |
| e4 | 15.24 | | | 0.600 | | |
| F | | | 14.48 | | | 0.570 |
| i | | | 5.08 | | | 0.200 |
| L | | 2.54 | | | 0.100 | |

SDIP42.TBL

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