STw4811M
STw4811N

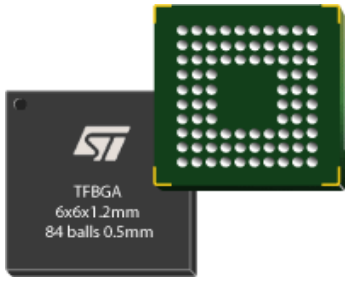
Power management for multimedia processors

Features

- 2 step-down converters
  - 1 to 1.45 V with 15 steps at 700 mA
  - 1.8 V at 600 mA for general purpose usage
- 3 low-drop output regulators for different uses
  - PLL analog supplies:
    1.05 V, 1.2 V, 1.3 V 1.8 V - 10 mA
  - Processor analog functions:
    2.5 V - 10 mA
  - Auxiliary device:
    1.5 V, 1.8V , 2.5 V, 2.8 V - 150 mA
- USB OTG module
  - Full and low speed USB OTG transceiver
  - Charge-pump (5 V, 100 mA) for USB cable
- Mass memory cards (SD/MMC/SDIO)
  - 1 linear regulator: 1.8 V, 1.85 V, 2.6 V,
    2.7 V, 2.85 V, 3 V, 3.3 V - 150 mA
  - Level shifter
- Miscellaneous
  - 32 kHz control for multimedia processor
  - Processor supply monitoring
  - Processor reset control
  - 2 serial I2C interfaces

Applications

- ST Nomadik™ STn881x
- Multimedia processor
- Mobile phones, PDA, videophone



STw4811
TFBGA 84
6x6x1.2mm
0.5mm pitch

STw4811
VFBGA 84
4.6x4.6x1.0mm
0.4mm pitch

Description

STw4811 is a power management companion chip for multimedia processors used in portable applications. It supplies the multimedia processor including its memories and peripherals. STw4811 supports the main mass memory standard cards. SDIO™ is also supported and allows to connect multimedia peripherals like cameras.

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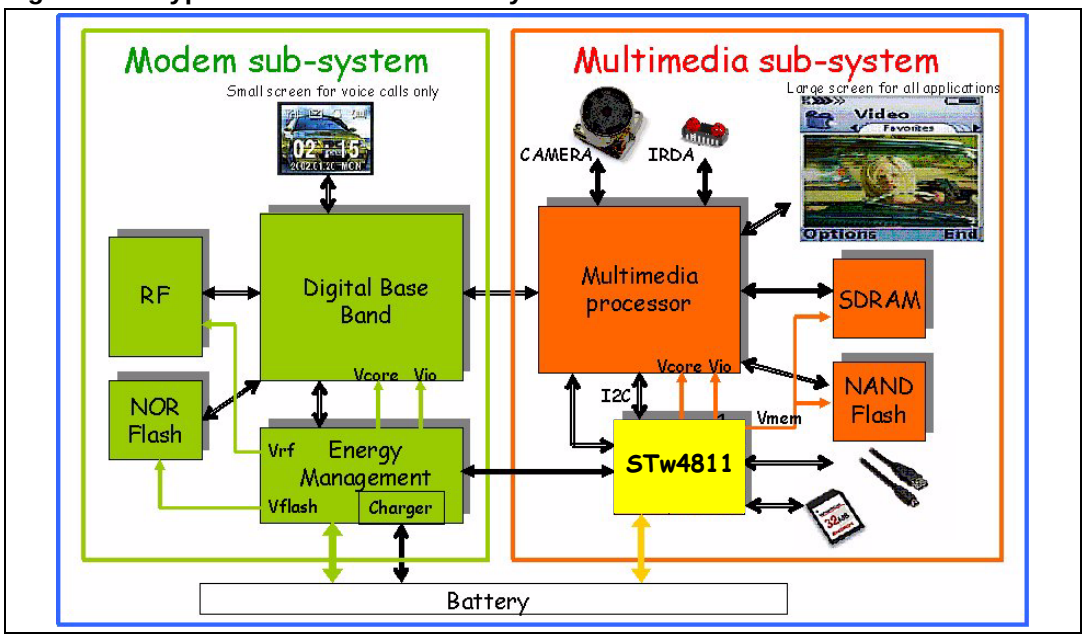
1 Overview

The STw4811 power management device has the following features:

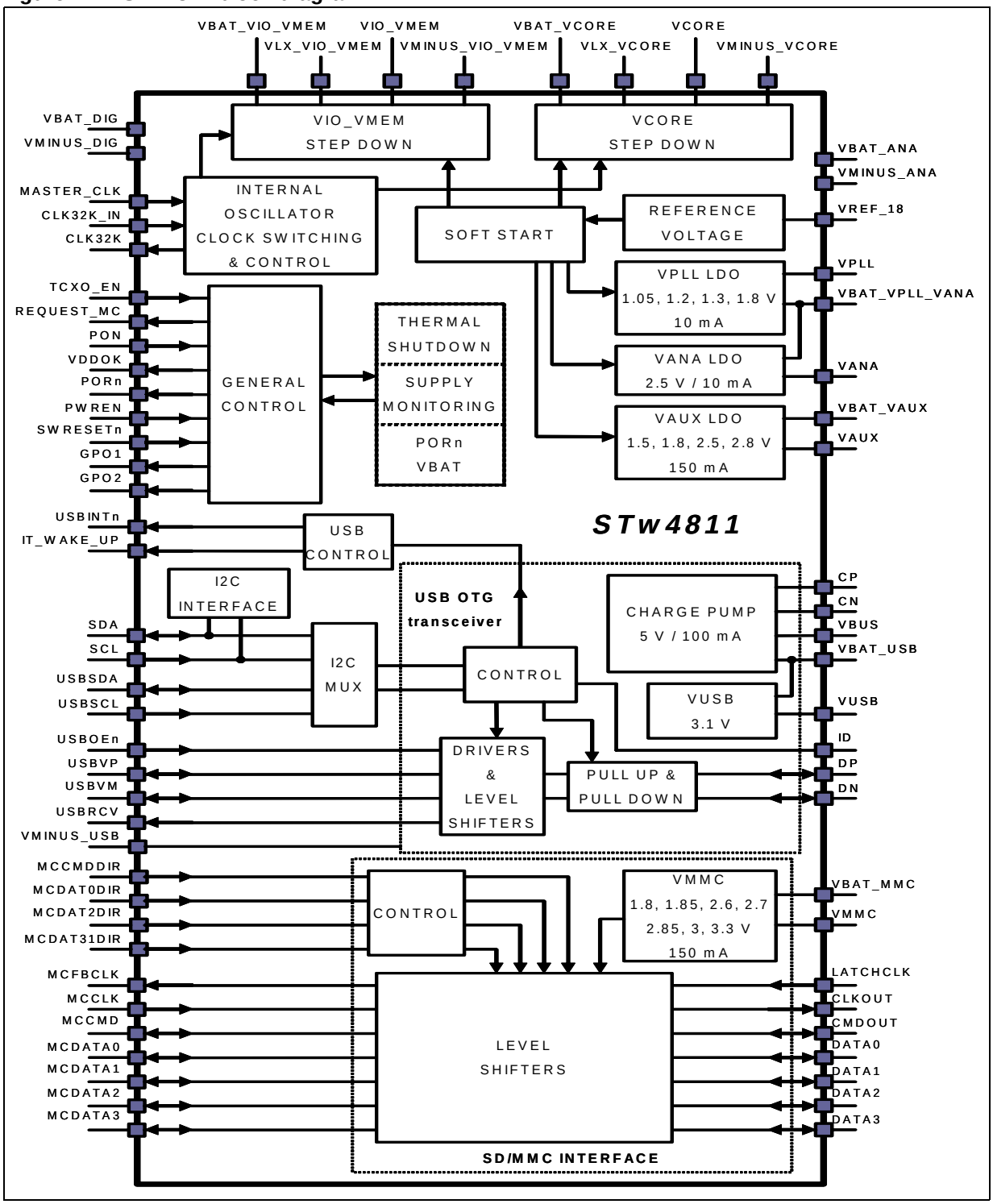
- Power management module
  - 1 step-down converter for processor core (1 V to 1.45 V with 15 steps at 700 mA)
  - 1 step-down converter (1.8 V at 600 mA) for general purpose usage such as processor input/output supply, external memory, DDR and SDRAM and peripherals
  - 1 low-drop output regulator for analog supplies, such as PLL (1.05 V, 1.2 V, 1.3 V, 1.8 V at 10 mA)
  - 1 low-drop output regulator for processor analog functions (2.5 V at 10 mA)
  - 1 low-drop output regulator for auxiliary devices (1.5 V, 1.8 V, 2.5 V, 2.8 V at 150 mA)
- Auxiliary device
  - STw4811M: Vaux OFF at start up
  - STw4811N: Vaux ON at start up
- USB OTG module
  - Full and low speed USB OTG transceiver
  - 1 linear regulator 3.1 V supplying transceiver
  - 1 charge-pump (5 V at 100 mA) supplying VBUS line of the USB cable
- Mass memory cards (SD/MMC/SDIO)
  - 1 linear regulator (1.8 V, 1.85 V, 2.6 V, 2.7 V, 2.85 V, 3 V, 3.3 V at 150 mA)
  - Level shifters
- Miscellaneous
  - 32 kHz control for multimedia processor
  - Processor supply monitoring
  - Processor reset control
  - 2 serial I2C interfaces

Figure 1. Typical mobile multimedia system



2 Functional block diagram

Figure 2. STw4811 block diagram



3 Ball information

3.1 Ball connections

Table 1. STw4811 ball connections

	1	2	3	4	5	6	7	8	9	10
A	CLK32K_IN	VMINUS_ VIO_VMEM	VLX_VIO_ VMEM	VBAT_VIO_ VMEM	VIO_VMEM	VAUX	VANA	VPLL	VREF_18	VCORE
B	“Reserved”	REQUEST_ MC	VMINUS_ VIO_VMEM	VBAT_VIO_ VMEM	VMINUS_ ANA	VBAT_ VAUX	“Reserved”	“Reserved”	“Reserved”	VMINUS_ VCORE
C	TCXO_EN	IT_WAKE_ UP	VMINUS_ DIG	VLX_VIO_ VMEM	“Reserved”	VBAT_ANA	VBAT_ VPLL_ANA	PON	VMINUS_ VCORE	VLX_ VCORE
D	VBAT_DIG	MASTER_ CLK	“reserved”					VLX_ VCORE	VBAT_ VCORE	VBAT_ VCORE
E	DATAOUT0	DATAOUT <1>	DATAOUT <2>					ID	DP	DN
F	DATAOUT <3>	CMDOUT	LATCHCLK					“Reserved”	VBAT_USB	VUSB
G	CLKOUT	MCCLK	MCCMD DIR					“Reserved”	USBSCL	VBUS
H	MCCMD	MCDATA <3>	MCDATA <1>	MCDATA31 DIR	MCFBCLK	PWREN	SDA	USBINTn	USBSDA	CP
J	MCDATA <2>	VDDOK	PORN	VBAT_ MMC	GPO1	SCL	USBVP	USBVM	VMINUS_ USB	CN
K	MCDATA0	MCDAT0 DIR	CLK32K	SW_ RESET	VMMC	GPO2	USBRCV	USBOEn	MCDAT2 DIR	“Reserved”

3.2 Ball functions

STw4811 includes the following ball types

- VDDD/VDDA: digital/analog power supply
- VSSD/VSSA: digital/analog ground supply
- DO/DI/DIO: digital output / digital input / digital input output
- DOz: digital output with high impedance capability
- AO/AI/AIO: analog output / analog input / analog input-output
- G: to be connected to ground
- O: to be left open
- Int-Ref: associated to internal reference

Table 2 details the ballout.

Table 2. STw4811 balls function

Ball	Ball name	Ball type	Description
General supplies			
D1	VBAT_DIG	VDDD-VBAT	Battery supply for digital/oscillator
C3	VMINUS_DIG	VSSD	Ground for digital and oscillator
C6	VBAT_ANA	VDDA-VBAT	Battery supply for analog
B5	VMINUS_ANA	VSSA	Ground for analog
F9	VBAT_USB	VDDA-VBAT	Battery supply for USB block
J9	VMINUS_USB	VSSA	Ground for USB block
A9	VREF_18	Int-Ref	Internal reference
Control balls			
C8	PON	DI(VBAT) Pull down 1.5MΩ	Power-on and reset
K4	SW_RESETn	DI(VIO_VMEM) Pull up 1.5MΩ	Software reset. Reset all registers except *power control* and *configuration 2* (address 20h) registers when SW_RESETn = 0
J2	VDDOK	DO(VIO_VMEM)	Supply monitoring for multimedia processors. Interruption for high temperature warning
J3	PORn	DO(VIO_VMEM)	Multimedia processor Resetn
H6	PWREN	DI(VIO_VMEM) Pull Up 1.5MΩ	Sleep mode from multimedia processor
C1	TCXO_EN	DI(VIO_VMEM) Pull Down 1.5MΩ	Request of master clock from modem part
B2	REQUEST_MC	DO(VIO_VMEM)	Request to master clock oscillator
J6	SCL	DI(VIO_VMEM)	Clock for Main I2C interface
H7	SDA	DIO(VIO_VMEM)	SDA for Main I2C interface
D2	MASTER_CLK	AI Pull Down 1.5MΩ	26 MHz, 13 MHz or 19.2 MHz from modem
A1	CLK32K_IN	DI(VIO_VMEM) Pull down 1.5MΩ	32 kHz input
K3	CLK32K	DO(VIO_VMEM)	32 kHz to multimedia processor

Table 2. STw4811 balls function (continued)

Ball	Ball name	Ball type	Description
General supplies			
Regulator balls			
A4 B4	VBAT_VIO_VMEM	VDDA-VBAT	Battery power supply for step down VIO_VMEM
A2 B3	VMINUS_VIO_VMEM	VSSA	Ground for step down VIO_VMEM
A3 C4	VLX_VIO_VMEM	AIO	BUCK of step down VIO_VMEM
A5	VIO_VMEM	AI	VIO_VMEM Feed back input
D9 D10	VBAT_VCORE	VDDA-VBAT	Battery power supply for step down VCORE
B10 C9	VMINUS_VCORE	VSSA	Ground for step down VCORE
C10 D8	VLX_VCORE	AIO	BUCK of step-down VCORE
A10	VCORE	AI	VCORE sense
C7	VBAT_VPLL_ANA	VDDA-VBAT	Battery supply for VPLL, VANA
A7	VANA	AO	VANA output
A8	VPLL	AO	VPLL output
A6	VAUX	AO	VAUX output
B6	VBAT_VAUX	VDDA-VBAT	Battery supply for VAUX
USB balls			
C2	IT_WAKE_UP	DO (Open drain)	Interrupt to modem or APE for wake-up due to USB plug
K8	USBOEn	DIO(VIO_VMEM) Pull down 1.5MΩ	Output enable of the differential driver in the USB mode
J7	USBVP	DIO(VIO_VMEM) Pull down 1.5MΩ	Data input in the USB transmit mode, positive data input the single-ended transmit mode, or TXD in UART mode
J8	USBVM	DIO(VIO_VMEM) Pull Down 1.5MΩ	Single-ended zero input in the USB transmit mode, negative data input in the single-ended transmit mode, or RXD in the UART mode
K7	USBRCV	DO(VIO_VMEM)	Differential receiver output
E9	DP	AIO(VUSB)	Positive data line in the USB mode, or serial data input in the UART mode
E10	DN	AIO(VUSB)	Negative data line in the USB mode, or serial data output in the UART mode.
E8	ID	AI(VBAT-USB)	ID ball of the USB detector used for protocol identification.

Table 2. STw4811 balls function (continued)

Ball	Ball name	Ball type	Description
General supplies			
H10	CP	AIO(VBUS)	C plus flying capacitor (VBUS level 4.4 to 5.25)
J10	CN	AIO(VBUS)	C minus flying capacitor (VBUS Level)
G10	VBUS	AIO(VBUS)	USB cable supply (VBUS Level)
F10	VUSB	AIO	Decoupling capacitor for USB internal regulator
G9	USBSCL	DI(VIO_VMEM)	Clock for dedicated USB I2C
H9	USBSDA	DIO(VIO_VMEM)	SDA for dedicated USB I2C
H8	USBINTn	DO(VIO_VMEM)	Interrupt to multimedia processor for USB or accessory plug
SD/MMC/SDIO balls			
G3	MCCMDDIR	DI(VIO_VMEM) Pull down 1.5MΩ	CMD direction. - “high”: CMD signal from processor to card - “Low”: CMD signal from card to processor
K2	MCDAT0DIR	DI(VIO_VMEM) Pull down 1.5MΩ	DATA0 direction - “high”: DATA0 signal from processor to card - “Low”: DATA0 signal from card to processor
K9	MCDAT2DIR	DI(VIO_VMEM) Pull down 1.5MΩ	DATA2 direction - “high”: DATA2 signal from processor to card - “Low”: DATA2 signal from card to processor
H4	MCDAT31DIR	DI(VIO_VMEM) Pull down 1.5MΩ	DATA(3,1) direction - “high”: DATA(3,1) signal from processor to card - “Low”: DATA(3,1) signal from card to processor
G2	MCCLK	DI(VIO_VMEM) Pull Down 1.5MΩ	Host clock, between processor and STw4811, to the card (processor clock).
H5	MCFBCLK	DO(VIO_VMEM)	Host feedback clock between STw4811 and processor, to re-synchronize data in processor.
H1	MCCMD	DIO(VIO_VMEM) Pull Up 1.5MΩ	Bidirectional command/response signal between processor and STw4811.
K1	MCDATA0	DIO(VIO_VMEM) Pull Up1.5MΩ	Bidirectional data0 between processor and STw4811
H2 H3 J1	MCDATA[3:1]	DIO(VIO_VMEM) Pull up 1.5MΩ	Bidirectional data [3:1] between processor and STw4811.
F3	LATCHCLK	DI(VMMC) Pull down 1.5MΩ	Host feedback clock to STw4811, to re-synchronize data in processor.
G1	CLKOUT	DO(VMMC)	Host clock, between STw4811 and card (processor clock).
F2	CMDOUT	DIO(VMMC) Pull up 1.5MΩ	Bidirectional command/response signal between STw4811 and processor.

Table 2. STw4811 balls function (continued)

Ball	Ball name	Ball type	Description
General supplies			
E1	DATAOUT0	DIO(VMMC) Pull up 1.5MΩ	Bidirectional data0 between STw4811 and card
F1 E3 E2	DATAOUT[3:1]	DIO(VMMC) Pull up 1.5MΩ	Bidirectional data[3:1] between STw4811 and card.
J4	VBAT_MMC	VDDA-VBAT	Battery supply for VMMC
K5	VMMC	AIO	VMMC supply output
Other balls			
J5	GPO1	AO	General purpose output
K6	GPO2	AO	General purpose output
B9 D3	“Reserved”	G	To be connected to ground
B1 B7 B8 C5 F8 G8 K10	“Reserved”	O	To be left open

4 Functional description

4.1 Introduction

The STw4811 integrates all the power supplies for a multimedia processor as well as memories and peripherals:

- Two switched mode power supply regulators: one for the multimedia processor core, one for multimedia processor I/Os and memories
- Three low-drop output regulators for multimedia processor analog supplies (PLL and others) and auxiliary components
- USB OTG FS/LS physical interface
- MMC card power supplies and level shifters
- Multimedia processor supply monitoring / power-on reset and power supply alarms / interrupt management
- Two serial I2C communication interfaces; one to control the devices (SDA, SCL) and one to control the USB (USBSDA, USBSCL).

4.2 Digital control module

This module describes the interfaces used to program the device and the related registers.

4.2.1 State machine

Description of each states: (*Figure 3.*)

OFF: In this mode the STw4811 is switched off. Off is when PON=0, when battery level is under 2.4 V or when thermal shutdown is activated. There is no multimedia processor power supply. The only active cell is the USB cable detection and V_{BAT} level detection.

OSC_START: Oscillator is enabled and the power up module is waiting for the rising edge of the internal signal OSC_OK to start power up sequence. This state duration is 300 µs.

START_BIAS: Bias, reference and thermal shut-down are enabled, a counter is activated to wait for rising edge of internal signals PDN_regulators. This state duration has a typical value of 7.77 ms and a worst case value of 9.46 ms.

START_PM: after a 1 ms wait, multimedia processor power supplies are available (VIO_VMEM, VCORE, VPLL, and VANA). The device can allow I2C communication, output power supply monitoring and application (USB,SD/MMC/SDIO).

OFF2: STw4811 is waiting for the 32 kHz multimedia processor signal. This state has an indeterminate duration. If 32kHz is present during the states describes above, it has no effect. The 32 kHz signal is taken into account by STw4811 only when the ‘VDDOK’ ball is high, that is at the end of START_PM state.

RESET: STw4811 forces a reset during 11*1/32 kHz period before setting PORn high.

INT_OSC: The STw4811 can work without MASTER_CLK via its internal oscillator. The device waits for an external clock detection before switching to the external clock. When receiving a rising edge on PWREN ball (coming from multimedia processor) or on TCXO_EN ball (coming from modem), STw4811 answers by asserting to “1” the

REQUEST_MC ball. STw4811 remains in internal oscillator mode until it receives the external clock signal on MASTER_CLK ball (optional).

EXT_CLK: if MASTER_CLK is used, when detected, the STw4811 uses this clock as reference and switches off its internal oscillator. MASTERCLK should remain connected up to sleep mode.

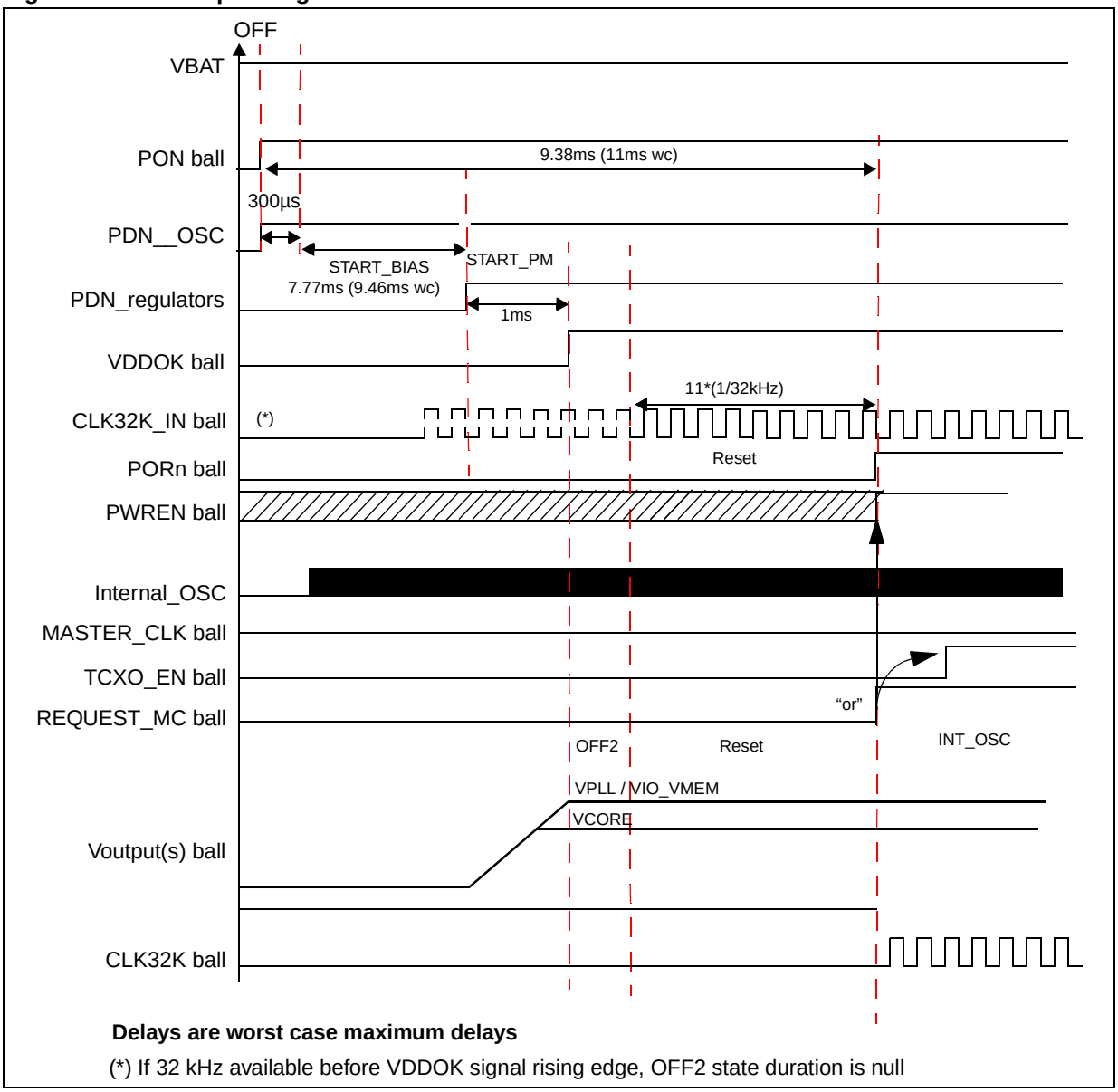
SLEEP: sleep mode is required by multimedia processor by setting a PWREN at low level. Then VDDOK is forced to 0, regulators (VCORE, VIO_VMEM) switch to sleep mode and wait for PWREN at high level (*Figure 4*).

WAKE-UP: from sleep mode, the multimedia processor requests to switch back to high power mode. Thus the device restarts its internal oscillator and then switches regulators from SLEEP to high power mode and informs multimedia processor with VDDOK at high level (*Figure 4*).

Note: The default state of VAUX is different for STw4811M and for STw4811N.
- VAUX default state is OFF at start up for STw4811M.
- VAUX default state is ON at start up for STw4811N.
VAUX can be programmed in high power mode only by asserted pdn_vaux bit to “1” (Table 18).

If MASTER_CLK is used instead of internal oscillator all the features are not supported in sleep mode (see Section 4.2.3).

Figure 3. Start-up timing

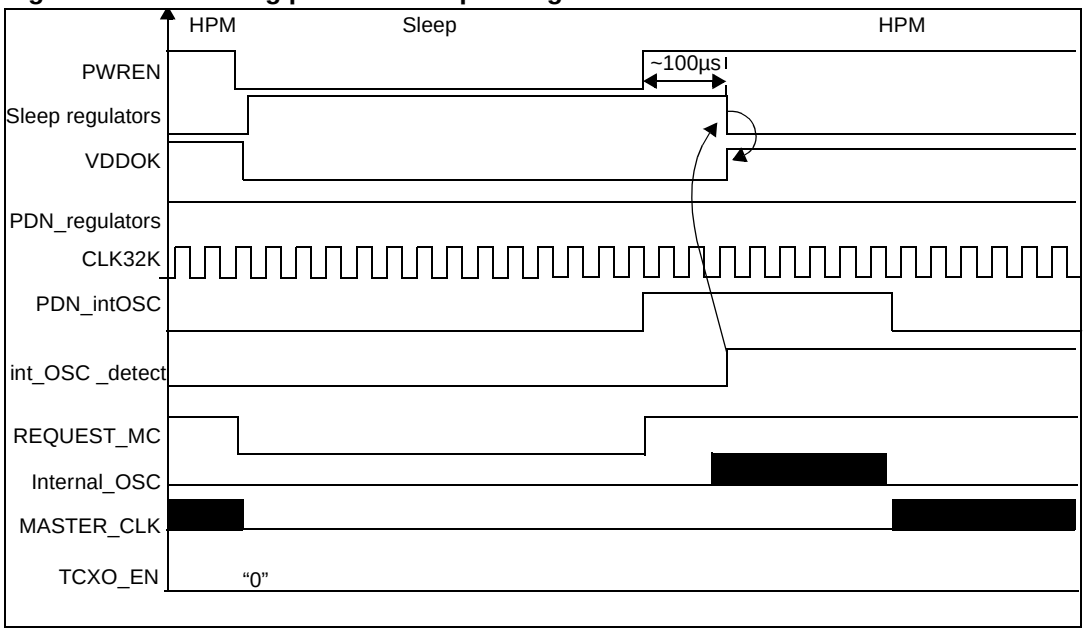


Delays are worst case maximum delays

(*) If 32 kHz available before VDDOK signal rising edge, OFF2 state duration is null

All regulators are started with PDN_regulators or EN_regulators but can be switched off from the beginning or during application by software, 'pdn_(regulator)' or 'en_(regulator)' bits (*Table 18*,*Table 24*, and *Table 25*).

Figure 4. Switching power to sleep timing



Register reset

In the event of a hardware reset coming from the modem, PON ball set to "0", all registers are reset at initial value when PON ball goes back to "1" level.
A software reset from multimedia processor of STw4811, through SW_RESETn ball set to "0", resets all registers except *power control* register (at address 1E & 1F) and the *configuration 2* register at address 20h.

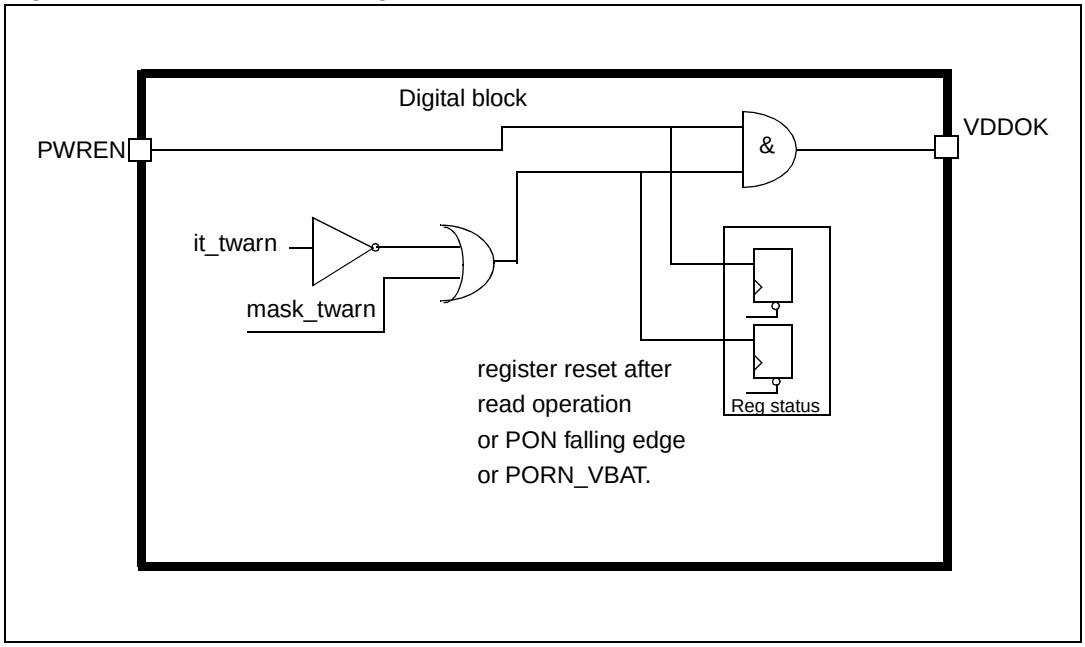
Main clock oscillator control

REQUEST_MC is an OR output gate between PWREN (coming from multimedia processor) and TCXO_EN (coming from modem supply), it is synchronized on 32 kHz, except during power-up where PWREN is masked and considered as high.
REQUEST_MC enabled or disabled the master clock oscillator device.

4.2.2 POWER OFF / VDDOK

- In case of VDDOK falling edge due to under voltage on VCORE or VIO_VMEM detection, or 'it_twarn' bit set to "1" (*Table 18*); the multimedia processor is then reset (PORn low during a minimum time of 333 µs) and restarted with no time-out. (see *Figure 5*). In case of VDDOK falling edge because PWREN balls equals "0", there is no reset (PORn still high).
- In case of PON falling edge (STw4811 switched off from modem); the multimedia processor is also reset with no time-out. We consider that clean switch off between modem and multimedia processor is done by software directly.

Figure 5. VDDOK block diagram



4.2.3 Sleep mode

STw4811 goes into sleep mode by different ways. Whether VCORE, VIO_VMEM and VAUX are programmed to sleep mode or not is indicated in *Table 26* and *Table 27*.

Taking in account the bit programming from *Table 26* and *Table 27*, sleep mode is summarized with the following formula:

SLEEP = ('vxxx_sleep' x $\overline{\text{PWREN}}$) + ('vxxx_force_sleep') = 1
(vxxx = vcore or vio_vmem or vaux)

Note: The configuration vxxx_sleep = 0 (device in active mode) and vxxx_force_sleep = 1 (device in sleep mode, but no priority level on this bit) is forbidden.

If the master clock is used in high power mode when switching to sleep mode, the following features are not available:

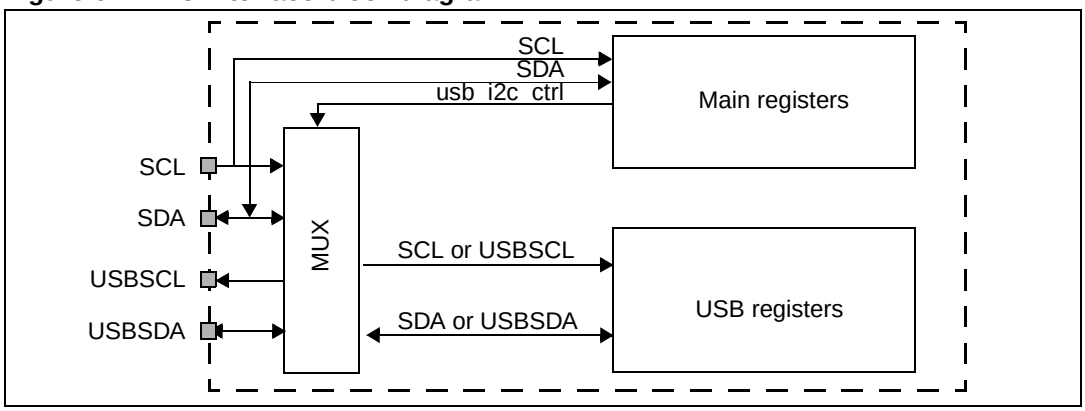
- Bit 1 (vcore_sleep) and bit 2 (vio_vmem_sleep) in power control register address 9 must be at high level
  (VIO_VMEM and VCORE cannot remain in high power mode)
- USB charge pump is not available in sleep mode: bit 5 in USB control register address 07h must be set

4.2.4 I2C Interface

The device supports two I2C bus interfaces. One main interface (SDA,SCL) controls power management and all programmable functions, the second interface (USBSDA, USBSCL) is dedicated to USB control. STw4811 allows to work with only the main I2C interface to control all the functions, including the USB, via 'usb_i2c_ctrl' bit of *power control* register (*Table 23*). I2C interface is used to read status information from inside the device.

Flags, interrupt and *write* registers are used to configure the device functions (threshold, clock division, output voltage, etc....). By default, the main I2C interface (SCL,SDA) controls the main registers and USB I2C interface (USBSCL, USBSDA) controls *USB* registers.

Figure 6. I2C interface block diagram



Both I2C are configured as slave serial interface compatible with I2C registered trademark of Phillips Inc. (version 2.1).

I2C interface description

Note: When not using the USB I2C interface, the two pins USBSCL and USCSDA must be connected to the VIO voltage.

STw4811 I2C is a slave serial interface with a serial data line (SDA or USBSDA) and a serial clock line (SCL or USBSCL):

- SCL / USBSCL: input clock used to shift data
- SDA / USBSDA: input/output bidirectional data transfers

It is composed of:

- One filter to reject spikes on the bus data line and preserve data integrity
- Bidirectional data transfers up to 400kbit/s (fast mode) via SDA or USBSDA signal

The SDA or USBSDA signal contains the input/output control and data signals that are shifted in the device, MSB first. The first bit must be high (START) followed by the Device ID (7 bits) and Read/Write bit control (1 indicates read access, a logical 0 indicates a write access).

- Device ID in write mode: 5Ah (01011010)
- Device ID in read mode: 5Bh (01011011)

Then STw4811 sends an acknowledge at the end of an 8 bit transfer. The next 8 bits correspond to the register address followed by another acknowledge. The 8-bit data field is sent last, followed by a last acknowledge.

Table 3. Device ID

b7	b6	b5	b4	b3	b2	b1	b0
AdrID6	AdrID5	AdrID4	AdrID3	AdrID2	AdrID1	AdrID0	R/W

Table 4. Register address

b7	b6	b5	b4	b3	b2	b1	b0
RegADR7	RegADR6	RegADR5	RegADR4	RegADR3	RegADR2	RegADR1	RegADR0

Table 5. Register data

b7	b6	b5	b4	b3	b2	b1	b0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

I2C interface modes

Figure 7. Control interface: I2C format

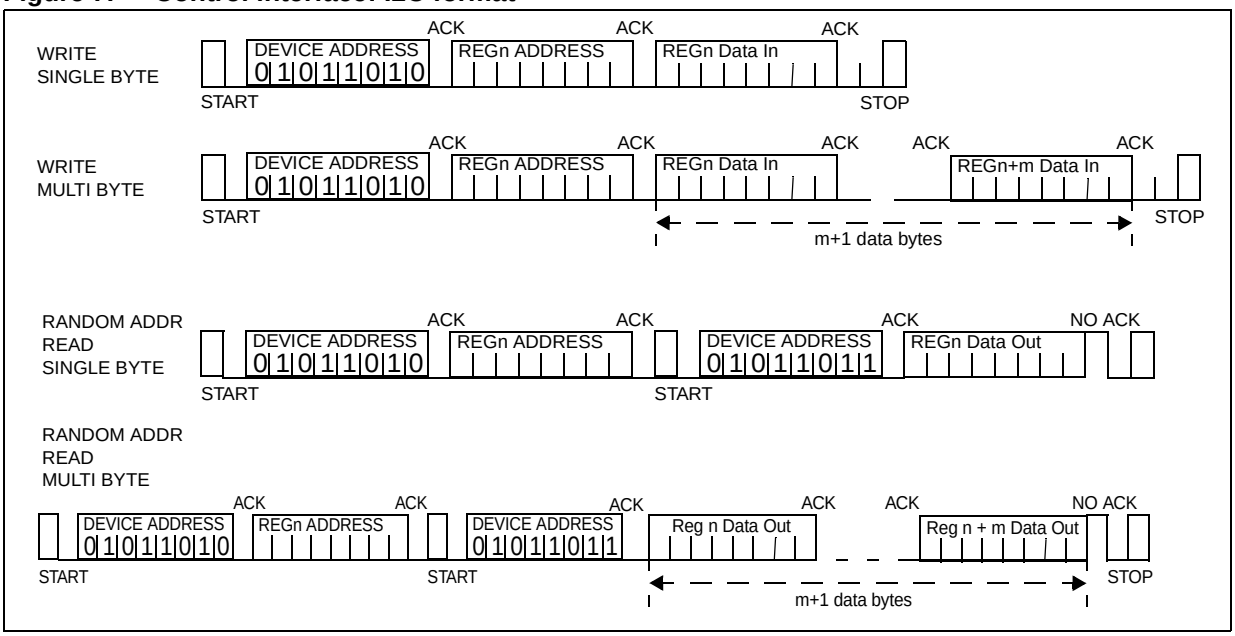
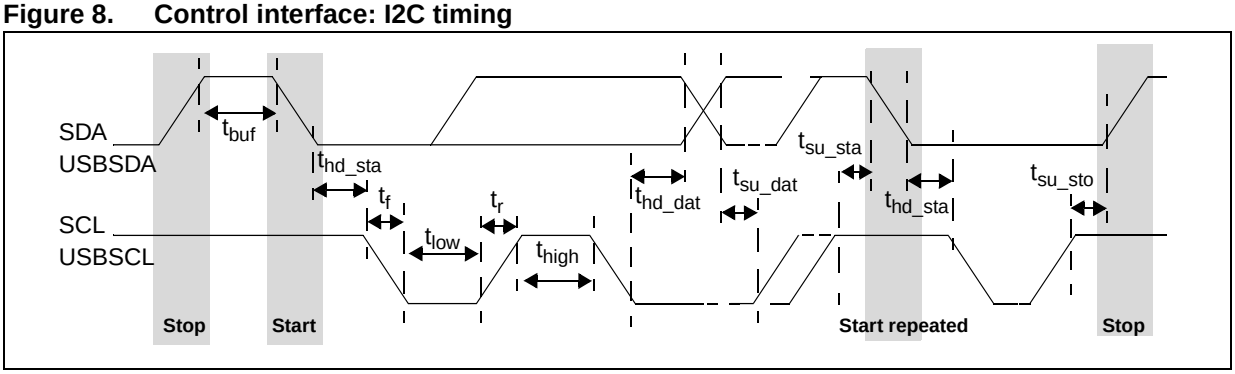


Figure 8. Control interface: I2C timing



4.2.5 Control registers

Control registers have the following functions:

- select level of regulation for multimedia processor supply
- control the USB interface
- control the SD/MMC/SDIO interface
- control the state machine

Table 6. Register general information

Address	Comment	I2C control
00h to 10h	*USB* registers (*Table 9* to *Table 17*)	USBSDA / USBSCL or SDA / SCL (1)
11h	*Configuration 1* register (*Table 18*)	SDA / SCL
12h to 1Dh	Reserved registers	
1Eh to 1Fh	*Power control* registers (*Table 19* to *Table 27*)	SDA / SCL
20h	*Configuration 2* register (*Table 28*)	SDA / SCL
21h	VCORE_sleep (*Table 29*)	SDA/SCL

1. Controlled by USB_I2C_CTRL bit of *power control* register (*Table 23*)

Register summary

Table 7. Register summary

Register	Addr.	7	6	5	4	3	2	1	0
Vendor ID	00h	1	0	0	0	0	0	1	1
	01h	0	0	0	0	0	1	0	0
Product ID	02h	0	0	0	1	0	0	0	1
	03h	0	1	0	0	0	0	0	0
USB control register 1	04h 05h	Not used	uart_en	oe_int_en	bdis_ acon_en	not used	dat_se0	suspend	speed
USB control register 2	06h 07h	vbus_ chrg	vbus_ dischrg	vbus_ drv	id_gnd	dn_ pulldown	dp_ pulldown	dn_ pullup	dp_ pullup
USB interrupt source	08h	cr_int	bdis_ acon	id_float	dn_hi	id_gnd_ forced	dp_hi	sess_vld	vbus_vld
USB interrupt latch	0Ah 0Bh	cr_int	bdis_ acon	id_float	dn_hi	id_gnd_ forced	dp_hi	sess_vld	vbus_vld
USB interrupt mask false	0Ch 0Dh	cr_int	bdis_ acon	id_float	dn_hi	id_gnd_ forced	dp_hi	sess_vld	vbus_vld
USB interrupt mask true	0Eh 0Fh	cr_int	bdis_ acon	id_float	dn_hi	id_gnd_ forced	dp_hi	sess_vld	vbus_vld
USB EN	10h	Not used	B_sess_ end	Not used			th_ Bdevice	usb_en	not used
Configuration 1	11h	pdn_ vaux	it_warn	monitoring _vio_ vmem_ vcore	mmc_ls_ status	vmmc_sel[2:0]			pdn_ vmmc
Configuration 2	20h	not used		not used	gpo2	gpo1	mask_it_ wake_up	external_ vmmc	mask_ twarn
Vcore_Sleep	21h	not used			vcore_ available	vcore_sleep[3:0]			

Table 8. Power control register

Addr.	15	14	13	12	11	10	9	8
1Fh	Not used						reg address 2 bits	
Addr.	7	6	5	4	3	2	1	0
1 Eh	reg address 3 bits			data din/dout 4 bits				ena write

Registers controlled by I2C USB bus

The registers described in this chapter are controlled through the USB serial I2C interface, USBSCL and USBSDA balls.

These registers can also be controlled through the main I2C interface, SCL and SDA balls by setting to “1” ‘usb_i2c_ctrl’ bit in *power control* register (*Table 23*).

Table 9. USB register address

Address	Register	Type
00h - 01h	Vendor ID	R
02h - 03h	Product ID	R
04h set	USB control register 1	R/W
05h clearh	USB control register 1	R/W
06h set	USB control register 2	R/W
07h clearh	USB control register 2	R/W
08h	USB interrupt source	R
09h	Not used	
0Ah set	USB interrupt latch	R/W
0Bh clearh	USB interrupt latch	R/W
0Ch set	USB interrupt mask false	R/W
0Dh clearh	USB interrupt mask false	R/W
0Eh set	USB interrupt mask true	R/W
0Fh clearh	USB interrupt mask true	R/W
10h	USB_EN	R/W

Note: A bit of register 1 is set at “1” by writing a “1” at address 04h, is reset at “0” by writing a “1” at address 05h. This is also applicable for USB control register 2 (06h, 07h), USB interrupt register (0Ah,0Bh), USB interrupt mask false register (0Ch, 0Dh) and USB interrupt mask true register (0Eh, 0Fh). Writing “0” at any address has not effect on the content of any register.

Table 10. Vendor ID and Product ID: Read only

Name	Address	Register value
Vendor ID	00h	83h
Vendor ID	01h	04h
Product ID	02h	11h
	03h	40h

USB control register 1

Table 11. USB control register 1 (address = 04h set and 05h clearh)

7	6	5	4	3	2	1	0
Not used	uart_en	oe_int_en	bdis_ acon_en	not used	dat_se0	suspend	speed
-	R/W	R/W	R/W	-	R/W	R/W	R/W

Bits	Name	Value	Settings	Default
6	uart_en	0 1	Inactive UART logic buffers are enabled	0
5	oe_int_en	0 1	Inactive Allow to send interruption through USBOEn	0
4	bdis_acon_en	0 1	Inactive (default) Enable A-device to connect if B-device disconnect detected:	0
2	dat_se0	0 1	VP_VM USB mode DAT_SE0 USB mode	0
1	suspend	0 1	Inactive (default) Put transceiver in low power mode	0
0	speed	0 1	Set rise and fall times of transmit Low speed Full speed	0

USB control register 2

Table 12. USB control register 2 (address = 06h set and 07h clearh)

7	6	5	4	3	2	1	0
vbus_chrg	vbus_ dischrg	vbus_drv	id_gnd	dn_ pulldown	dp_ pulldown	dn_pullup	dp_pullup
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Value	Settings	Default
7	vbus_chrg	0 1	Inactive Charge VBUS through a resistor	0
6	vbus_dischrg	0 1	Inactive Discharge VBUS through a resistor to ground.	0
5	vbus_drv	0 1	Inactive Provide power to VBUS	0
4	id_gnd	0 1	Inactive Connect ID ball to ground	0
3	dn_pulldown	0 1	Inactive Connect DN pull-down	0
2	dp_pulldown	0 1	Inactive Connect DP pull-down	0
1	dn_pullup	0 1	Inactive Connect DN pull-up	0
0	dp_pullup	0 1	Inactive Connect DP pull-up	0

USB interrupt source register

Table 13. USB Interrupt source register (address = 08h)

7	6	5	4	3	2	1	0
cr_int	bdis_acon	id_float	dn_hi	id_gnd_ forced	dp_hi	sess_vld	vbus_vld
R	R	R	R	R	R	R	R

Bits	Name	Value	Settings	Default
7	cr_int	0 1	Inactive DP ball is above the carkit interrupt threshold	0
6	bdis_acon	0 1	Inactive Set when bdis_acon_en is set, and transceiver asserts dp_pullup after detecting B-device disconnect.	0
5	id_float	0 1	Inactive ID ball floating	0
4	dn_hi	0 1	Inactive DN ball is high	0
3	id_gnd_forced	0 1	Inactive ID ball grounded	0
2	dp_hi	0 1	Inactive DP asserted during SRP,	0
1	sess_vld	0 1	Session valid comparator threshold < 2V 2 V < Session valid comparator threshold	0
0	vbus_vld	0 1	A-device VBUS valid comparator threshold < 4.4V A-device VBUS valid comparator threshold > 4.4V	0

USB interrupt source register indicates the current state of the signals that can generate an interrupt.

USB latch register

Table 14. USB interrupt latch registers (address = 0Ah set and 0Bh clearh)

Register	7	6	5	4	3	2	1	0
Bit name	cr_int	bdis_ acon	id_float	dn_hi	id_gnd_ forced	dp_hi	sess_ vld	vbus_ vld
Default	0	0	0	0	0	0	0	0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

USB interrupt latch register indicates which source has generated an interrupt.

USB interrupt enable low register

Table 15. USB interrupt enable low register (address = 0Ch and 0Dh)

7	6	5	4	3	2	1	0
cr_int	bdis_acon	id_float	dn_hi	id_gnd_ forced	dp_hi	sess_vld	vbus_ vld
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

USB interrupt enable low register enables interrupts on transition from high to low.

USB interrupt enable high register

Table 16. USB interrupt enable high register (address = 0Eh and 0Fh)

7	6	5	4	3	2	1	0
cr_int	bdis_acon	id_float	dn_hi	id_gnd_ forced	dp_hi	sess_vld	vbus_vl d
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

USB interrupt enable high register enables interrupts on transition from low to high.

Interrupts

Table 13 indicates the signals that can generate interrupts. Any of the signals given in *Table 13* can generate an interrupt when the signal becomes either low or high. After an interrupt, the OTG controller is able to read each signal status as well as the bit that indicates whether or not that signal generated the interrupt.

A bit in the *interrupt latch register* is set when any of the following occurs:

- writing “1” to its set address causes the corresponding bit to be set.
- the corresponding bit in the *interrupt enable high* register is set, and the associated signal changes from low to high
- the corresponding bit in the *interrupt enable low* register is set, and the associated signal changes from high to low

The *interrupt latch* register is cleared by writing “1” to its clear address.

USB EN register

Table 17. USB EN register (address = 10h)

7	6	5	4	3	2	1	0
Not used	B_sess_ end	Not used			th_ Bdevice	usb_en	not used
-	R	-	-	-	R/W	R/W	-

Bits	Name	Value	Settings	Default
1	usb_en	0 1	Inactive Enable USB PHY	0
2	th_Bdevice	0 1	Threshold for vbus_valid = 4.4 V Threshold for vbus_valid = 3.87 V	0
6	B_sess_end	0 1	Vbus voltage is below B_session_end threshold (0.2 to 0.8 V) Vbus voltage is above B_session_end threshold (0.2 to 0.8 V)	0

Registers controlled by main I2C BUS

I2C controlled registers are controlled through the main serial I2C interface, SCL and SDA balls.

Configuration 1 register

Table 18. Configuration 1 register (11h)

7	6	5	4	3	2	1	0
pdn_vaux	it_warn	monitoring_vio_ vmem_vcore	mmc_ls_ status	vmmc_sel[2:0]			pdn_ vmmc
R/W	R(1)	R(1)	R/W	R/W			R/W

1. These bits are reset (0) after reading

Bits	Name	Value	Settings	Default
7	pdn_vaux	0 1	Inactive Enable LDO vaux	0(1)
6	it_warn	0 1	Below temperature threshold Above temperature threshold	0
5	monitoring_vio_ vmem_vcore	0 1	Outputs in the good range Outputs lower than expected on vio_vmem or vcore	0
4	mmc_ls_status	0 1	Level shifters ON, if ‘pdn_vmmc’ or ‘external_vmmc’ = 1 Level shifters High Impedance, if ‘pdn_vmmc’ or ‘external_vmmc’ =1	0
[3:1]	vmmc_sel[2:0]	000 001 010 011 100 101 110 111	1.8V selection 1.8V selection 2.85V selection 3V selection 1.85 V selection 2.6 V selection 2.7 V selection 3.3 V selection	000
0	pdn_vmmc	0 1	Inactive Enable SD/MMC/SDIO function.	0

1. In STw4811M, pdn_vaux = 0 is the default. In STw4811N, pdn_vaux = 1 is the default.

In Flash OTP two registers allow to program STw4811 energy management part.
These two registers are at addresses 1E and 1F and must be programmed with *1F* register first followed by *1E* register.

Power control register at address 1Eh

Table 19. Power control register - General information (address = 1Eh)

7	6	5	4	3	2	1	0
reg address 3 bits LSB's			data din/dout 4 bits				EN
R/W			R/W				R/W

Bits	Name	Value	Settings	Default
[7:5]	reg address 3 bits		See *Table 21* "Address" column (LSB's).	0
[4:1]	data din/ dout 4 bits		See *Table 21* control register	0
0	EN	0 1	Read enabled Write enabled	0

Power control register at address 1Fh

Table 20. Power control register - General information (address = 1Fh)

15	14	13	12	11	10	9	8
Not used						reg address 2 bits MSB's	
						R/W	

Bits	Name	Value	Settings	Default
[9:8]	reg address 2 bits MSB's		See *Table 21* "Address" column (MSB's).	0

Power control register mapping

Table 21. Power control register mapping

Address 1Fh						Address 1Eh										Comments
						reg address										
Not used						2 bits MSB's		3 bits LSB's			data din/dout 4 bits				EN	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						00h to 04h										Reserved
						05h to 0Ah					Setting					See *Table 22* to *Table 27*
						0Bh to 1E										Reserved

Caution: Only the latest value written in register at address 1E/1F can be read.

Power control register at address 05h

Table 22. Power control register at address 05h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used						0	0	1	0	1	vcore_sel [3:0]				EN

Bits	Name	Value	Settings	Default
[4:1]	vcore_sel [3:0]	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	= 1.00V = 1.05V = 1.10V = 1.15V = 1.20V = 1.22V = 1.24V = 1.26V (default) = 1.28V = 1.30V = 1.32V = 1.34V = 1.36V = 1.38V = 1.40V = 1.45V	0111

Power control register at address 06h

Table 23. Power control register at address 06h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used						0	0	1	1	0	vpll_sel [0]	vaux_sel <1:0>		usb_ i2c_ctrl	EN

Bits	Name	Value	Settings	Default
4	vpll_sel[1:0] on 06h and 07h address	00 01 10 11	= 1.05V = 1.2V = 1.3V = 1.8V	11
[3:2]	vaux_sel[1:0]	00 01 10 11	= 1.5V = 1.8V = 2.5V = 2.8V	00
1	usb_i2c_ctrl	0 1	USB I2C interface controls USB registers Main I2C interface controls USB registers	0

Power control register at address 07h

Table 24. Power control register at address 07h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used						0	0	1	1	1	en_vpll	not used	en_ vcore	vpll_sel [1]	EN

Bits	Name	Value	Settings	Default
4	en_vpll	0 1	Disabled / VPLL = OFF Enabled / VPLL = ON(1)	1
2	en_vcore	0 1	Disabled / VCORE = OFF Enabled / VCORE = ON(1)	1
1	vpll_sel[1]	-	See *Table 23*	-

1. No soft start feature at supply enabled after a disabled/enabled sequence

Power control register at address 08h

Table 25. Power control register at address 08h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used						0	1	0	0	0	en_clk squarer	en_ mo nitoring	en_ vana	not used	EN

Bits	Name	Value	Settings	Default
4	en_clock_squarer	0 1	Disabled ([0; vio_vmem] digital signal) Enabled (master clock input not in the range [0; vio_vmem])	0
3	en_monitoring	0 1	Disabled / MONITORING = OFF Enabled / VCORE & VIO_VMEM monitoring = ON	1
2	en_vana	0 1	Disabled / VANA = OFF Enabled / VANA = ON	1

Power control register at address 09h

Table 26. Power control register at address 09h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used						0	1	0	0	1	vaux_ sleep	not used	vio_ vmem_ sleep (1)	vcore_ sleep (1)	EN

1. Must be left at default value if the master clock is used.

Bits	Name	Value	Settings	Default
4	vaux_sleep	0 1	When PWREN is low: VAUX stays in high power mode VAUX goes in sleep mode	1
2	vio_vmem_sleep	0 1	When PWREN is low: VIO_VMEM stays in high power mode VIO_VMEM goes in sleep mode	1
1	vcore_sleep	0 1	When PWREN is low: VCORE stays in high power mode VCORE goes in sleep mode	1

Power control register at address 0Ah

Table 27. Power control register at address 0Ah

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used						0	1	0	1	0	vaux_ force_ sleep	not used	vio_ vmem_ force_ sleep	vcore_ force_ sleep	EN

Bits	Name	Value	Settings	Default
4	vaux_force_sleep	0 1	0: Vaux keeps the state controlled by Vaux_sleep and Pwren 1: VAUX goes in sleep mode (for any PWREN level)	0
2	vio_vmem_force_ sleep	0 1	0: VIO_VMEM keeps the state controlled by vio_vmem_sleep and Pwren 1: VIO_VMEM goes in sleep mode (for any PWREN level)	0
1	vcore_force_slee p	0 1	0: VCORE keeps the state controlled by vcore_sleep and Pwren 1: VCORE goes in sleep mode (for any PWREN level)	0

Configuration 2 register

Table 28. Configuration 2 register at address = 20h

7	6	5	4	3	2	1	0
Not used		Not used	gpo2	gpo1	mask_it_wake_up	external_vmmc	mask_twarn
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bits	Name	Value	Settings	Default
0	mask_twarn	0 1	Inactive Mask TWARN interruption (it_twarn bit) through VDDOK	0
1	external_vmmc	0 1	Internal LDO VMMC is used External VMMC is used	0
2	mask_it_wake_up	0 1	Inactive IT_WAKE_UP ball masked	0
3	gpo1	0 1	GPO1 in High impedance GPO1 at low level	0
4	gpo2	0 1	GPO2 in High impedance GPO2 at low level	0
5	not used	0 1	Not used	0

VCORE_sleep register

Table 29. VCORE_sleep register at address = 21h

Register	7	6	5	4	3	2	1	0
Bit name				vcore_ available	vcore_sleep[3:0]			
Type				R	R/W			

Bits	Name	Value	Settings	Default
[3:0]	vcore_sleep[3:0]	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	= 1.00V = 1.05V = 1.10V = 1.15V = 1.20V = 1.22V = 1.24V = 1.26V (default) = 1.28V = 1.30V = 1.32V = 1.34V = 1.36V = 1.38V = 1.40V = 1.45V	0111
4	vcore_available (1)	0 1	Inactive Reach the expected value when Vcore decreases or increases	0

1. read operation reset the value after status read operation from APE, functionality is described in *Section 4.3.7: Power supply monitoring*

4.2.6 IT generation

STw4811 has three interrupt balls:

IT_WAKE_UP: with only VBAT supply, no other supply available, when a USB cable is plugged this interrupt is activated to wake up the host or the modem, depends of application (open drain, active low).
By default this feature is available independently of PON level, it can be masked when PON = 1 by ‘mask_it_wake_up’ bit of *Configuration 2* register (see *Table 28*)

USBINTn: This interrupt ball is dedicated to USB protocol and sent to multimedia processor. Independently of PWREN ball state, this ball goes to low level if an USB interrupt source is detected. In sleep mode, PWREN = 0, an interrupt source is detected only if unmasked before PWREN goes to low level.

VDDOK: This ball has two functions:
- When high, it indicates that VIO_VMEM and VCORE output voltages are within the right range and that the device internal temperature is below the maximum allowed temperature.
- When low, it indicates that output regulators (VCORE or VIO_VMEM) are not regulated properly or PWREN = “0”, or that the temperature is above the allowed threshold (see *Thermal shut-down* section), ‘it_warm’ bit of *Configuration 1* register is the temperature interruption source (see *Table 18*).

4.2.7 Clock switching and control

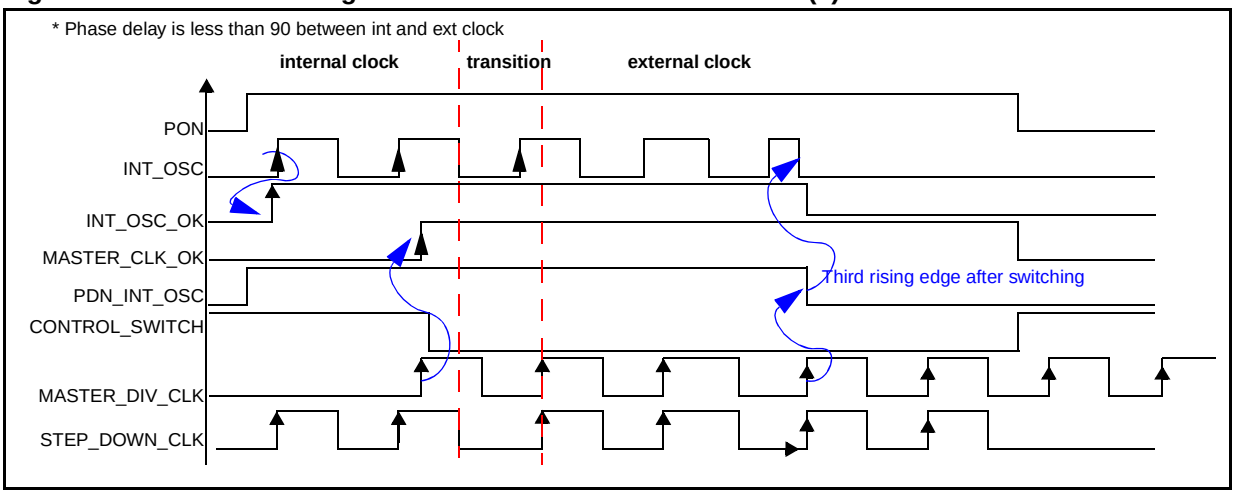
This block generates the clock used by the DC/DC converter (USB charge pump, step-down VIO_VMEM and step-down VCORE). STw4811 is able to sustain the master clock frequencies of 26 MHz, 19.2MHz and 13 MHz. If the clock is not detected the internal oscillator is automatically selected.

STw4811 allows customers to use the internal clock issued from the internal oscillator to switch the SMPS and charge pump; or, they can provide an external clock and connect it to the master clock input. If it is not necessary, it is recommended to run the device on the internal clock. Nevertheless, if the external clock is used, this clock has some constraints:

- the master-clk must be provided each time the device is in high power mode. When the device changes from sleep mode to high power mode the master-clk must be active before the device is in high power mode (the master-clk must be available and stable when PWREN pin goes to high level).
- the only way to stop the use of the master_clk, in HPM mode, is to restart the device with the OFF/ON sequence on PON (PON = 1 then 0 then 1)

Note: When present the Master clock should remain connected up to sleep mode.

Figure 9. Clock switching between master and internal clock (1)



4.3 Power management module

STw4811 includes several regulators that supply the multimedia processor and its peripherals. All regulators can work in different modes depending on the processor needs.

When the STw4811 is in ‘low current mode’”, the output current is reduced to save energy via the lower quiescent current. The nominal mode is called high power mode (HPM). The mode is selected by PWREN ball signal according to both multimedia processor and STw4811 state.

When PWREN = “0”, sleep mode is selected. HPM is selected as default when PWREN = “1”.

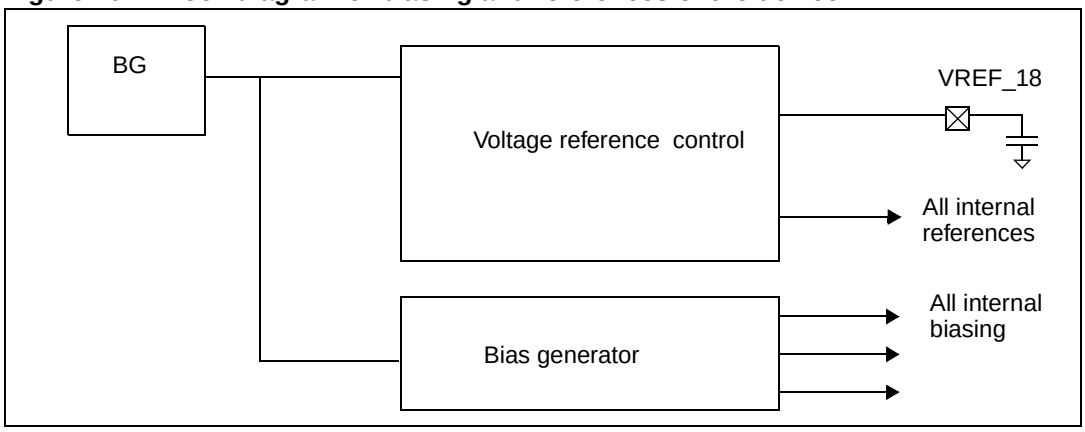
Except for VIO_VMEM, each supply can be powered down by a bit ‘pdn_(regulator name) or ‘en_(regulator name)’ (*Table 18*, *24* and *27*). In this mode, the regulator is switched off and only a leakage current is present (max. 1µA). VCORE, VAUX and VPLL output voltages are programmable, through main I2C interface, using the ‘(regulator”_sel[x:0])’ bits of the *power control* registers (*Table 22* to *Table 27*).

In addition, an output current limitation prevents high current delivery in case of output short circuit.

All multimedia processor power supplies have the same soft start to prevent leakage in the multimedia processor device during the start-up phase. There is an exception with VAUX which can be started independently.

4.3.1 Bandgap, biasing and references

Figure 10. Block diagram of biasing and references of the device



4.3.2 VCORE regulator: DC/DC STEP- DOWN regulator

This regulator drives the core of the multimedia processor. VCORE is a DC/DC step-down regulator that generates the regulated power supply with very high efficiency. The 16 voltage levels enable dynamic voltage and frequency scaling suitable for any supply voltage of CMOS process, they also follow the processor process roadmap. The regulated output voltage level is adjustable via the main I2C interface (SDA, SCL): in high power mode by the *power control* registers (*Table 22*), in sleep mode by *Vcore_sleep* register (*Table 29*).

The master clock (13, 19.2 or 26 MHz) is automatically detected, squared and divided to generate the switching clock of the SMPS. When this clock is not available, regulators run with the internal RC oscillator.

The DC/DC step-down regulator has the following main features;

- Programmable output voltage,
  - When changing the output voltage value (during a voltage scaling phase) the voltage step must be less than 100mV.
  - In high power mode, 16 levels from 1.0 V to 1.45 V through ‘vcore_sel [3:0]’ bits of *power control* register (*Table 22*)
  - In sleep mode,16 levels from 1.0 V to 1.45 V through ‘vcore_sleep [3:0]’ bits of *Vcore_sleep* register (*Table 29*).

Note: By default ‘vcore_sel’ = ‘vcore_sleep’

- 3 power domains:
  - ‘High power mode’ when multimedia processor is in run mode, 700 mA full load
  - ‘Low current mode’ when multimedia processor is in sleep mode, 5 mA current capability.
    Fast switching from low current to high power mode.
    The regulator is in ‘low current mode’ when multimedia processor is in sleep mode. PWREN signal indicates that the multimedia processor is about to switch to high power mode. VDDOK signal indicates to the multimedia processor that all supplies are in the specified range.

Note: The definition of sleep mode is given in section 4.2.3: Sleep mode.

  - ‘Power down mode’ or ‘standby mode’ when regulator is switched off, no consumption (‘en_vcore’ bit of *power control* register - *Table 24*)
- Soft start circuitry at start up, from power off to high power mode, when PON ball changes from “0” to “1”.

4.3.3 VIO_VMEM regulator: DC/DC step- down regulator

VIO_VMEM step-down regulator has the same structure than VCORE.

The VIO_VMEM regulator supplies the IOs of the multimedia processor and its peripherals.

This regulator can be used to supply the memories working with the multimedia processor, such as DDR-SDRAM. A switched mode power supply - voltage down converter is used to generate the 1.8 V regulated power supply with very high efficiency.

The master clock (13, 19.2 or 26 MHz) is automatically detected and divided to generate the SMPS switching clock. Master clock is squared when bit en_clock_squarer is enabled (*Table 25: Power control register at address 08h*). When this clock is not available, regulators can run with the internal RC oscillator.

Main features

- Fixed 1.8 V output voltage
- Two power domains:
  - ‘High power mode’ when multimedia processor is in run mode - 600 mA full load
  - ‘Low current mode’ when multimedia processor is in sleep mode, 5 mA current capability.
    Fast switching from low current to high power mode.
    The regulator is in ‘low current mode’ when multimedia processor is in sleep mode. PWREN signal indicates that the multimedia processor is about to switch to run mode. VDDOK signal indicates to the multimedia processor that all supplies are in the specified range.

Note: The definition of sleep mode is given in 4.2.3: Sleep mode section.

- Soft start circuitry at start up, from power off to high power mode, when PON ball changes from “0” to “1”.

4.3.4 VPLL

This LDO is dedicated to the multimedia processor PLL (1.05, 1.2, 1.3, 1.8 V) power supply with 10 mA max full load (*power control* registers - *Table 23* and *Table 24*).

Main features

- Programmable output voltage, ‘vpll_sel[1:0]’ bits of *power control* register - *Table 23* and *Table 24*)
- Two power domains:
  - ‘High power mode’ 10 mA full load
  - ‘Power down mode’ or ‘standby mode’ when regulators are switched off and there is no power consumption (‘en_vpll’ bit of *power control* register - *Table 24*)
- Soft start circuitry at start up, from power off to high power mode, when PON ball changes from “0” to “1”.

4.3.5 VANA

This LDO is dedicated to the multimedia processor analog function (2.5 V) power supply with 10 mA full load.

Main features:

- 2.5 V output voltage,
- Two power domains
  - ‘High power mode’ 10 mA full load
  - ‘Power down mode’ or ‘standby mode’ when regulators are switched off and there is no power consumption (‘en_vana’ bit of *power contro*l register - *Table 25*),

4.3.6 VAUX

This LDO is dedicated either to the multimedia processor input/output signals or to the auxiliary devices. Power supply values are 1.5, 1.8, 2.5, 2.8 V with 150 mA full load and 0.5 mA in sleep mode. In case of 1.5 V on the output, this LDO can be supplied by using VIO_VMEM DC/DC converter (1.8 V). One pad feed-back is used.

Main features:

- Programmable output voltage, 4 levels
  ('vaux_sel[1:0]' bits of *power control* register - *Table 23*)
- Three power domains:
  - 'High power mode' when multimedia processor is in run mode, 150 mA full load
  - 'Low current mode' when multimedia processor is in sleep mode, 0.5 mA current capability.
    Fast switching from low current to high power mode.

Note: The definition of sleep mode is given in 4.2.3: Sleep mode section.

  - 'Power down mode' or 'standby mode' when regulator is switched off, no power consumption ('pdn_vaux' bit of *configuration 1* register - *Table 18*).

4.3.7 Power supply monitoring

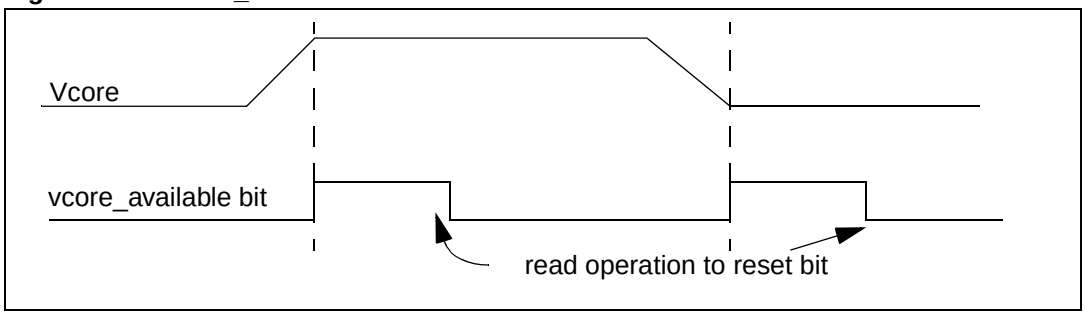
This block monitors the VCORE and VIO_VMEM output voltage. If VCORE or VIO_VMEM drop below the threshold, the multimedia processor is reset, through PORn output ball.

In high power mode, this feature can be disabled by setting 'en_monitoring' bit of *power control* register to "0" (*Table 25*).

When VCORE programmed value changes, 'vcore_available' bit (*Table 29*) gives the status of VCORE output supply value and informs the APE that the expected output voltage is reached, this bit is a read only bit and is reset after an APE read operation.

Figure 11 describes 'vcore_available' bit behavior.

Figure 11. 'vcore_available' bit behavior



4.3.8 Power supply domains

Table 30 lists the register bits that control STw4811 supply domains for each supply.

Table 30. Power supply domains

Supply name	Description	Supply domains		
		High power	Sleep	Power down
VCORE	STEP-DOWN	vcore_sel[3:0]	vcore_sleep[3:0] vcore_sleep vcore_force_sleep	en_vcore
VIO_VMEM	STEP-DOWN	-	vio_vmem_sleep vio_vmem_force_sleep	-
VPLL	LDO	vpll_sel[1:0]	-	en_vpll
VANA	LDO	-	-	en_vana
VAUX	LDO	vaux_sel[1:0]	vaux_sleep vaux_force_sleep	pdn_vaux
VMMC	LDO	vmmc_sel[2:0]	-	pdn_vmmc

Note: More details on VMMC supply are given in Section 4.5

4.3.9 Thermal shut-down

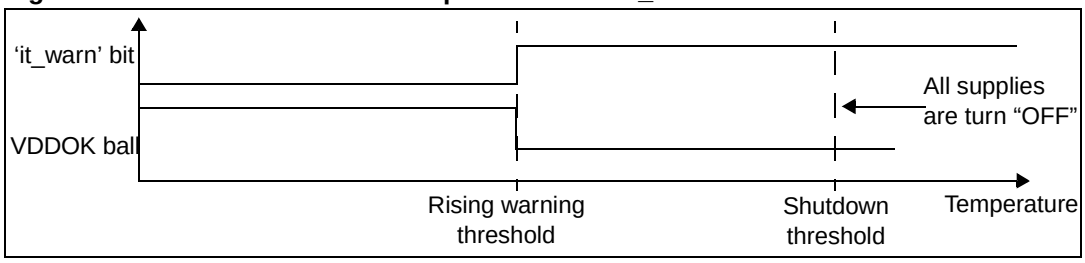
A thermal sensor is used to monitor the die temperature.

- As soon as the die temperature exceeds the thermal warning rising threshold, VDDOK ball goes to “0” and ‘it_warn’ bit is set to “1” (*configuration 1* register - *Table 18*). The IC turns back VDDOK ball to “1” and ‘it_warn’ bit to “0” when the device temperature drops below the thermal warning falling threshold of the thermal sensor.
- A second thermal detection level, thermal shutdown threshold, puts all STw4811 supplies OFF, the supplies goes back to ON state when the temperature is under the thermal shutdown threshold and after a new startup phase.

Table 31. Thermal threshold values

Description	Min	Typ	Max	Unit
Thermal warning threshold				
Rising threshold	134	140	149	°C
Falling threshold	117	123	131	°C
Thermal shutdown threshold				
Threshold	149	155	164	°C

Figure 12. Thermal threshold temperatures for 'it_warn' bit and VDDOK ball



4.4 USB OTG module

This transceiver complies with the USB specification;

- Universal serial bus specification Rev 2.0
- On the go supplement to the USB specification Rev 1.0-a
- Car kit interface specification (see: OTG transceiver specification Rev 0.92)

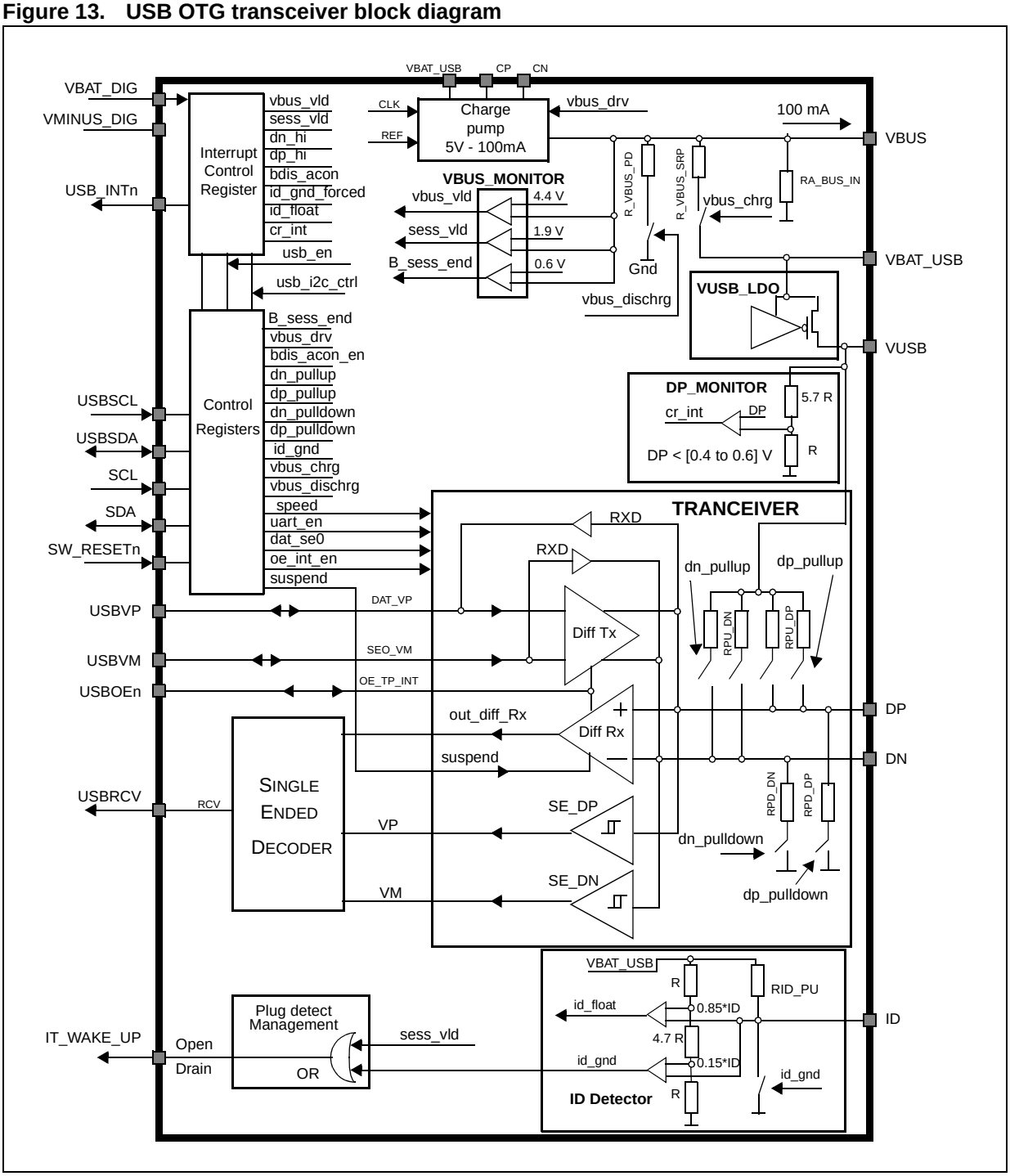
The USB OTG Transceiver has two modes: USB mode and UART mode. It includes:

- Full and low speed transceiver (12 Mbit/s and 1.5 Mbit/s data rate)
- Support data line and VBUS pulsing session request
- Contains Host Negotiation Protocol (HNP) command and *status* register
- Charge pump regulator (5 V at 100 mA) to supply VBUS line of the USB cable
- VBUS pull-up and pull-down resistors as defined by Session Request Protocol (SRP)
- VBUS threshold comparators
- VUSB LDO internal regulator which provides power supply for the bus driver and receiver.
- ID line detector and interrupt generator
- Dedicated I²C serial control interface

Note: The transceiver complies with USB specification if Vbat is greater than 3.2 V.

4.4.1 Block diagram

Figure 13. USB OTG transceiver block diagram



Interrupt management

IT_WAKE_UP: with only VBAT supply, no other supply available, when a USB cable is plugged this interrupt is activated to wake up the host or the modem, depends of application (open drain, active low).
By default this feature is available independently of PON level, it can be masked when PON = 1 by ‘mask_it_wake_up’ bit of *configuration 2* register (see *Table 28*)

USBINTn: This interrupt ball is dedicated to USB protocol and sent to multimedia processor. Independently of PWREN ball state, this ball goes to low level if an USB interrupt source is detected. In sleep mode, PWREN = 0, an interrupt source is detected only if unmasked before PWREN goes to low level.

VBUS monitoring

These comparators monitor the VBUS voltage. They detect the current status of the VBUS line:

- VBUS > 4.4 V means A-Device VBUS_Valid
- 0.8 V < VBUS < 2 V means A-Device Session Valid and 0.8 V < VBUS < 4 V means B-Device Session Valid. To be compatible with both Session Valid threshold, STw4811 threshold is equal to 1.9 V.
- VBUS < 0.8 V means B_Device Session End

These three bits generate an interrupt when active (see *USB interrupt* registers (*Table 13*)).

VUSB LDO: Internal regulator which provides power supply for the bus driver and receiver.

ID detector: This block detects the status of the ID line. It is capable of detecting three different states of line:

- ball is floating ‘id_float’ bit is high, Threshold detection is equal to 0.85 * Vbattery.
- ball is tied to ground ‘id_gnd_forced’ bit is high, Threshold detection is equal to 0.15 * Vbattery.
- ball is grounded via resistor, voltage is between 0.85 * Vbattery and 0.15 * Vbattery. ‘id_float’ and ‘id_gnd_forced’ bits are low.

This detection generates interrupts (see *USB interrupt* registers (*Table 13*)).

Transceiver: The driver can operate in different modes. It can act as a classical low-speed and full-speed differential driver, as two independent single-ended drivers or as a single-ended driver in UART mode. This block contains one differential receiver for the USB mode of operation and two single-ended receivers for USB signaling and UART mode.

DP monitor: This block is used to detect car kit peripheral, ‘cr_int’,0.6 V on DP (see *USB interrupt* registers (*Table 13*)).

Pull up and pull down resistors: Configurable integrated pull-up and pull-down resistor of data line and VBUS (see *USB control* register 2 (*Table 12*)).

4.4.2 Modes and operations

Power modes

The transceiver power modes are:

- active mode
- suspend mode
- power down mode

In suspend mode the differential transmitter and receiver are turned off to save power but the USB interface is still active (pull-up and pull-down on, VBUS on).
In power down mode, only the serial interface is active and the transceiver is able to detect SRP. In power down mode, ID ball can be grounded by 'id_gnd' bit of *USB control* register 2 (*Table 12*).

USB modes

The two transceiver modes are:

- DAT_SEO mode (dat_se0 = 1 in *USB control* register 1 - *Table 11*)
- VP_VM mode (dat_se0 = 0 in *USB control* register 1 - *Table 11*)

Data transmission The transceiver transmits USB data in the following conditions for *USB control register 1* (*Table 32*, *Table 33*):

uart_en=0; oe_int_en=0

and USBOEn ball at low level.

Table 32. Data transmission via USB control register 1 (DAT_SE0 mode) - Suspend = 0

USB mode (DAT_SE0)	Inputs		Outputs			Comments
	USBVP	USBVM	DP	DN	USBRCV	
1 (DAT_SE0 mode)	0	0	0	1	Not used	Single ended data (zero sent)
1 (DAT_SE0 mode)	1	0	1	0	Not used	Single ended data (1 sent)
1 (DAT_SE0 mode)	x	1	0	0	Not used	Force single ended zero
0 (VP_VM mode)	0	0	0	0	DIFF_RX	DAT_VP drives the level of DP SE0_VM drives the level of DN
0 (VP_VM mode)	1	0	1	0	DIFF_RX	
0 (VP_VM mode)	0	1	0	1	DIFF_RX	
0 (VP_VM mode)	1	1	1	1	DIFF_RX	

Table 33. Data transmission via USB control register 1 (DAT_SE0 mode) - Suspend = 1

USB mode (dat_se0)	Inputs		Outputs			Comments
	USBVP	USBVM	DP	DN	USBRCV	
1 (DAT_SE0 mode)	0	0	0	1	Not used	Single ended data (zero sent)
1 (DAT_SE0 mode)	1	0	1	0	Not used	Single ended data (1 sent)
1 (DAT_SE0 mode)	x	1	0	0	Not used	Force single ended zero
0 (VP_VM mode)	0	0	0	0	0 (off)	Driver are suspended
0 (VP_VM mode)	1	0	1	0	0 (off)	
0 (VP_VM mode)	0	1	0	1	0 (off)	
0 (VP_VM mode)	1	1	1	1	0 (off)	

If oe_int_en = 1 and suspend=1 (*USB control register 1* - *Table 11*), the USBOEn ball becomes an output used to generate an IT to multimedia processor.

Data reception The transceiver receives USB data in the following conditions:

uart_en = 0 (*USB control register 1*); oe_int_en = 1

and USBOEn at high level.

Table 34. Data receiver via USB control register 1

USB mode (dat_se0)	Suspend	Inputs		Outputs		
		DP	DN	USBVP	USBVM	USBRCV
1 (DAT_SE0 mode)	0	0	0	Diff rcv 1	1	Not used
1 (DAT_SE0 mode)	0	1	0	1	0	Not used
1 (DAT_SE0 mode)	0	0	1	0	0	Not used
1 (DAT_SE0 mode)	0	1	1	Diff rcv 1	0	Not used
1 (DAT_SE0 mode)	1	0	0	0	1	Not used
1 (DAT_SE0 mode)	1	1	0	1	0	Not used
1 (DAT_SE0 mode)	1	0	1	0	0	Not used
1 (DAT_SE0 mode)	1	1	1	1	0	Not used
0 (VP_VM mode)	0	0	0	0	0	diff rcv 1
0 (VP_VM mode)	0	1	0	1	0	1
0 (VP_VM mode)	0	0	1	0	1	0
0 (VP_VM mode)	0	1	1	1	1	diff rcv 1
0 (VP_VM mode)	1	0	0	0	0	Not used
0 (VP_VM mode)	1	1	0	1	0	Not used
0 (VP_VM mode)	1	0	1	0	1	Not used
0 (VP_VM mode)	1	1	1	1	1	Not used

UART mode

UART mode is entered by setting the ‘uart_en’ bit to 1 (*USB control register 1* - *Table 11*). The transceiver contains two digital logic level translators between the following balls:

- TXD signal: from USBVM ball to DN ball
- RXD signal: from DP ball to USBVP ball

When not in UART mode the level translators are disabled.

VBUS monitoring and control

The monitoring is made of three comparators that determine if the VBUS voltage is at a valid level for operation:

- VBUS VALID: It corresponds to the minimum level on VBUS. Any voltage on VBUS below the threshold is considered to be a fault. During power-up, it is expected that this comparator output is ignored.
- VBUS SESSION VALID: This threshold is necessary for session request protocol to detect the VBUS pulsing.
- VBUS SESSION END: Session is ended. In this USB block, a B-device Session End threshold is defined within the range [0.2; 0.8] V. The reason for a low 0.2 V limit is that the leakage current could charge the VBUS up to 0.2 V (maximum).

When the A-device (default master) is power supplied and does not supply VBUS, it presents an input impedance RA_BUS_IN on VBUS of no more than 100 kΩ. If the A-device responds to the VBUS pulsing method of SRP, then the input impedance RA_BUS_IN may not be lower than 40 kΩ.

When the A-device supplies power, the rise time TA_VBUS_RISE on VBUS to go from 0 to 4.4 V is less than 100 ms when driving 100 mA and with an external load capacitance of 10 µF (in addition to VBUS decoupling capacitance). If VBUS does not reach this voltage within TA_VBUS_RISE maximum time, it indicates that the B-device is drawing more current that the A-device is capable of providing and an over-current condition exists. In this case, the A-device turns VBUS off and terminates the session.

VBUS capacitance

A dual-role device must have a VBUS capacitance CDRD_VBUS value comprised between 1 µF and 6.5 µF (see charge pump specification). The limit on the decoupling capacitance allows a B-device to differentiate between a powered-down dual-role device and a powered-down standard host. The capacitance on a host is higher than 96 µF.

Data line pull-down resistance

The two bits of *USB control* register, dp_pulldown and dn_pulldown (*Table 12*) are used to connect/disconnect the pull-down resistors.

When an A-device is idle or acting as host, it activates the pull-down resistors RPD on both DP and DN lines.

When an A-device is acting as peripheral, it disables RPD on DP, not DN.

The A-device can disable both pull-down resistors during the interval of a packet transmission when acting as either host or peripheral.

When the line is not used, the pull-down is activated and the maximum level on this ball should not exceed 0.342 V.

Data line pull-up resistance

The two bits of *USB control* register dp_pullup and dn_pullup (*Table 12*) are used to connect/disconnect pull-up resistors.

Full-speed and low-speed devices are differentiated by the position of the pull-up resistor from the peripheral device. A pull-up resistor is connected to DP line for a full-speed device and a pull-up resistor is connected to DN line for a low-speed device. The pull-up resistor value is in the range of 900 Ω to 1600 Ω when the bus is idle and 1425 Ω to 3100 Ω when the upstream device is transmitting.

Session Request Protocol (SRP)

To save power, the OTG supplement allows an A-device to leave the VBUS turned off when the bus is not being used. If the B-device wants to use the bus when VBUS is turned off, then it requires the A-device to supply power on VBUS using the Session Request Protocol (SRP).

- Initial conditions

The B-device does not attempt to start a new session until it has determined if the A-device has detected the end of the previous session. The B-device must ensure that VBUS is below VBUS_SESSION_END before requesting a new session.

Additionally, the B-device switches a pull-down resistor (R_VBUS_PD) from VBUS to ground in order to quicken the discharge process as long as the B-device does not draw more than 8 mA from VBUS. R_VBUS_PD is activated by bit ‘vbus_dischrg’ of *USB control register 2*, (*Table 12*).

When the B-device detects that VBUS is below the VBUS_SESSION_END and that both DP and DN have been low (SEO) for at least 2 ms, then any previous session on the A-device is over and a new session can start.

- Data-line pulsing

To indicate a request for a new session using the data line pulsing, the B-device turns on the DP pull-up resistor for 5 ms to 10 ms (only at full speed, no DN pulsing). The DP pull-up resistor is connected to VUSB (regulator output voltage). Timing is controlled by the USB digital control.

- VBUS pulsing

To indicate a request for a new session using the VBUS pulsing method, the B-device waits for the initial conditions and then drives VBUS. VBUS is driven for a long enough period for a capacitance on VBUS that is smaller than 2x6.5 µF to be charged to 2.1 V while a capacitance on VBUS higher than 97 µF is not charged above 2.0 V. In this USB block, the VBUS_SESSION_VALID threshold is used to determine if an A-device is DRD (dual role device) or a standard host.

The B-device VBUS pulsing block is designed so that the maximum drawn current does not exceed 8 mA. In this USB block, the pull-up is 600 Ω +/- 30%.

If a B-device is attached to a standard device, the pull-up must be disconnected after the defined timing to prevent damage of standard hosts not designed to withstand a voltage externally applied to VBUS.

- Session Request Protocol (SRP)

If the B-device is in correct condition to start a new session, it first performs data line pulsing, followed by VBUS pulsing. When VBUS next crosses the SESSION VALID threshold, the B- device considers a session to be in progress and asserts the DP or DN data line within 100 ms. After SRP initialization, the B- device is set up to wait for at least 5 seconds for the A-device to respond before informing the user that the consumption attempt has failed.

- Host Negotiation Protocol (HNP)

At the start of a session, the A-device has the role of host as default. During a session, the host role can be transferred back and forth between the A-device and the B-device any number of times using the Host Negotiation Protocol (HNP). The sequence of events for this exchange of host role is described in the “On the Go Supplement to the USB 2.0 Specification” (rev 1.0) as follow:

  – The A-device puts the bus in the suspend state
  – The B-device simulates a disconnect by de-asserting its DP pull-up
  – The A-device detects SE0 on the bus and asserts its DP pull-up
  – The B-device detects that DP line is high and takes the role of the host.

ID detector

In either active or suspended power mode, the ID detector detects the condition of the ID line and differentiates between the following three conditions:

- ID ball floating: (e.g. with USB B-device connected)
- ID ball shorted to ground: (e.g. with USB A-device connected)
- ID ball connected to ground through resistor RACC_ID: (e.g.with an accessory).

The transceiver pulls the ID ball to VID_HI (VBAT) through a resistance of RID_PU when an accessory is plugged in. In this case, the ID ball is externally connected to ground via Racc_ID resistor.

Two comparators are used to detect the ID voltage: VID_GND and VID_FLOAT (*Figure 13*).

The ID detector also has a switch that can be used to ground the ID ball. This switch is controlled by ‘id_gnd bit’ of *USB control register 2* (*Table 12*); This pull-down is used for CEA_KARKIT purposes.

Car kit interrupt detector

The transceiver is able to detect when the DP line is below the car kit interrupt threshold ‘cr_int’, (see *USB interrupt* register in *Table 13* and refer to OTG specifications, Rev 0.92, §2.7, p13).

Charge pump

From VBAT_USB, the charge pump supplies VBUS, ‘vbus_drv’ bit of *USB control register 2* (*Table 12*) is used to enable/disable the charge pump.

If VBUS is “ON” before going to sleep mode, it remains “ON” in sleep mode.

LDO USB

From VBAT_USB, a LDO provides VUSB supply, ‘usb_en’ bit of *USB_EN* register (*Table 17*) is used to enable/disable the VUSB LDO and the transceiver.

4.4.3 USB enable control

STw4811 OFF

In this state: PON ball = 0

In this state, the overall system is able to detect USB connection through IT_WAKE_UP ball and with VBUS session valid comparator and ID detection ON.

IT_WAKE_UP ball is activated (low level if tied by an external Pull Up resistor to VIO or VBAT) in either of the two following cases:

- When a mini A connector cable is connected and ID goes low
- When activity on VBUS, that is a mini B is connected and is able to communicate. This mode is used to wake-up the platform. In this configuration, USBINTn ball is not enabled and IT_WAKE_UP ball cannot be masked by ‘mask_it_wake_up’ bit (*Table 28*).

STw4811 ON, USB driver not enabled

In this state: PON = 1

If ‘mask_it_wake_up’ bit is set to “0”, IT_WAKE_UP ball has the same behavior as above (PON = 0) and turns ON the transceiver, ‘usb_en’ bit set to “1” (*Table 17*).
If ‘mask_it_wake_up’ is set to “1”, IT_WAKE_UP ball feature is disabled and always stay at level “1” if tied by an external pull up resistor to VIO or VBAT and the transceiver is not turn ON.

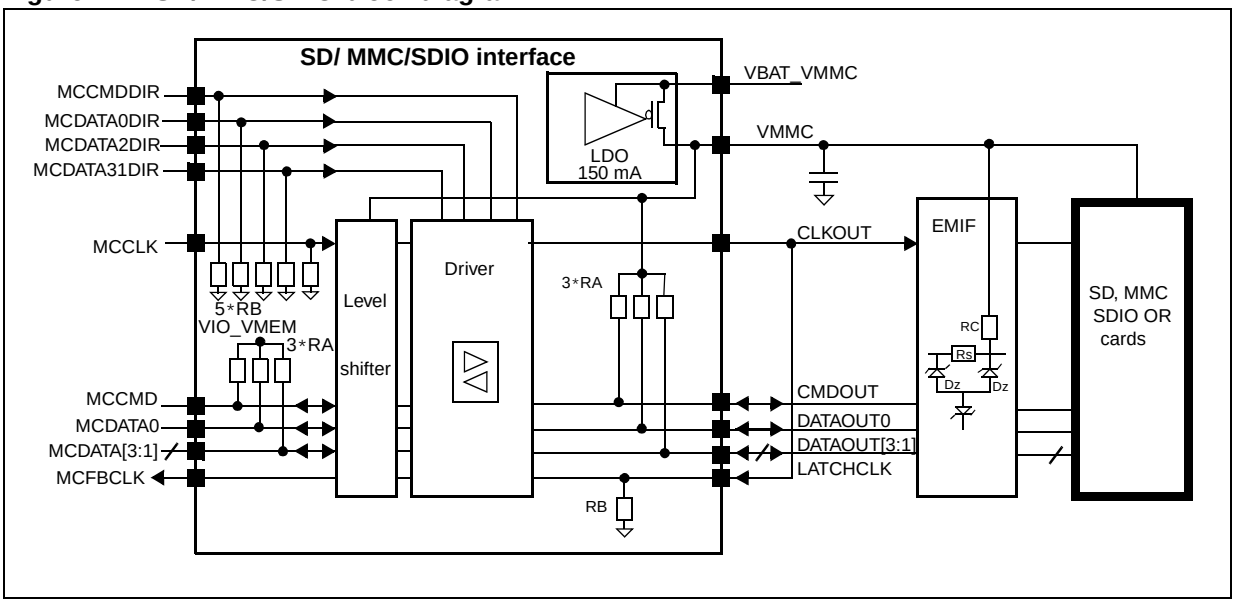
In sleep mode and in HIGH POWER mode, USBINTn ball is now enabled.

If the USB cable is already connected while STw4811 is starting, the USB driver will be enabled when power management is ready.

- Wake-up USB driver conditions
  - A plug-in on a mini A-device and active ID detector
  - B device is connected and ready to start data transfer, VBUS is driven high (session valid high)
  - Activity on *USB* registers (00h to 0Fh - *Table 9* to *Table 16*). Multimedia processor ready to wake-up and set-up USB PHY.
  - Possibility to force PHY high (enable) when writing ‘usb_en’ = 1 in USB EN register (*Table 17*)
- Set condition: one among the following possibilities
  - External it_wake_up =0
  - usb_en = 1 by writing to I2C USB interface
  - Access to any other *USB* register (00h to 0Fh)
- Power down USB driver conditions in order to set the USB driver to power down mode:
  - it_wake_up = 1, and only then
  - Set ‘usb_en’ bit of USB EN register (*Table 17*) to “0”

4.5 SD/MMC/SDIO module

Figure 14. SD/MMC/SDIO block diagram



4.5.1 SD/MMC/SDIO LDO supply

The Vmmc LDO is supplied via the input Vbat_Vmmc. According to the protection diode design, the voltage on this input pin Vbat_Vmmc must be always higher or equal to the battery voltage.

Vbat_Vmmc >= Vbat

By programming ‘vmmc_sel[2:0] bits of *configuration 1* register (*Table 18*), this LDO provides the power supply (1.8 V, 1.85 V, 2.6 V, 2.7 V, 2.85 V, 3 V, 3.3 V) with a 150 mA current compliance for any of the following peripherals.

- SD card
- MMC card
- SDIO card

If an application does not request to use the level shifter feature, this LDO can be used to supply an other peripheral, in this case, to reduce the internal current consumption due to level shifter it is recommended to set to “1” ‘mmc_ls_status’ bit of *configuration 1* register (*Table 18*).

If an application, like HDD, requests more than 150 mA current supply and the use of the internal level shifters, internal LDO must be disabled.
The application will be supplied by an external LDO and internal level shifter will be directly supplied by the external LDO.
In this configuration, ‘pdn_vmmc’ bit is set to “0”, ‘mmc_ls_status’ is set to “0” (*Table 18*) and ‘external_vmmc’ bit is set to “1” (*Table 28*).

4.5.2 Level shifters

Signal shifting cards voltage level value is automatically done by the multimedia processor system. Following a card detection, the multimedia processor starts the SD/MMC/SDIO application by writing in the *configuration 1* register (*Table 18*) to program LDO VMMC output supply and then starts the protocol initialization.

The module includes:

- Five bidirectional level shifter channels compatible with 1.8 V, 1.85 V, 2.6 V, 2.7 V, 2.85 V, 3.0 V, 3.3 V
- Two unidirectional lines for clock: multimedia processor to card and feedback clock to multimedia processor for synchronization.
- Four control signals for channel direction. When direction balls (MCCMDDIR, MCDATA0DIR, MCDATA2DIR, MCDATA31DIR) are at low level, data is transmitted from Card to APE. When direction balls are at high level data is transmitted from APE to card.

When the level shifters are “ON”, the APE interface MCDATA[3:0] and the MCCMD balls have a 1.5 Mohm pull up resistor to VIO_VMEM.

It is possible to connect another card on the APE interface (1.8 V interface) for this:

- set to “1” ‘mmc_ls_status’ bits of *configuration 1* register (*Table 18*) with this configuration:
  - the APE interface MCDATA[3:0] and the MCCMD balls are put in high impedance and the pull up resistors are disconnected.
  - the card interface DATAOUT[3:0] and the CMDOUT balls are set to “1” with an internal 1.5 Mohm pull up resistor
  - the card clock, CLKOUT ball, is set to “0” and the APE feedback clock, MCFBCLK ball is configured in high impedance.

5 Electrical and timing characteristics

Otherwise specified typical parameters are defined for T = 25 °C / VBAT = 3.6 V.

5.1 Absolute maximum rating

Table 35. STw4811 absolute maximum ratings

Symbol	Description		Values	Units
	Maximum power supply		-0.5 to 7	V
Ta	Maximum operating ambient temperature		-30 to +85	°C
V_{ESD}	Electrostatic discharge model	Human body model(1)	-2 to +2	kV
		Charge device model(2)	-300 to +1000	V

1. HBM tests have been performed in compliance with JESD22-A114-B and ESD STM 5.1-2001.HBM
2. CDM tests have been performed in compliance with CDM ANSI-ESD STM 5.3.1-1999

5.2 Package dissipation

Table 36. Package dissipation

Symbol	Description	Min.	Typ.	Max.	Units
TFBGA 84 6x6x1.2mm 0.5mm ball pitch					
RTH_{J-A}	Thermal resistance junction to ambient		70		°C/W
VFBGA84 4.6x4.6x1.0mm 0.4mm ball pitch					
RTH_{J-A}	Thermal resistance junction to ambient		76		°C/W

5.3 Power supply

Note: STw4811 has different ways to go in sleep mode.

The different possibilities for VCORE, VIO_VMEM and VAUX to be programmed to sleep mode are given in *Table 26* and *Table 27*.

Taking in account the bit programming from *Table 26* and *Table 27*, sleep mode is summarized with the following formula:

SLEEP = (Vxxx_SLEEP x $\overline{PWREN}$) + (Vxxx_FORCE_SLEEP) = 1
(Vxx = VCORE or VIO_VMEM or VAUX)

Note: The configuration Vxxx_SLEEP = 0 (device in active mode) and Vxxx_FORCE_SLEEP = 1 (device in sleep mode, but no priority level on this bit) is forbidden.

In all the following tables:

- "High power mode" is defined as "SLEEP = '0'"
- "Sleep mode" is defined as "SLEEP = '1'"

Use *Table 27* to refer to each Vxxx supply (VCORE or VIO_VMEM or VAUX).

5.3.1 Operating conditions

Table 37. Operating conditions (temperature range: -30 to +85 °C)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
V_{BAT}	Power supply		2.7		4.8	V
I_{QSLEEP}	Quiescent current	Sleep mode V_{BAT} = 3.6 V		140		µA
I_{QSTDBY}		OFF mode V_{BAT} = 3.6 V			4	µA

5.3.2 VREF18

Table 38. VREF18

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
V_{BAT}	Supply voltage		2.7		4.8	V
V_{REF_18}	Output voltage		1.78	1.8	1.84	V
PSRR	Power supply rejection ratio	Vpp = 0.3 V f ≤ 100 kHz		60		dB
	Noise	100 Hz ≤ f ≤ 100 kHz		30		µV
t_S	Settling time			7.77	9.46	ms

5.3.3 VCORE DC/DC step-down converter

Table 39. VCORE DC/DC step-down converter

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
VCORE regulator in high power mode (SLEEP = 0) unless otherwise specified, VCORE = 1.26V						
V_{BAT}	Input power supply	Battery voltage	2.7	3.6	4.8	V
V_{RIPPLE}	Output voltage ripple			6		mVpp
V_{OUT}	Programmable output voltage	'vcore_sel'[3:0] 1111 1110 1101 1100 1011 1010 1001 1000 0111 (default) 0110 0101 0100 0011 0010 0001 0000	 -3.7% -4.25% -5%	 1.45 1.40 1.38 1.36 1.34 1.32 1.30 1.28 1.26 1.24 1.22 1.20 1.15 1.10 1.05 1.00	 +3.7% +4.25% +5%	V
I_{OUT}	Output current				700	mA
P_{EFF}	Power efficiency	V_{BAT} = 3.6 V I_{OUT} = 200 mA		86		%
L_{IR}	Line regulation	V_{BAT}: [2.7; 4.8]V			10	mV
L_{DR}(1)	Load regulation	I_{OUT}: [0.1; 700] mA			10	mV
I_{SHORT}	Short circuit current limitation		0.9	1.2	1.4	A
I_Q	Quiescent current	I_{OUT} = 0 mA		130	200	µA
I_{LKG}	Power-down current	'en_vcore' = 0			1	µA
PSRR(1)	Power supply rejection	Vpp = 0.3 V [0; 20] kHz	40			dB
L_{IRT}	Transient line regulation	ΔV_{BAT} = 300 mV $t_R = t_F$ = 10 µs		7		mV
L_{DRT}	Transient load regulation	I_{OUT} = [1; 700] mA $t_R = t_F$ = 100 ns		70		mV

Table 39. VCORE DC/DC step-down converter (continued)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
VCORE regulator in sleep mode (SLEEP= '1')						
V_{BAT}	Input power supply	Battery voltage	2.7	3.6	4.8	V
V_{RIPPLE}	VCORE output voltage ripple			6		mVpp
L_{IR}	Line regulation	V_{BAT}: [2.7; 4.8]V			10	mV
L_{DR}	Load regulation	I_{OUT}: [0.1; 5] mA			10	mV
I_{OUT}	VCORE output current				5	mA
P_{EFF}	Power efficiency	V_{BAT}= 3.6 V I_{OUT}: [0.1; 5] mA		85		%
I_Q	Quiescent current	I_{OUT} = 0 mA		20	30	µA
L_{IRT}	Transient line regulation	ΔV_{BAT}= 300 mV $t_R = t_F$ = 10 µs		7		mV

1. Guaranteed by design

5.3.4 VIO_VMEM DC/DC step-down converter

Table 40. VIO_VMEM DC/DC step-down converter

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
VIO_VMEM regulator in high power mode (SLEEP = '0')						
V_{BAT}	Input power supply	Battery voltage	2.7	3.6	4.8	V
V_{OUT}	Output voltage (1)		-3%	1.8	+3%	V
V_{RIPPLE}	Output ripple			6		mVpp
L_{IR}	Line regulation	V_{BAT}: [2.7; 4.8]V			10	mV
L_{DR}(2)	Load regulation	I_{OUT}: [0.1; 600] mA			10	mV
I_{OUT}	Output current				600	mA
P_{EFF}	Power efficiency	VBAT = 3.6 V, VIO = 1.8 V I_{OUT}= 200 mA		90		%
I_{SHORT}	Short circuit current limitation		0.9	1.2	1.4	A
I_Q	Quiescent current	I_{OUT} = 0 mA		130	250	µA
PSRR(2)	Power supply rejection	Vpp = 0.3 V [0; 20] kHz	40			dB
L_{IRT}	Transient line regulation	ΔV_{BAT} = 300 mV $t_R = t_F$ = 10 µs		7		mV
L_{DRT}	Transient load regulation	I_{OUT}= [1; 600] mA $t_R = t_F$ = 100 ns		70		mV

Table 40. VIO_VMEM DC/DC step-down converter (continued)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
VIO_VMEM regulator in sleep mode (SLEEP='1')						
V_{BAT}	Input power supply	Battery voltage	2.7	3.6	4.8	V
V_{RIPPLE}	Output ripple			10		mVpp
L_{IR}	Line regulation	V_{BAT}: [2.7; 4.8]V			10	mV
L_{DR}	Load regulation	I_{OUT}: [0.1; 5] mA			10	mV
I_{OUT}	Output current				5	mA
P_{EFF}	Power efficiency	V_{BAT} = 3.6 V I_{OUT} = [0.1; 5] mA		85		%
I_Q	Quiescent current	I_{OUT} = 0 mA			20	µA
L_{IRT}	Transient line regulation	ΔV_{BAT} = 300 mV $t_R = t_F$ = 10 µs		2		mV

1. Including output voltage temperature coefficient, DC line and load regulations, voltage reference accuracy, industrial manufacturing tolerances and ripple voltage due to switching
2. Guaranteed by design

5.3.5 LDO regulators

VPLL

Table 41. LDO regulators - VPLL

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
VPLL regulator in high power mode unless otherwise specified, VPLL = 1.8 V						
V_{BAT}	Input power supply	Battery voltage	2.7	3.6	4.8	V
V_{OUT}	Output voltage	'vpll_sel'[1:0] 11 (default) 10 01 00	-3%	 1.8 1.3 1.2 1.05	+3%	V
I_{OUT}	Output current			3.5	10	mA
I_{SHORT}	Short-circuit limitation		95	130	165	mA
I_Q	Quiescent current	I_{OUT} = 0 mA		30	40	µA
I_{LKG}	Power-down current	EN_VPLL = 0			1	µA
PSRR(1)	Power supply rejection	Vpp = 0.3 V f < 10 kHz 10 kHz < f <100 kHz	 55 45			 dB dB
L_{IR}	Line regulation	V_{BAT}: [2.7; 4.8]V			5	mV
L_{DR}	Load regulation	I_{OUT}: [0.1; 10] mA			10	mV
L_{IRT}	Transient line regulation	ΔV_{BAT} = 300 mV $t_R = t_F$ = 10 µs		1		mV
L_{DRT}	Transient load regulation	I_{OUT} = [0.1; 10] mA $t_R = t_F$ = 1 µs		1		mV
En(1)	Noise density	at 1 kHz BW = 100 Hz			250	$\frac{nV_{rms}}{\sqrt{Hz}}$

1. Guaranteed by design

VANA

Table 42. LDO regulators - VANA

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
VANA regulator in high power mode						
V_{BAT}	Input power supply	Battery voltage	2.7	3.6	4.8	V
V_{OUT}	Output voltage		-5%	2.5	+5%	V
I_{OUT}	Output current				10	mA
I_{SHORT}	Short-circuit limitation		39	51	64	mA
I_Q	Quiescent current	I_{OUT} = 0 mA			30	µA
I_{LKG}	Power-down current	EN_VANA = 0			1	µA
PSRR(1)	Power supply rejection	Vpp = 0.3 V f < 10 kHz	45			dB
L_{IR}	Line regulation	V_{BAT}: [2.7; 4.8] V			5	mV
L_{DR}	Load regulation	I_{OUT}: [0.1; 10] mA			5	mV
L_{IRT}	Transient line regulation	ΔV_{BAT} = 300 mV $t_R = t_F$ = 10 µs		2		mV
L_{DRT}	Transient load regulation	I_{OUT} = [0.1; 10] mA $t_R = t_F$ = 1 µs		15		mV

1. Guaranteed by design

VAUX

Table 43. LDO regulators - VAUX

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
VAUX regulator in high power mode (pdn_vaux = 1, SLEEP = 0)						
V_{BAT}	Input power supply	V_{OUT} = 1.5V	1.7		4.8	V
		V_{OUT} = 1.8/2.5 V	2.7	3.6	4.8	V
		V_{OUT} = 2.8 V	3	3.6	4.8	
V_{OUT}	Output voltage	'vaux_sel'[1:0] 00 (default) 01 10 11	-3%	 1.5 1.8 2.5 2.8	+3%	V
I_{OUT}	Output current				150	mA
I_{SHORT}	Short-circuit limitation		220		410	mA
I_Q	Quiescent current	I_{OUT} = 0 mA			30	µA

Table 43. LDO regulators - VAUX (continued)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
I_{LKG}	Power-down current	'pdn_vaux' = 0			1	µA
PSRR(1)	Power supply rejection	V_{OUT}=1.5 V Vpp = 0.3 V f < 10 kHz	40			dB
L_{IR}	Line regulation	V_{OUT}=1.5 V V_{BAT}: [2.7; 4.8]V			5	mV
L_{DR}(1)	Load regulation	V_{OUT}=1.5 V I_{OUT}= [0.1; 150] mA			10	mV
L_{IRT}	Transient line regulation	ΔV_{BAT} = 300 mV $t_R = t_F$ = 10 µs		2		mV
L_{DRT}	Transient load regulation	I_{OUT} = [10; 90%] mA $t_R = t_F$ = 1 µs		35		mV
t_S	Settling time				100	µs
VAUX regulator in sleep mode ('pdn_vaux'= 1, SLEEP='1')						
V_{BAT}	Input power supply	V_{OUT} = 1.5V VIO_VMEM supply	1.7		4.8	V
		V_{OUT} = 1.8/2.5 V	2.7	3.6	4.8	V
		V_{OUT} = 2.8 V	3	3.6	4.8	
I_{OUT}	Output current				500	µA
I_Q	Quiescent current	I_{OUT} = 0 mA			20	µA
PSRR(1)	Power supply rejection	V_{OUT}=1.5 V Vpp = 0.3 V f < 10 kHz	38			dB
L_{IR}	Line regulation	V_{OUT}=1.5 V V_{BAT}: [2.7; 4.8]V			5	mV
L_{DR}	Load regulation	V_{OUT}=1.5 V I_{OUT}= [10; 90%] µA			10	mV
L_{IRT}	Transient line regulation	ΔV_{BAT} = 300 mV $t_R = t_F$ = 10 µs		2		mV
L_{DRT}	Transient load regulation	I_{OUT} = [10; 90%] µA $t_R = t_F$ = 1 µs		35		mV

1. Guaranteed by design

5.3.6 Power supply monitoring

This block monitors the VCORE and VIO_VMEM output voltage. If VCORE or VIO_VMEM drops below the threshold, the multimedia processor is reset.

Table 44. Power supply monitoring

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Threshold						
T_{HCORE}(1)	Threshold VCORE		-3%	VCORE-150	+3%	mV
T_{HVIO}(1)	Threshold VIO_VMEM		-3%	1.65	+3%	V
Comparators						
V_{BAT}	Supply voltage		2.7	3.6	4.8	V
t_{RES}	Response time			100		ns
H_{YFALL}	Hysteresis (input voltage falling)			26		mV
H_{YRIS}	Hysteresis (input voltage rising)			+4		mV

1. Guaranteed by design

5.4 Digital specifications

5.4.1 CMOS input/output static characteristics: I2C interface

Table 45. CMOS input/output static characteristics: I²C interface

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
I²C interface(1)						
V_{IL}	Low level input voltage				0.3*V_{IO}	V
V_{IH}	High level input voltage		0.7*V_{IO}			V
I_{IL}	Low level input current		-1.0		1.0	µA
I_{IH}	High level input current		-1.0		1.0	µA
V_{OL}	Low level output voltage	IOL = 3mA (with open drain or open collector)			0.2*V_{IO}	V
V_{OH}	High level output voltage	IOL = 3mA (with open drain or open collector)	0.8*V_{IO}			V

1. Vio is for VIO_VMEM

5.4.2 CMOS input/output dynamic characteristics: I2C interface

Table 46. CMOS input/output dynamic characteristics: I²C interface

Symbol	Description	Min.	Typ.	Max.	Units
I²C interface (*Figure 8*)					
Fscl	Clock frequency			400	kHz
thigh	Clock pulse width high	600			ns
tlow	Clock pulse width low	1300			ns
tr	SDA, SCL, USBSDA, USBSCL rise time	20+0.1*Cb (1)		300	ns
tf	SDA, SCL, USBSDA, USBSCL fall time	20+0.1*Cb		300	ns
thd_sta	Start condition hold time	600			ns
tsu_sta	Start condition set up time	600			ns
thd_dat	Data input hold time	0			ns
tsu_dat	Data input set up time	100			ns
tsu_sto	Stop condition set up time	600			ns
tbuf	Bus free time	1300			ns
Cb	Capacitive load for each bus line			400	pF

1. Cb = total capacitance of one bus line in pF

5.4.3 CMOS input/output static characteristics: VIO level

USB and control I/Os

Table 47. VIO level: USB and control I/Os

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
SW_RESETn, VDDOK, PORN, PWREN, TCXO_EN, REQUEST_MC, CLK32K, CLK32K_IN, USBOEN, USBVP, USBVM, USBRCV, USBINTn, MASTER_CLK						
V_{IL} (1)	Low level input voltage				0.3*Vio	V
V_{IH}	High level input voltage		0.7*Vio			V
I_{IL}	Low level input current		-1.0		1.5	µA
I_{IH}	High level input current		-1.0		1.5	µA
C_{IN}	Input capacitance				10	pF
V_{OL}	Low level output voltage	IOL = 4 mA			0.2*Vio	V
V_{OH}	High level output voltage	IOL = 4 mA	0.8*Vio			V
t_{OF}	Output fall time	Capacitance 10pF			10	ns
t_{OR}	Output rise time	Capacitance 10pF			10	ns
$C_{I/O}$	Driving capability				100	pF

1. Vio for VIO_VMEM

MMC interface

Table 48. VIO level: MMC interface

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
MMC interface: MCCLK, MCFBCLK, MCCMDDIR, MCCMD, MCDATA2DIR, MCDAT2, MCDATA0DIR, MCDAT0, MCDAT31DIR, MCDAT3, MCDAT1						
V_{IL} (1)	Low level input voltage				0.3*Vio	V
V_{IH}	High level input voltage		0.7*Vio			V
I_{IL}	Low level input current		-1.0		1.5	µA
I_{IH}	High level input current		-1.0		1.5	µA
C_{IN}	Input capacitance				10	pF
V_{OL}	Low level output voltage	IOL = 15 mA			0.2*Vio	V
V_{OH}	High level output voltage	IOL = 15 mA	0.8*Vio			V
$C_{I/O}$	Driving capability at 52 MHz				30	pF

1. Vio for VIO_VMEM

5.4.4 CMOS input/output static characteristics: VBAT level

Table 49. CMOS input/output static characteristics: VBAT level

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
IT_WAKE_UP, PON, GPO1, GPO2						
V_{IL}	Low level input voltage	PON			0.3*Vbat	V
V_{IH}	High level input voltage	PON	0.7*Vbat			V
I_{IL}	Low level input current	PON	-1.0		1.5	µA
I_{IH}	High level input current	PON	-1.0		1.5	µA
C_{IN}	Input capacitance				10	pF
V_{OL}	Low level output voltage	IT_WAKE_UP, GPO1, GPO2 IOL = 2 mA			0.2*Vbat	V
V_{OH}	High level output voltage	IT_WAKE_UP, GPO1, GPO2 IOL = 2 mA	0.8*Vbat			V
t_{OF}	Output fall time	Capacitance 10pF			5	ns
t_{OR}	Output rise time	Capacitance 10pF			50	ns
$C_{I/O}$	Driving capability				100	pF

5.4.5 CMOS input/output static characteristics: VMMC level

Table 50. CMOS input/output static characteristics VMMC level

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
DATAOUT0, DATAOUT1, DATAOUT2, DATAOUT3, CMDOUT, LATCHCLK, CLKOUT						
V_{IL}	Low level input voltage				0.3*VMMC	
V_{IH}	High level input voltage		0.7*VMMC			
I_{IL}	Low level input current		-1.0		1.5	µA
I_{IH}	High level input current		-1.0		1.5	µA
C_{IN}	Input capacitance				10	pF
V_{OL}	Low level output voltage	I_{OL} = 25 mA			0.2*VMMC	
V_{OH}	High level output voltage	I_{OL} = 25 mA	0.8*VMMC			
$C_{I/O}$	Driving capability				40	pF

5.5 USB OTG transceiver

Table 51. USB OTG transceiver

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
UART mode						
t_R	Rise time	C_{LOAD}= [50;100] pF [10; 90] % of V_{OH}-V_{OL}			100	ns
t_F	Fall time	C_{LOAD}= [50;100] pF 10.....90% of V_{OH}-V_{OL}			100	ns
t_{PLH}	Drive propagation delay low => high	C_{LOAD}= [50;100] pF 50% of $\|V_{OH}$-$V_{OL}\|$			100	ns
t_{PHL}	Drive propagation delay high => low	C_{LOAD}= [50;100] pF 50% of $\|V_{OH}$-$V_{OL}\|$			100	ns
USB full speed mode (DP & DN signals)						
t_R	Rise time	USBVP & USBVM : - Trise & Tfall < 1 ns - Skew < 0.66 ns	4		20	ns
t_F	Fall time		4		20	ns
D_{RFM}	Differential rise an fall time matching		90		111	%
OS_{CV}	Output signal crossover voltage		1.3		2	V
P_{DEL}	Propagation delay				18	ns
USB low speed mode (DP & DN signals)						
t_R	Rise time		75		300	ns
t_F	Fall time		75		300	ns
D_{RFM}	Differential rise an fall time matching		80		125	%
OS_{CV}	Output signal crossover voltage		1.3		2	V
VBUS comparators						
V_{BAT}	Input power supply	Battery voltage	3.1	3.6	4.8	V
t_{RR}	Rising reacting time			1.7		µs
t_{FR}	Fall reacting time			2.1		µs

Table 51. USB OTG transceiver (continued)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Threshold VBUS monitoring						
V_{Aval}	VBUS valid		4.4	4.5	4.6	V
V_{th_dev}	Threshold device	'th_Bdevice' = 1	3.77	3.87	3.97	V
V_{Bses}	VBUS session valid		1.8		2	V
V_{Bsess_end}	B_session_end		0.2		0.8	V
VBUS						
$R_{A\_BUS\_IN}$			40		100	kΩ
$T_{A\_VBUS\_RISE}$		V_{BUS} = [0; 4.4] V I_{LOAD} = 100mA External cap 10µF			100	ms
Data line pull-down resistance						
R_{PD_DPDN}			14	19	25	kΩ
Data line pull-up resistance						
R_{PU_DP}		Bus idle Bus driven	900 1425	1200 2300	1600 3100	Ω
R_{PU_DN}		Bus idle Bus driven	900 1425	1200 2300	1600 3100	Ω
PULL-DOWN on VBUS						
R_{VBUS_PD}			650	925	1200	Ω
PULL-UP on VBUS						
R_{VBUS_SRP}			420	600	780	Ω
ID						
V_{ID_GND}	ID_GND comparator threshold	2.7 V < V_{BAT} < 4.8 V		0.15* V_{BAT}		V
V_{ID_HI} (V_{BAT})	Battery level		2.7	3.6	4.8	V
V_{ID_FLOAT}	ID_FLOAT comparator threshold			0.85* V_{BAT}		V
R_{PU_ID}			70	100	130	kΩ
R_{PD_ID}					10	kΩ
Carkit threshold detection						
c_{R_INT}	Carkit interrupt threshold		0.4		0.6	V

Table 51. USB OTG transceiver (continued)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Transceiver						
$V_{OH\_TXD\_DAT}$	TXD output high on DN	I_{SOURCE} = 500 µA	2.4		3.6	V
$V_{OL\_TXD\_DAT}$	TXD output low on DN	I_{SINK} = 2mA			0.4	V
$V_{IH\_RXD\_DAT}$	RXD input high on DP		2			V
$V_{IL\_RXD\_DAT}$	RXD input low on DP				0.8	V
Charge pump						
V_{BAT}	Input power supply	Battery voltage	VUSB+0.1	3.6	4.8	V
V_{BUS}	Output voltage	Current load up to 100 mA	4.75	5	5.25	V
t_S	Settling time	[0;4.8] V) Ext. load: 100 mA + External cap = 10µF		1.2		ms
IQ	Quiescent current	No Load		2.7		mA
VRipple	Amplitude output ripple on VBUS	Current load 8 mA Current load 100mA		25 40		mV mV
I_{OUT}	Output current				100	mA
Eff	Efficiency	V_{BAT} = 3.0V I_{OUT} =100mA VBAT= 3.6V. I_{OUT} = 8 mA.		85 60		% %
VUSB regulator						
V_{BAT}(1)	Input voltage	Battery voltage: V_{BAT} min = V_{OUT} + 0.1V	VUSB+0.1	3.6	5.5	V
V_{OUT}	Output voltage	V_{BAT} min= V_{OUT} + 0.1V	3.0	3.1	3.2	V
I_{SHORT}	Short circuit current limitation				320	mA
I_Q	Quiescent current	No load			70	µA
PSRR(2)	Power supply rejection	V_{BAT}= V_{OUT}+0.2V f < 20 kHz	45			dB
L_{IRT}	Transient line regulation	ΔV_{BAT} = 300 mV t_R = t_F = 10µs.		5		mV

Table 51. USB OTG transceiver (continued)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
t_S	Settling time OFF->ON	I_{OUT} = 0mA		25		µs
t_D	Discharge time ON>OFF	I_{OUT} = 0mA		400		µs

1. From 4.8 V to 5.5 V, charge pump is “Off” and no OTG feature is provided
2. Guaranteed by design

5.6 SD/MMC/SDIO card interface

Table 52. SD/MMC/SDIO card interface

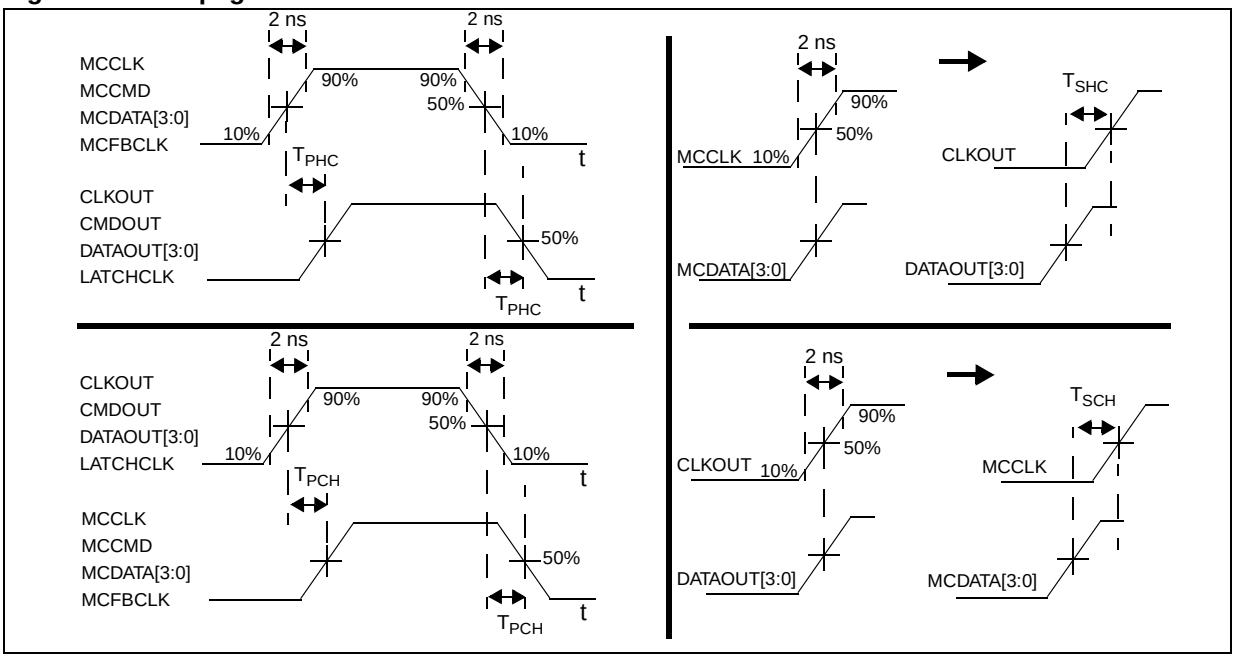
Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
VMMC regulator specifications (’pdn_vmmc’ = 1)						
V_{IN}	Input voltage	V_{OUT} = 3.3 V V_{OUT} = 3 V V_{OUT} = 2.85 V V_{OUT} = 2.7 V V_{OUT} = 2.6 V V_{OUT} = 1.8/1.85 V	3.55 3.25 3.1 2.95 2.85 2.7	3.6	5.5	V
V_{OUT}	Output voltage		-3%	3.3 3 2.85 2.7 2.6 1.85 1.8	+3%	V
I_{OUT}	Output current				150	mA
I_{SHORT}	Short circuit current limitation		240	360	600	mA
IQ	Quiescent current	I_{OUT} = 0 mA			30	µA
I_{LKG}	Power-down current	’pdn_vmmc’ = 0			1	µA
PSRR(1)	Power supply rejection	I_{OUT} = 150 mA Vpp = 0.3 V f < 20 kHz	45			dB
L_{IR}(1)	Line regulation	V_{OUT}=2.85 V V_{BAT}: [3.1; 4.8]V			5	mV
L_{DR}(1)	Load regulation	V_{OUT}=2.85 V I_{OUT}= [1; 150] mA			10	mV
L_{IRT}	Transient line regulation	V_{OUT}=2.85 V V_{BAT}: 3.1 to 3.4V $t_R = t_F$ = 10 µs.		2		mV

Table 52. SD/MMC/SDIO card interface (continued)

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
VMMC regulator specifications ('pdn_vmmc' = 1)						
L_{DRT}	Transient load regulation	I_{OUT} = [1; 150] mA $t_R = t_F$ = 1 µs		25		mV
t_S	Settling time OFF->ON	I_{OUT} = 0 mA			100	µs
t_D	Discharge time ON>OFF	I_{OUT} = 0 mA			1	ms
Bus line specifications						
RA(2)	Pull-up resistor	To prevent bus from floating		1.5		MΩ
RB	Pull-down resistor	To prevent bus from floating		1.5		MΩ
f_{DT}	Clock frequency data transfert mode	With CL = 30pF			52	MHz
f_{ID}	Clock frequency identification mode	With CL = 30pF			400	kHz
T_{PHC}	Propagation time from Host to card	*Figure 15*		7		ns
T_{PCH}	Propagation time from card to host	*Figure 15*		7		ns
T_{SHC}	Clock /data skew time from host to card	*Figure 15* Reference is CLKOUT		+/- 0.5		ns
T_{SCH}	Clock /data skew time from card to host	*Figure 15* Reference is MMCLK		+/- 0.5		ns
T_R	Rise time				3	ns
T_F	Fall time				3	ns
$C1_{LINE}$	Between host and STw4811	Bus line capacitance f < 52 MHz			20(3)	pF
$C2_{LINE}$	Between STw4811 and MMC card	Bus line capacitance f < 52 MHz			20 + 20(4)	pF

1. Guaranteed by design
2. MMC interface pull up resistors are in EMIF06-HCM01F2 device (7 KΩ for CMD; 75 KΩ for Data wires)
3. 20 pF for equivalent board parasitic capacitance.
4. 20 pF for EMIF06 protection + 20 pF for board parasitic capacitance.

Figure 15. Propagation and clock/data skew times



6 Application information

6.1 Components list

Table 53. Components list

Name	Typical value	Comments	Function
C1	22µF	In the complete system application, the sum of the capacitors connected on each STw4811 ball must never be less than 30% of the value indicated in the typical value column of this table. This includes all capacitor parameters: – production dispersion – DC bias voltage applied – temperature range of the complete system application – aging	VIO_VMEM output filter
C4			VCORE output filter
C2	10µF		VBAT_VIOVMEM decoupling
C3			VBAT_ANA decoupling
C5			VBAT_VCORE decoupling
C6	1µF		VPLL output filter
C7			VANA output filter
C8			VREF output filter
C10			VUSB output filter
C13			VAUX output filter
C9	470nF		Flying capacitor for charge pump
C11	4.7µF		VBUS output filter (tank charge pump capacitor)
C12	2.2µF		VSD_MMC output filter
C13, C14, C15, C16, C17	1 µF		Vbattery input voltage decoupling capacitors
L1	4.7µH	See *Table 54* for recommended coils	Coil VIOVMEM DC/DC
L2			Coil VCORE DC/DC

Table 54. Recommended coils

Supplier	Part number	DCR (Ω)	Irms[1] (A)	L x l x h (mm * mm * mm)
TDK	VLF3010AT-4R7MR70	0.28	0.7	2.8 * 2.6 * 1.0
	VLF3012AT-4R7MR74	0.16	0.74	2.8 * 2.6 * 1.2
	VLF4012AT-4R7M1R1	0.14	1.1	3.7 * 3.5 * 1.2
Coilcraft	DO1605T-472MX	0.15	1.1	5.5 * 4.2 * 1.8
	DO3314-472ML	0.32	1.1	3.3 * 3.3 * 1.4
	ME3320-472MX	0.19	1.1	3.2 * 2.5 * 2.0

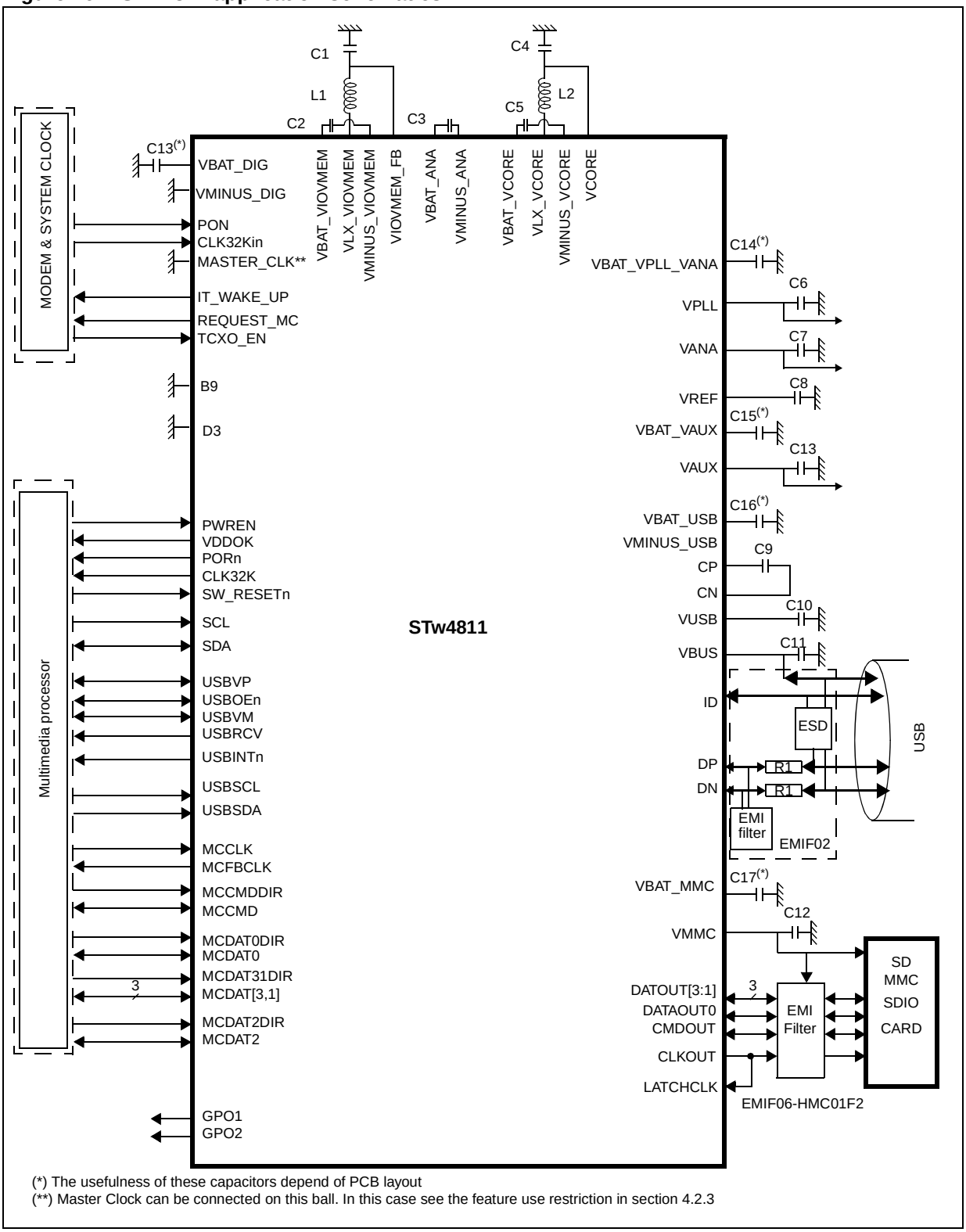
1. Irms: 30% decrease of initial value

Table 55. Other ST components

Name	Order code	Function
EMIF02	EMIF02USB05	USB ESD/EMI Protection
EMIF06	EMIF06-HMC01F2	MMC Interface ESD/EMI Protection

6.2 Application schematics

Figure 16. STw4811 application schematics



(*) The usefulness of these capacitors depend of PCB layout
(**) Master Clock can be connected on this ball. In this case see the feature use restriction in section 4.2.3

7 Package mechanical data

In order to meet environmental requirements, ST-Ericsson offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is a trademark of STMicroelectronics group of companies. ECOPACK specifications are available at: www.st.com.

7.1 TFBGA 84 balls

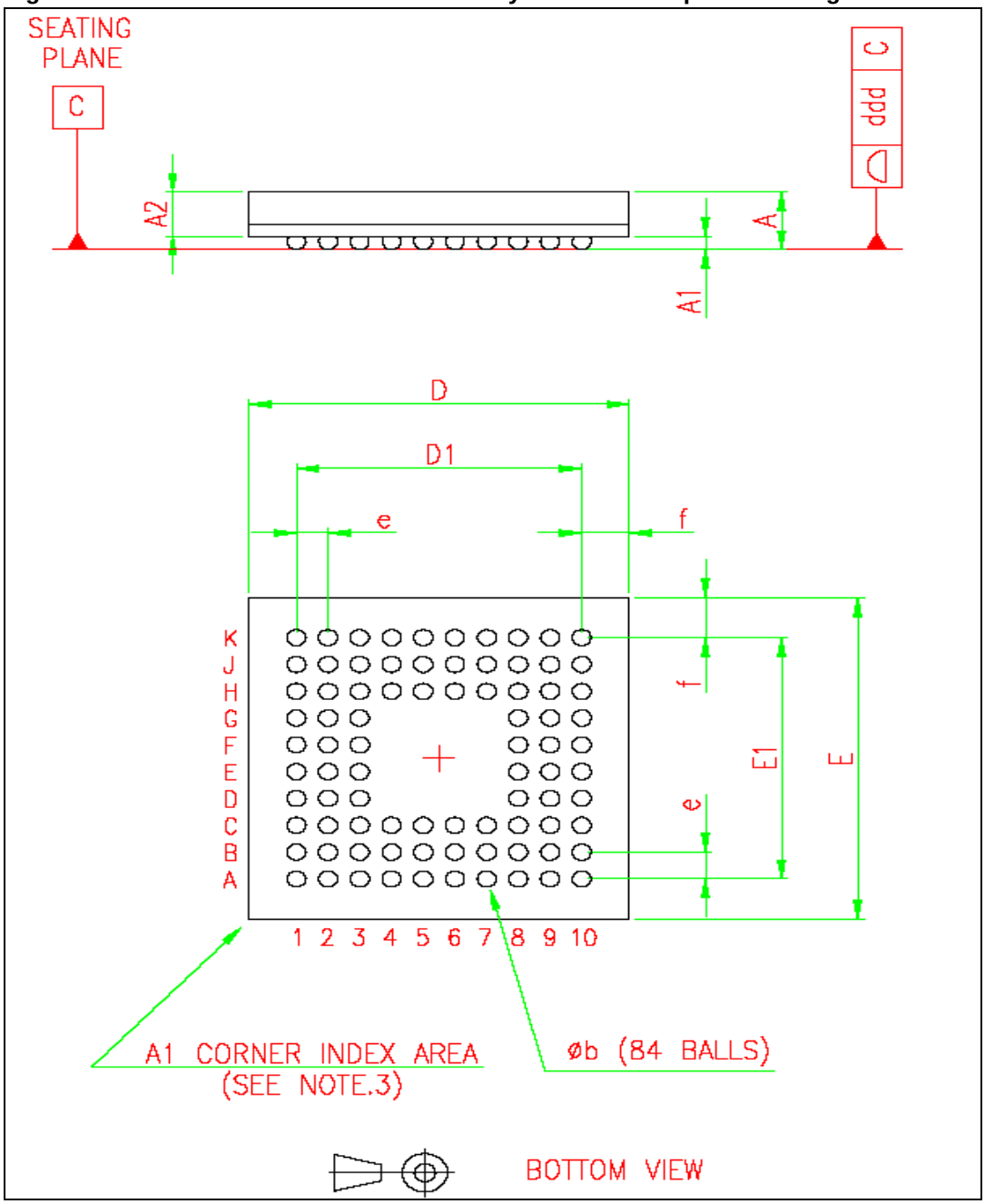
See *Figure 17: TFBGA 84 balls 6x6x1.2mm body size / 0.5 ball pitch drawing*.

Table 56. TFBGA 84 balls 6x6x1.2mm body size / 0.5 ball pitch dimensions(1)

Drawing dimensions (mm)	Min.	Typ.	Max.
A			1.16
A1	0.20	0.25	0.30
A2		0.82	
b	0.25	0.30	0.35
D	5.90	6.00	6.10
D1		4.50	
E	5.90	6.00	6.10
E1		4.50	
e	0.45	0.50	0.55
f	0.65	0.75	0.85
ddd			0.08

1. These measurements conform to JEDEC standards

Figure 17. TFBGA 84 balls 6x6x1.2mm body size / 0.5 ball pitch drawing



Note: The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

7.2 VFBGA 84 balls

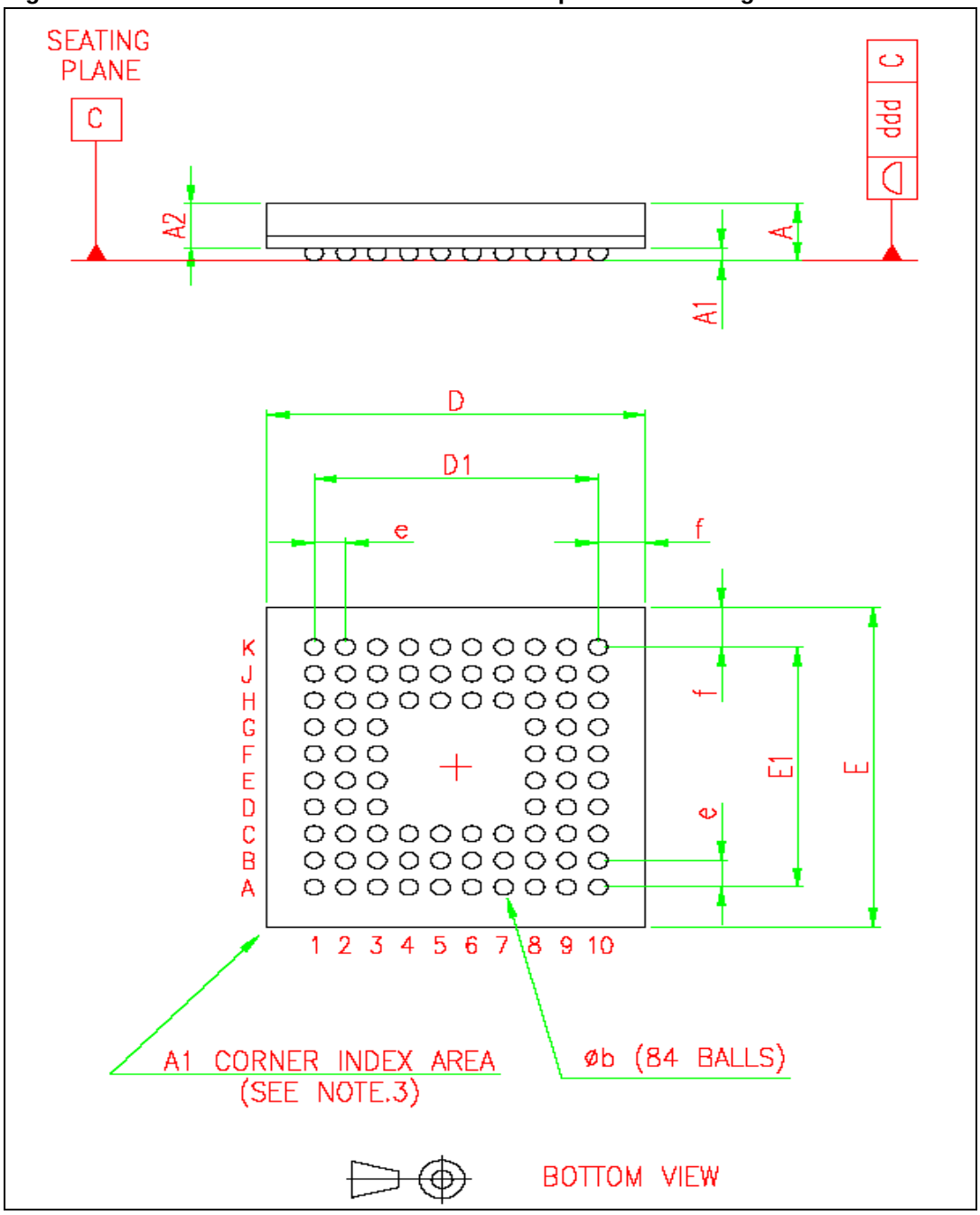
See *Figure 18: VFBGA 84 balls 4.6x4.6x1.0 mm ball pitch 0.4 drawing*.

Table 57. VFBGA 84 balls / 4.6x4.6x1.0 mm body size / 0.4 mm ball pitch(1)

Drawing dimensions (mm)	Min.	Typ.	Max.
A			0.864
A1	0.15	0.19	0.23
A2		0.615	
A3		0.18	
A4		0.435	
b	0.21	0.25	0.29
D	4.55	4.60	4.65
D1		3.60	
E	4.55	4.60	4.65
E1		3.60	
e		0.40	
f		0.50	
ddd			0.08
eee			0.13
fff			0.04

1. These measurements conform to JEDEC standards

Figure 18. VFBGA 84 balls 4.6x4.6x1.0 mm ball pitch 0.4 drawing



Note: The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

8 Ordering information

Table 58. Order codes

Part number	Package	Comments	Packing
STW4811MBHD/LF	TFBGA84- 6x 6 x 1.2 mm / 0.5 mm pitch	-	Tray
STW4811MBHDT/LF	TFBGA84- 6x 6 x 1.2 mm / 0.5 mm pitch	-	Tape and Reel
STW4811MBRA/LF	VFBGA 84 - 4.6x 4.6 x 1 mm / 0.4 mm pitch	-	Tray
STW4811MBRAT/LF	VFBGA 84 - 4.6x 4.6 x 1 mm / 0.4 mm pitch	-	Tape and Reel
STW4811NBHD/LF	TFBGA84- 6x 6 x 1.2 mm / 0.5 mm pitch	-	Tray
STW4811NBHDT/LF	TFBGA84- 6x 6 x 1.2 mm / 0.5 mm pitch	-	Tape and Reel
STW4811NBRA/LF	VFBGA 84 - 4.6x 4.6 x 1 mm / 0.4 mm pitch	-	Tray
STW4811NBRAT/LF	VFBGA 84 - 4.6x 4.6 x 1 mm / 0.4 mm pitch	-	Tape and Reel
STW4811MBRAT/HF	VFBGA 84 - 4.6x 4.6 x 1 mm / 0.4 mm pitch	ECOPACK2	Tape and Reel

Note: STw4811M: Vaux OFF at start up

STw4811N: Vaux ON at start up

9 Revision history

Table 59. Document revision history

Date	Revision	Changes
05-Sep-2007	1	Initial release on www.st.com. Reviewed the first sentence in *Section 5.3: Power supply* to precise 'typical' parameters.
17-Apr-2008	2	Updated the document status to 'datasheet' with respect to the device maturity level.
25-Aug-2008	3	Updated the maximum current value of the step-down converter for processor core to 700 mA in *Features*, *Chapter 1: Overview*, *Section 4.3.2: VCORE regulator: DC/DC STEP- DOWN regulator* and *Table 39: VCORE DC/DC step-down converter*.
04-June-2010	4	Updated *Chapter 8: Ordering information* and the ECOPACK information in *Chapter 7: Package mechanical data*