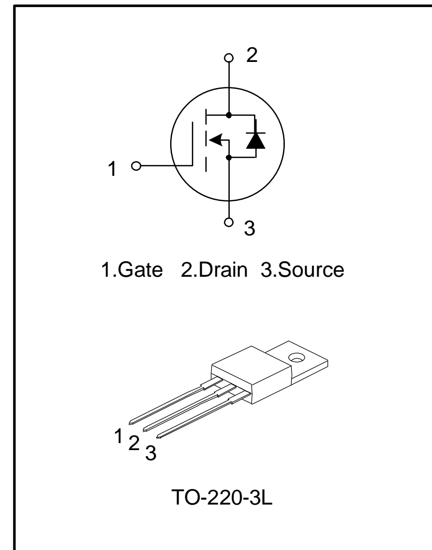
2A, 600V N-Channel MOSFET

GENERAL DESCRIPTION

SVD2N60T is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure DMOS technology. The improved planar stripe cell and the improved guarding ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

* 2A,600V,$R_{DS(on)(typ.)}$=4.0Ω@V_{GS}=10V
* Low gate charge
* Low C_{rss}
* Fast switching
* Improved dv/dt capability

ORDERING SPECIFICATIONS

Part No.	Package	Marking	Shipping
SVD2N60T	TO-220-3L	SVD2N60T	50Unit/Tube

ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	±30	V
Drain Current	I_D	2.0	A
Drain Current Pulsed	I_{DM}	8	A
Power Dissipation(T_C=25°C)	P_D	44	W
-Derate above 25°C		0.22	W/°C
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	120	mJ
Repetitive Avalanche Energy	E_{AR}	5.4	mJ
Operation Junction Temperature	T_J	-55～+150	°C
Storage Temperature	Tstg	-55～+150	°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{θJC}$	2.87	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{θJA}$	100	°C/W

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=1.0A	--	4.0	4.6	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	320	380	pF
Output Capacitance	C_{oss}		--	30	45	
Reverse Transfer Capacitance	C_{rss}		--	3	5.6	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V,I_D=2.0A, R_G=25Ω (Note 2,3)	--	13	30	ns
Turn-on Rise Time	t_r		--	12	60	
Turn-off Delay Time	$t_{d(off)}$		--	73	100	
Turn-off Fall Time	t_f		--	14.3	70	
Total Gate Charge	Q_g	V_{DS}=480V,I_D=2.0A, V_{GS}=10V (Note 2,3)	--	9.3	13	nC
Gate-Source Charge	Q_{gs}		--	2.0	--	
Gate-Drain Charge	Q_{gd}		--	3.3	--	

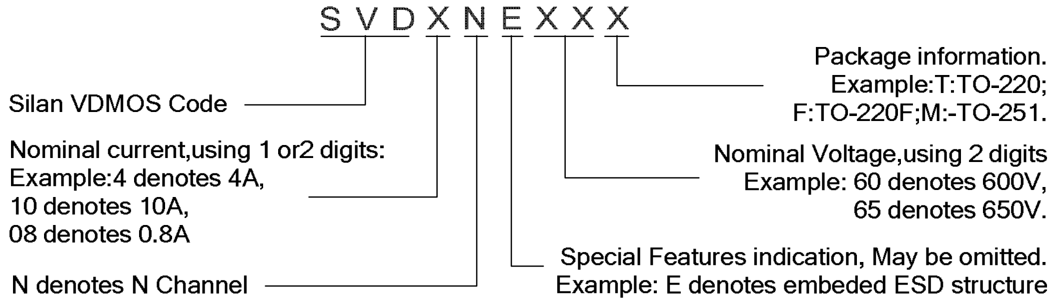
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	2	A
Pulsed Source Current	I_{SM}		--	--	8.0	
Diode Forward Voltage	V_{SD}	I_S=2.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=2.0A,V_{GS}=0V, dI_F/dt=100A/μS	--	230	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.0	--	μC

Notes:

1. L=56mH, I_{AS}=2.0A,V_{DD}=50V,R_G=25Ω,starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

NOMENCLATURE



TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

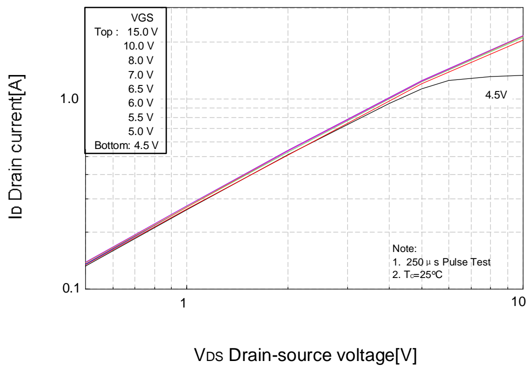


Figure 2. Transfer Characteristics

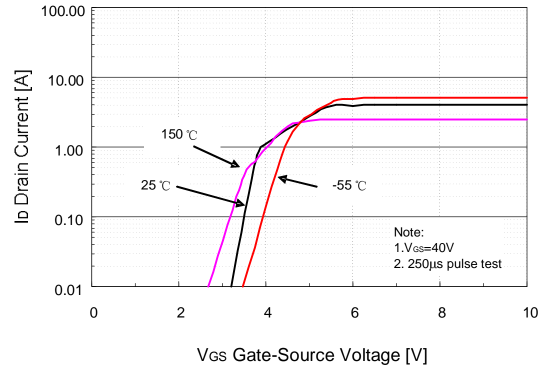


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

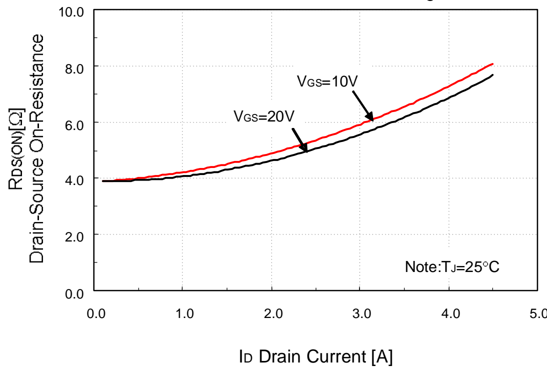
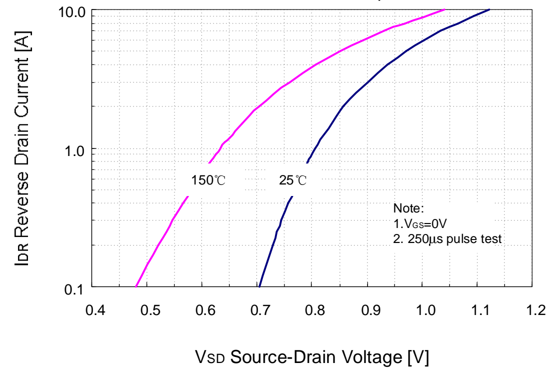


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS (continued)

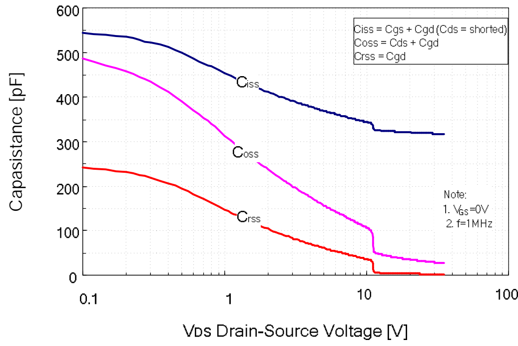


Figure 5. Capacitance Characteristics

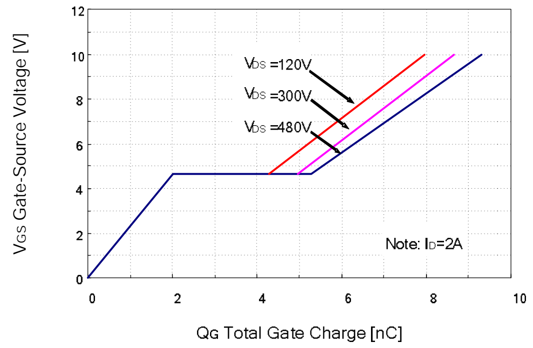


Figure 6. Gate Charge Characteristics

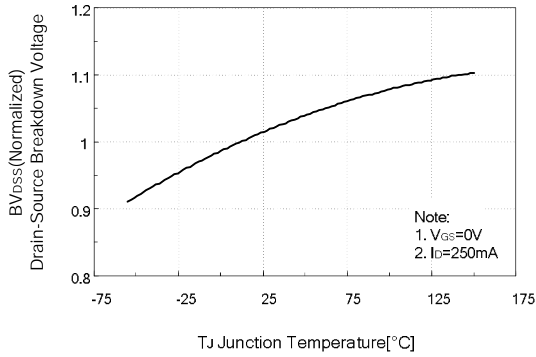


Figure 7. Breakdown Voltage Variation vs. Temperature

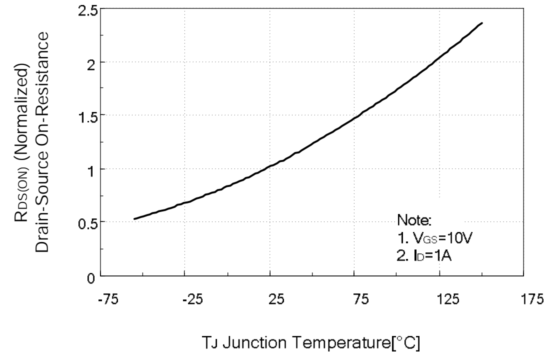
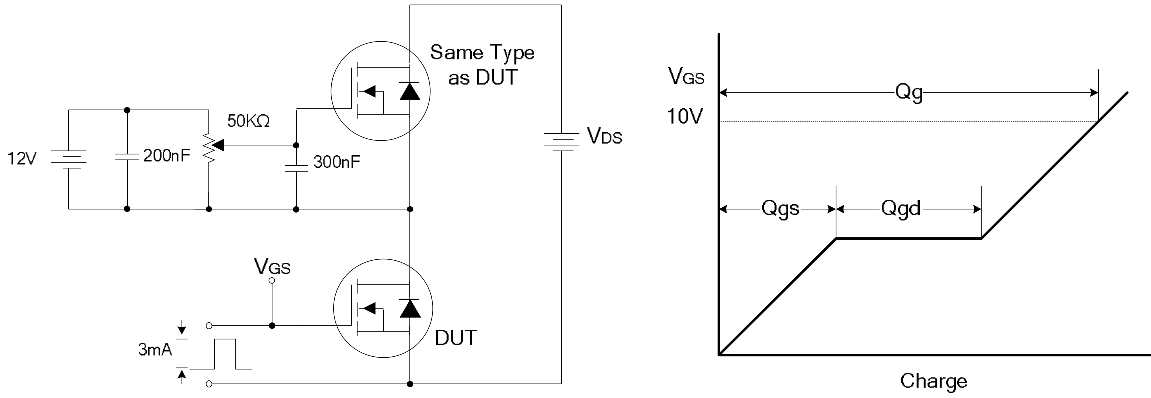


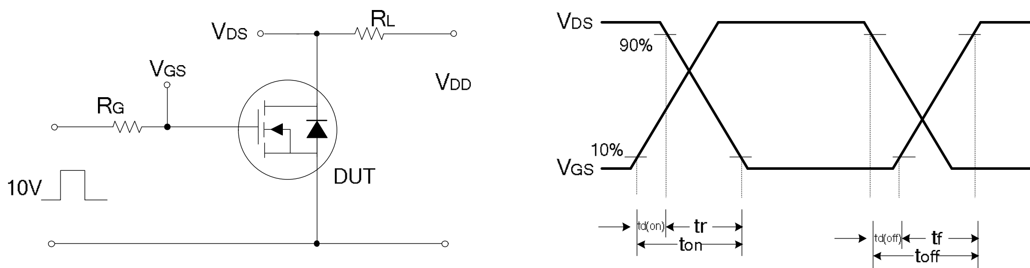
Figure 8. On-resistance Variation vs Temperature

TYPICAL TEST CIRCUIT

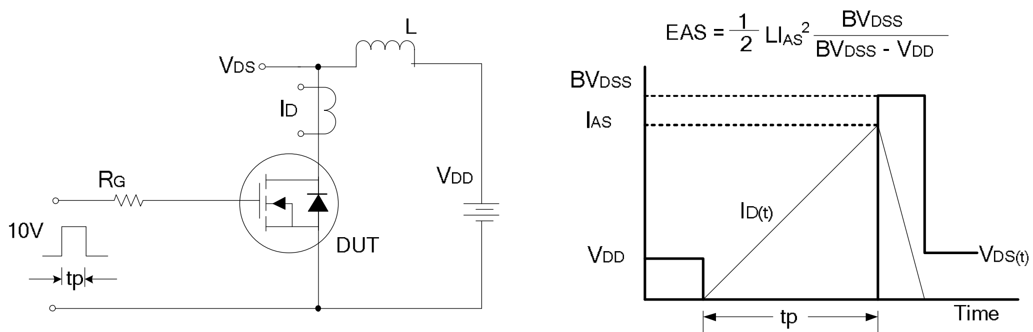
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

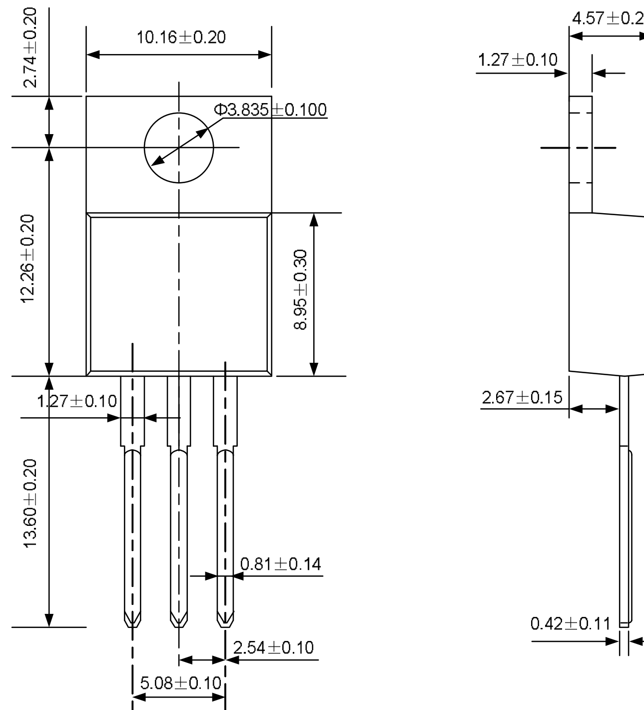


Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220-3L(One) UNIT: mm



TO-220-3L（Two） UNIT: mm