

## FEATURES

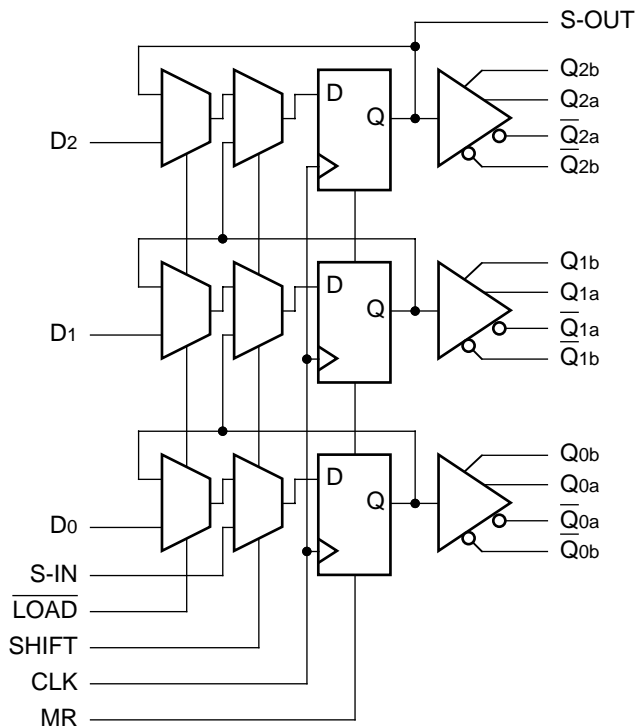
- Scannable version E112 driver
- Extended 100E VEE range of -4.2V to -5.5V
- 1025ps max. CLK to Output
- Dual differential outputs
- Master Reset
- Internal 75KΩ input pull-down resistors
- Fully compatible with industry standard 10KH, 100K ECL levels
- Fully compatible with Motorola MC10E/100E212
- Available in 28-pin PLCC package

## DESCRIPTION

The SY10/100E212 are scannable registered ECL drivers typically used as fan-out memory address drivers for ECL cache driving. In a VLSI array-based CPU design, use of the E212 allows the user to conserve array output cell functionality and also output pins.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

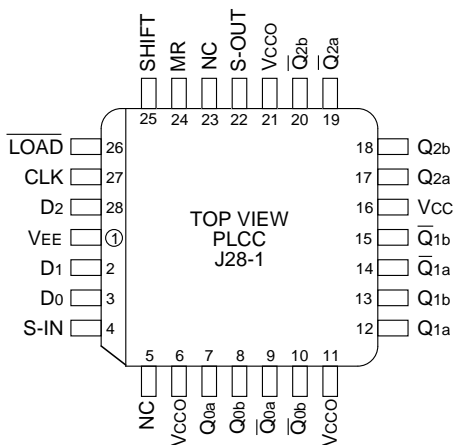
## BLOCK DIAGRAM



## PIN NAMES

Pin	Function
D0 – D2	Data Inputs
S-IN	Scan Input
LOAD	LOAD/HOLD Control
SHIFT	Scan Control
CLK	Clock
MR	Master Reset
S-OUT	Scan Output
Q[0:2]a, Q[0:2]b	True Outputs
$\bar{Q}$ [0:2]a, $\bar{Q}$ [0:2]b	Inverting Outputs
Vcco	Vcc to Output

**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E212JC	J28-1	Commercial	SY10E212JC	Sn-Pb
SY10E212JCTR <sup>(2)</sup>	J28-1	Commercial	SY10E212JC	Sn-Pb
SY100E212JC	J28-1	Commercial	SY100E212JC	Sn-Pb
SY100E212JCTR <sup>(2)</sup>	J28-1	Commercial	SY100E212JC	Sn-Pb
SY10E212JZ <sup>(3)</sup>	J28-1	Commercial	SY10E212JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E212JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY10E212JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E212JZ <sup>(3)</sup>	J28-1	Commercial	SY100E212JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E212JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY100E212JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

**TRUTH TABLE**

$\overline{\text{LOAD}}$	SHIFT	MR	Mode
L	L	L	Load
H	L	L	Hold
X	H	L	Shift
X	X	H	Reset

**DC ELECTRICAL CHARACTERISTICS**

$V_{EE} = V_{EE} (\text{Min.})$  to  $V_{EE} (\text{Max.})$ ;  $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I <sub>IH</sub>	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I <sub>EE</sub>	Power Supply Current										mA	—
	10E	—	80	96	—	80	96	—	80	96		
	100E	—	80	96	—	80	96	—	92	110		

**AC ELECTRICAL CHARACTERISTICS**

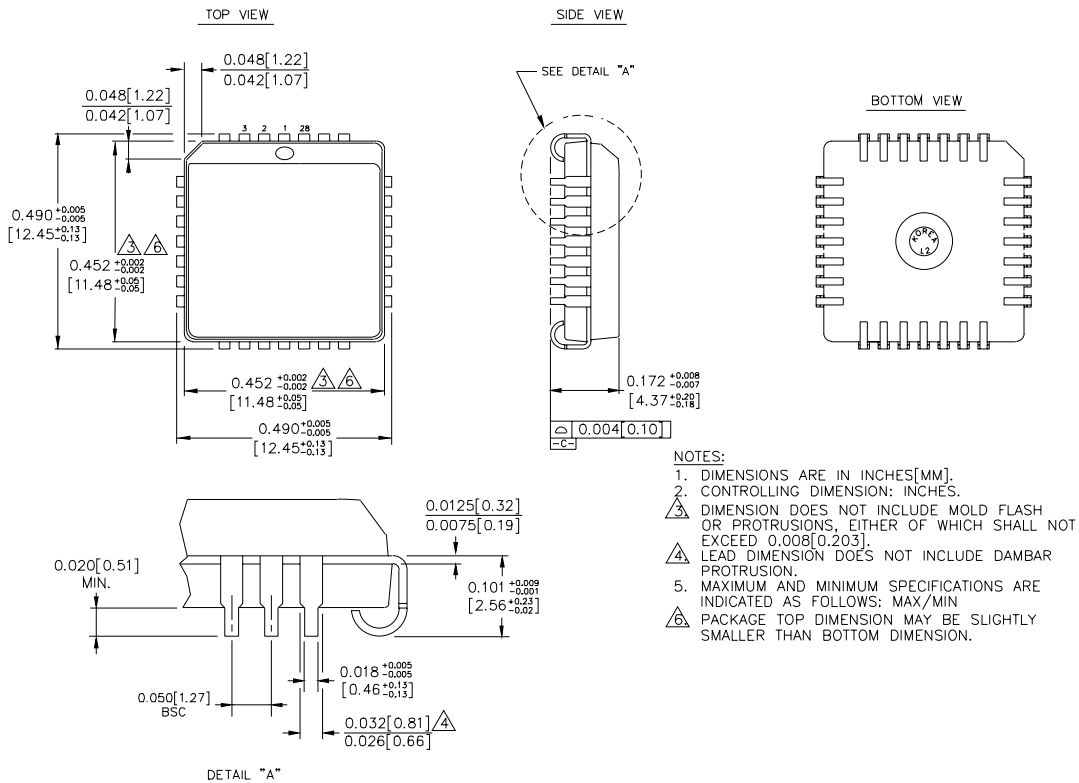
$V_{EE} = V_{EE} (\text{Min.})$  to  $V_{EE} (\text{Max.})$ ;  $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t <sub>PD</sub>	Propagation Delay to Output CLK MR CLK to S-OUT	575 575 575	800 800 800	1025 1025 1025	575 575 575	800 800 800	1025 1025 1025	575 575 575	800 800 800	1025 1025 1025	ps	—
t <sub>s</sub>	Set-up Time D SHIFT LOAD S-IN	175 150 225 150	25 -50 50 -50	— — — —	175 150 225 150	25 -50 50 -50	— — — —	175 150 225 150	25 -50 50 -50	— — — —	ps	—
t <sub>H</sub>	Hold Time D SHIFT LOAD S-IN	250 300 225 300	25 100 0 100	— — — —	250 300 225 300	25 100 0 100	— — — —	250 300 225 300	25 100 0 100	— — — —	ps	—
t <sub>RR</sub>	Reset Recovery	600	350	—	600	350	—	600	350	—	ps	—
t <sub>skew</sub>	Within-Device Skew	—	100	—	—	100	—	—	100	—	ps	1
t <sub>skew</sub>	Within-Gate Skew	—	50	—	—	50	—	—	50	—	ps	2
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Times 20% to 80%	275	425	650	275	425	650	275	425	650	ps	—

**Notes:**

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input.

**28-PIN PLCC (J28-1)**



Rev. 03

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