Features

- **Single 3-V Supply Voltage**
- **High Power-added Efficient Power Amplifier (P_{out} Typically 23 dBm)**
- **Ramp-controlled Output Power**
- **Current-saving Standby Mode**
- **Few External Components**
- **HP-VFQFP-N16 Package**

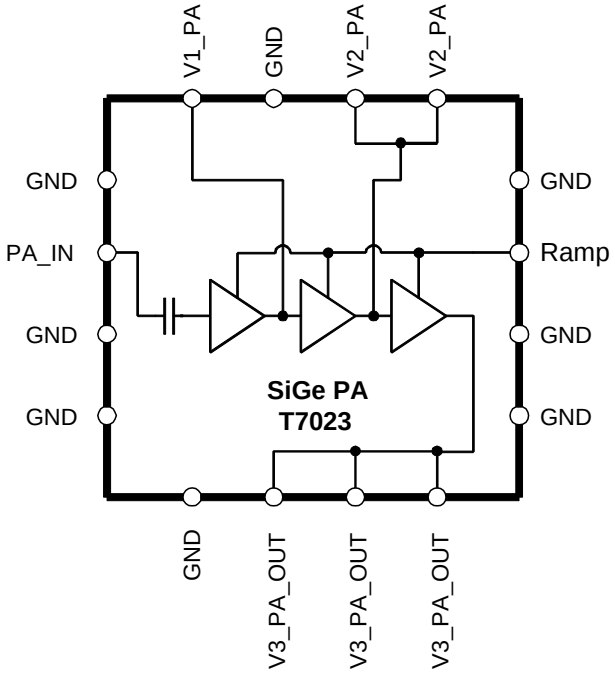
Electrostatic sensitive device.
Observe precautions for handling.

Description

The T7023 is a monolithic SiGe power amplifier. It is especially designed for operation in TDMA systems like Bluetooth, DECT, and many other ISM applications according to FCC part 15.

Due to the ramp-control feature and a very low quiescent current, an external switch transistor for V_S is not required.

Figure 1. Block Diagram



ISM/Bluetooth™ 2.4-GHz Power Amplifier

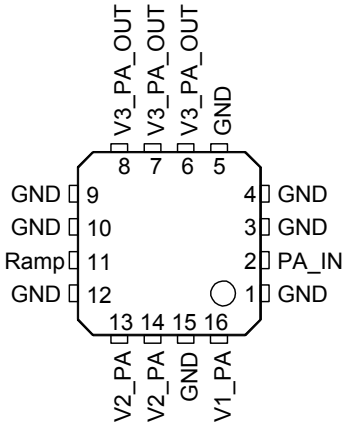
T7023

Preliminary

Rev. 4532A–BLURF–09/02

Pin Configuration

Figure 2. Pinning HP-VFQFP-N16



Pin Description

Pin	Symbol	Function
1	GND	Ground
2	PA_IN	Power amplifier input
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
7	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
8	V3_PA_OUT	Inductor to power supply and matching network for power amplifier output
9	GND	Ground
10	GND	Ground
11	RAMP	Power ramping control input
12	GND	Ground
13	V2_PA	Inductor to power supply for power amplifier
14	V2_PA	Inductor to power supply for power amplifier
15	GND	Ground
16	V1_PA	Supply voltage for power amplifier
Slug	GND	Ground

Absolute Maximum Ratings

All voltages are referred to ground (Pins GND and slug), no RF

Parameters	Symbol	Value	Unit
Supply voltage Pins V1_PA, V2_PA and V3_PA_OUT	V_S	6	V
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-40 to +125	°C
RF input power PA	P_{inPA}	10 dBm	dBm

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient HP-VFQFP-N16	R_{thJA}	TBD	K/W

Operating Range

All voltages are referred to ground (Pins GND and slug). Power supply points are V1_PA, V2_PA, V3_PA_OUT.
The following table represents the sum of all supply currents depending on the TX mode.

Parameters		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pins V1_PA, V2_PA and V3_PA_OUT	V_S	2.7	3.0	4.6	V
Supply current		I_S		165		mA
Standby current		$I_{S\_standby}$		10		µA
Ambient temperature		T_{amb}	-25	+25	+70	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 3.0 V, T_{amb} = 25°C

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Power Amplifier (1)						
Supply voltage	Pins V1_PA, V2_PA and V3_PA_OUT	V_S	2.7	3.0	4.6	V
Supply current	TX	I_{S_TX}		165		mA
	RX (PA off), $V_{RAMP} \geq 0.1$ V	I_{S_RX}			10	µA
	Standby	$I_{S\_standby}$			10	µA
Frequency range	TX	f	2.4		2.5	GHz
Gain-control range	TX	ΔGp	60	42		dB
Power gain maximum	TX Pin PA_IN to V3_PA_OUT	Gp	28	30	33	dB
Power gain minimum	TX Pin PA_IN to V3_PA_OUT	Gp	-40		-17	dB
Ramping voltage maximum	TX, power gain (maximum) Pin RAMP	$V_{RAMP\ max}$	1.7	1.75	1.83	V
Ramping voltage minimum	TX, power gain (minimum) Pin RAMP	$V_{RAMP\ min}$		0.1		V
Ramping current maximum	V = 1.75 V				0.5	mA
Power-added efficiency	TX	PAE	35	42		%
Saturated output power	TX, input power = 0 dBm referred to Pins V3_PA_OUT	P_{sat}	22.5	23	23.5	dBm
Input matching (2)	TX, Pin PA_IN	Load VSWR		<1.5:1		
Output matching (2)	TX, Pin V3_PA_OUT	Load VSWR		<1.5:1		
Harmonics at P_{sat} = 23 dBm	TX, Pin V3_PA_OUT	2 f_o			-30	dBc
Harmonics at P_{sat} = 23 dBm	TX, Pin V3_PA_OUT	3 f_o			-30	dBc

Notes: 1. Power amplifier shall be unconditionally stable, maximum duty cycle 100%, true CW operation, maximum load mismatch and duration: VSWR 10:1 (all phases) 10 s, Z_G = 50 Ω.
2. With external matching network, load impedance 50 Ω

Typical Operating Characteristics

Figure 3. Output Power and PAE versus Supply Voltage

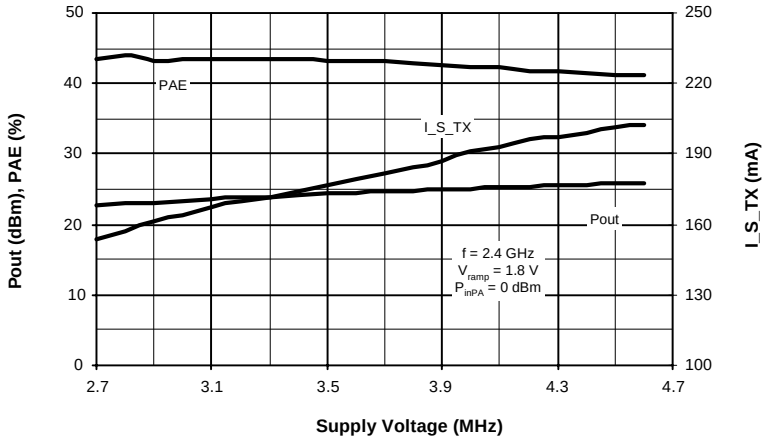


Figure 4. Output Power and PAE versus Frequency

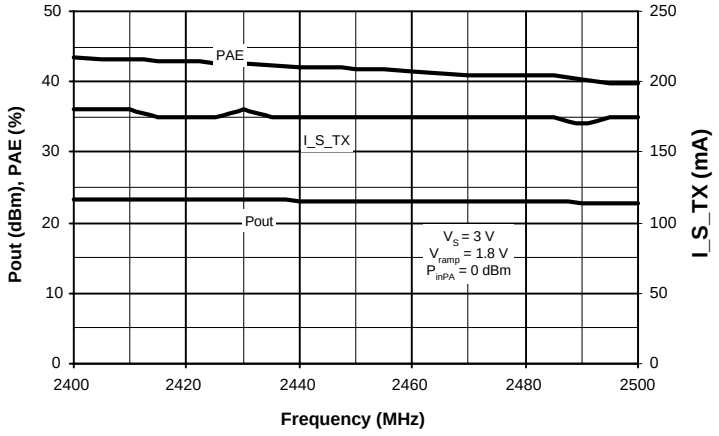


Figure 5. Output Power and PAE versus Ramp Voltage

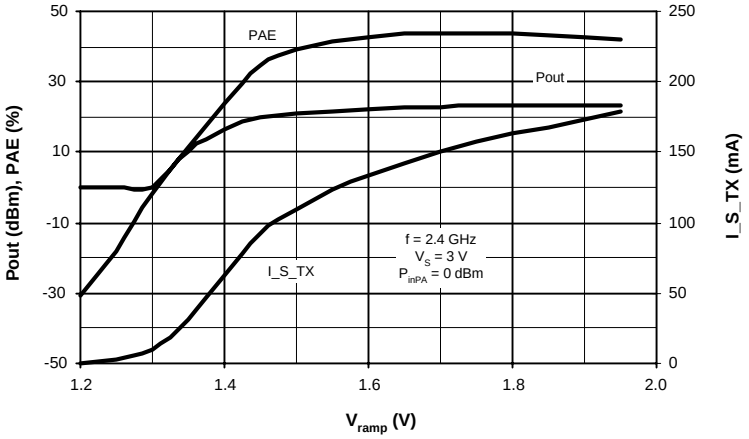


Figure 6. Output Power and PAE versus Input Power

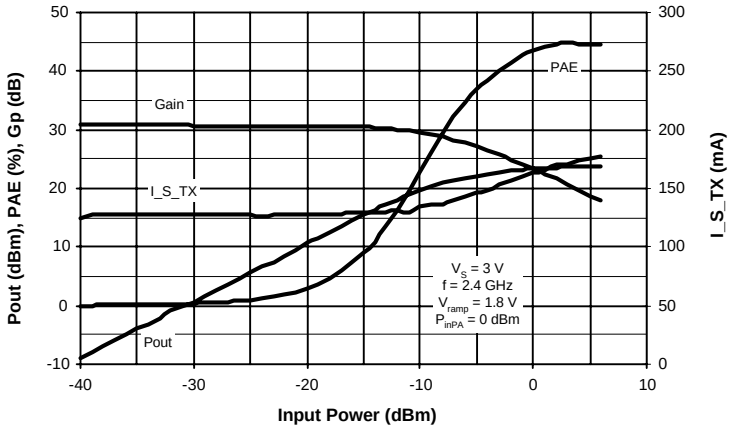


Figure 7. P_{out} versus V_{ramp} and Temperature

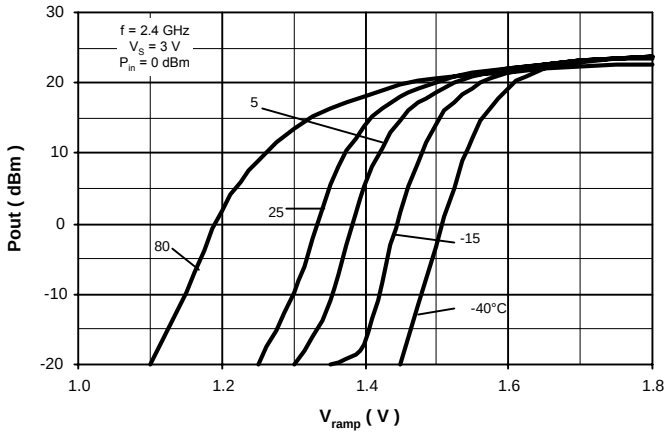


Figure 8. Output Power versus V_{Ramp} Current

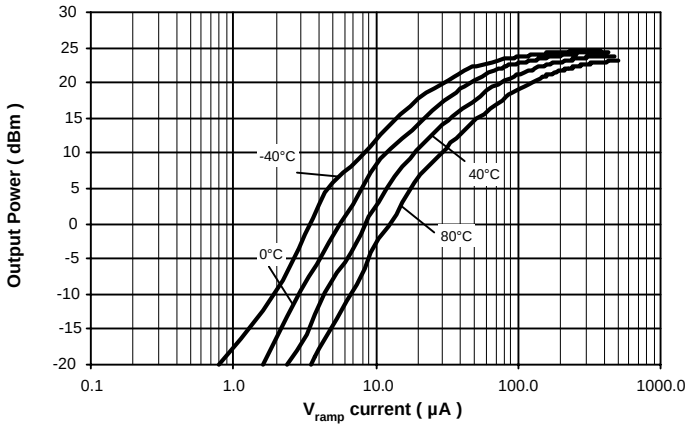
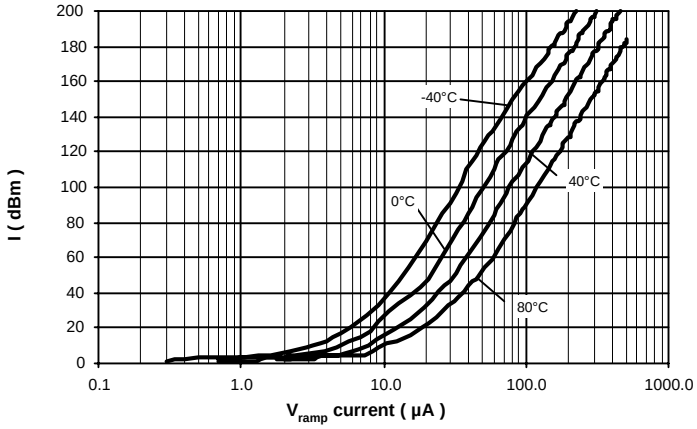


Figure 9. I versus V_{Ramp} Current



Input/Output Circuits

Figure 10. Input Circuit PA_IN/V1_PA

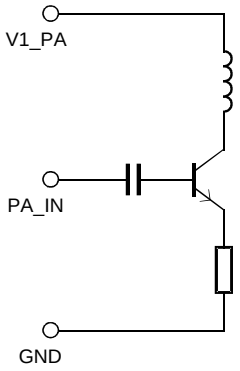


Figure 11. Input Circuit RAMP/V1_PA

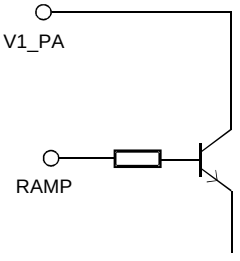


Figure 12. Input Circuit V2_PA

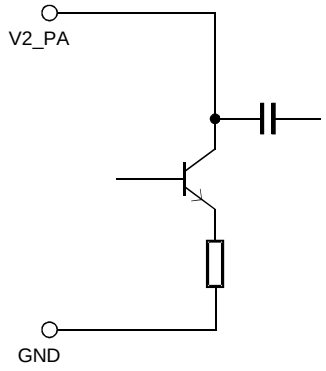


Figure 13. Input/Output Circuit V3_PA_OUT

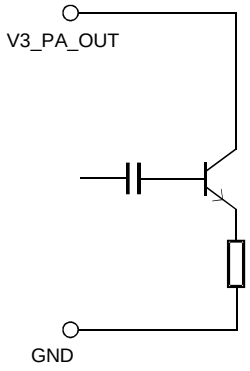


Figure 14. Application Board Schematic

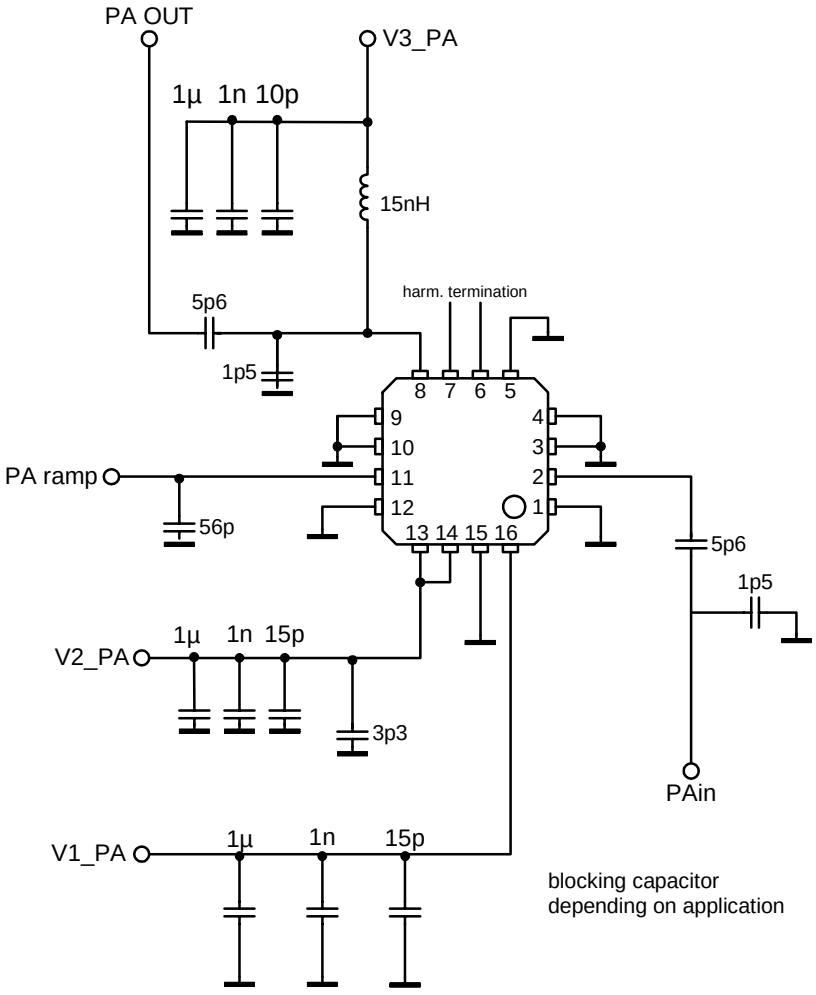
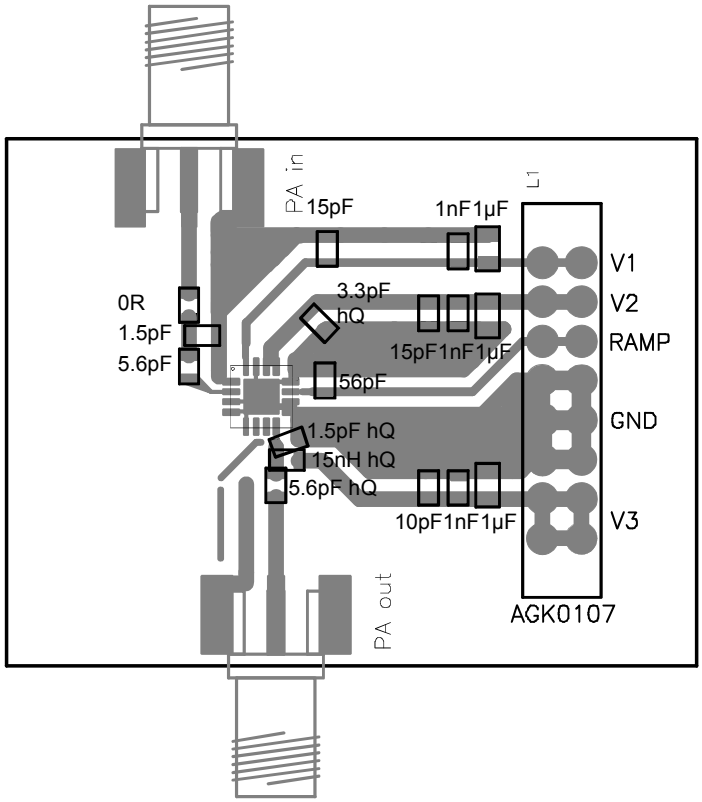


Figure 15. Application Board Layout



Gerberfiles are available on request.

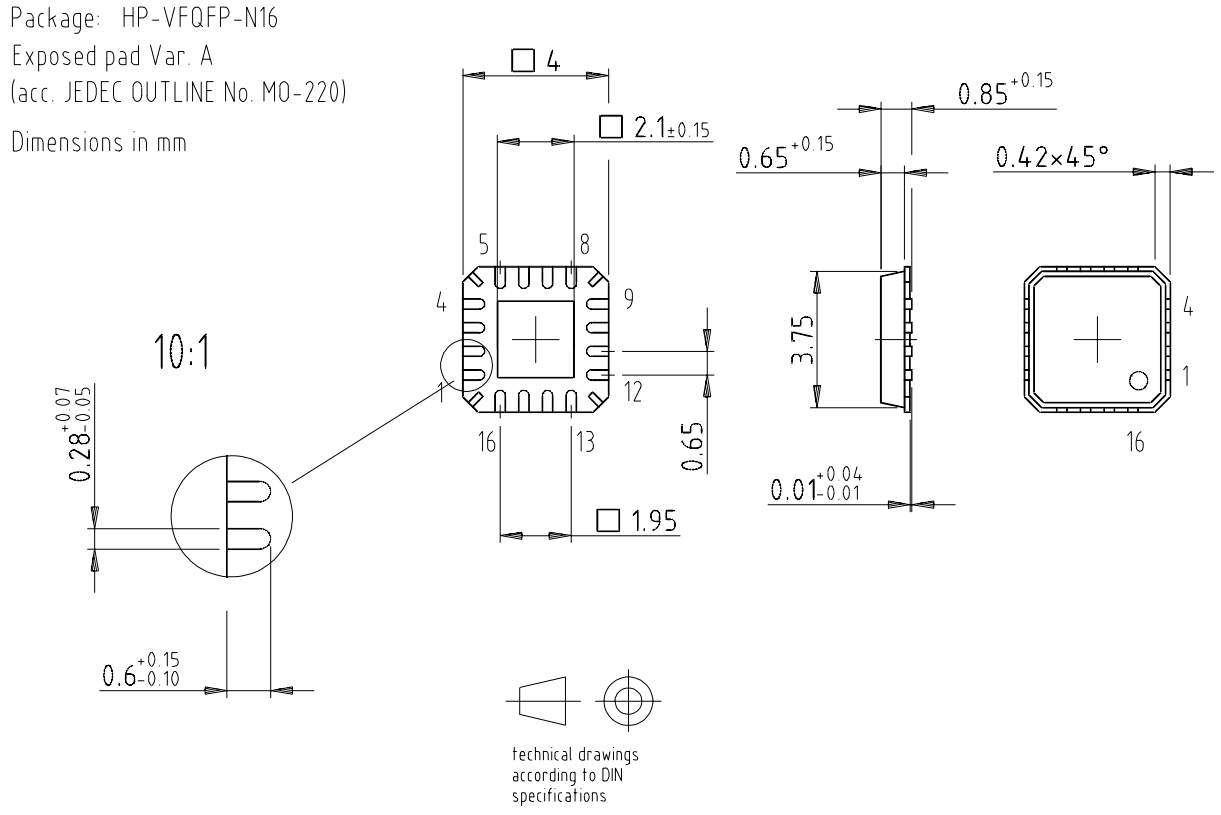
The application board consists of 4 layers:

1. top layer: RF-signals, 35 µm Cu
2. spacing: 490 µm FR4
3. second layer: GND, 35 µm Cu
4. spacing: 550 µm FR4
5. third layer: GND (optional), 35 µm Cu
6. spacing: 490 µm FR4
7. bottom layer: DC connection, 35 µm Cu

Ordering Information

Extended Type Number	Package	Remarks
T7023-PES	HP-VFQFP-N16	Tube
T7023-PEQ	HP-VFQFP-N16	Taped and reeled

Package Information



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