DC Accurate FSK Modulator

A typical, low cost, FSK modulator is implemented by injecting the modulation voltage into the phase lock loop of the carrier synthesizer. This is done in two ways, by summing the modulation voltage and the loop error voltage together and applying that to a VCO tuning port. Or, by using a separate tuning port usually having lower sensitivity to voltage changes. The modulating data would change the carrier frequency by a predetermined amount (deviation). This, however, causes a frequency error within the PLL that the loop begins to correct for. The effect of the loop correcting for the frequency errors caused by the modulation is analogous to passing the modulating signal through a high pass filter. Lower frequency components of the modulation signal get filtered off (or even eliminated). This results in unreliable communications for random data streams, especially for long strings of non-changing bits.

There have been several solutions developed and implemented that address this problem. One approach is to predistort the modulation signal to compensate for the effects of the PLL. This has limited results and a finite frequency range. Another commonly used method is to encode the data stream with such techniques as Manchester coding or split phase coding. The basis of this coding is to send two complementary symbols for every data bit, thus a transition is guaranteed for every data bit. This is very effective in that it fixes the lowest frequency component of the modulation signal so that a loop bandwidth can be designed to have a minimal effect on the coded data. Unfortunately, this means that the effective data rate of the radio is doubled, increasing channel bandwidth. The encoding procedure is rather simple (exclusive OR the data and clock together). The decoding is much more complicated requiring some synchronization to guarantee the correct two symbols are used to decode the data bit.

Other approaches avoid the problem altogether by modulating outside of the PLL loop. Modulating the reference crystal, for example, can do this. A varactor can be used with a crystal to pull the center frequency to the mark and space frequencies. Since the modulation occurs outside the loop, the PLL does not effect the modulation signal, it simply tracks the changes in the reference frequency. The pullability of the crystal will limit the achievable frequency deviation and thus the maximum data rate using this method. Given the variances in crystals and varactors, this would require tuning to set the desired deviation. Another method would be to generate the reference frequency with a Direct Digital Synthesizer and modulate within this synthesizer. This works very well and accurately but cost is considerably higher.

Another type of approach is to program the mark and space frequencies in the PLL. There are several ways to do this depending on the programmability of the PLL divider registers. A new technique takes advantage of low cost ICs that contain an integrated, simple PLL and the VCO functions. These devices are typically designed to be multipliers of a reference crystal to generate a local oscillator frequency or they can be modulated for FSK transmitters. One component of the PLL is the prescaler. This divides the VCO frequency down to the reference crystal frequency. The prescaler usually has 2 divide-by rates (N and N+1) and is referred to as dual modulus. By controlling the ratio of the 2 rates, the VCO frequency can be set to a desired frequency. Using one ratio for logic 1 and another ratio for logic 0 can effectively generate FSK modulation that is not affected by the PLL and therefore can be used for signals that contain near DC components.

One way to generate this ratio is to use a pulse width modulator. This is similar to how a typical PLL would work. The prescaler would divide by N for part of a cycle and then divide by N+1 for the remainder. This would synthesize a frequency that is N+(duty cycle) times the reference frequency. The step size between two frequencies is set by the resolution of the counter used to set the duty cycle. Another way to generate a ratio is to start with a clock pattern and periodically inject an extra bit. The ratio is then tied to the period of the injected bit. By changing the period of the injected bit, a new ratio is formed and thus a new synthesized frequency.

An example of this approach is as follows using a 4-bit programmable counter. By loading one set of bits into the counter with the carry-out, the counter can be programmed to divide the clock by s, (Fclk/s), resulting in a cycle rate of s/Fclk second. The first divider output, Qa, normally looks like Fclk divided by 2. If the programmed value s is chosen such that a “1” is loaded into the “a” divider (an odd number), then the Qa output stays a “1” from the previous state. This puts one more “1” in the Qa output than “0” for every cycle of the counter. This unequal number of 1s and 0s will define a

Copyright 1997-2000 RF Micro Devices, Inc.

fractional number over the cycle rate of the programmed bits. Different programmed bits can generate different fractional numbers and thus different synthesized frequencies. If b is the number of bits in the counter and s is the programmed word, then the fractional number generated is:

# of Qa states per cycle = 2^b-s

# of 0s per cycle = 2^b-s-1

Then fractional n = 2^b-s-1

The synthesized frequency can then be calculated as $F(ref)*(N+n)$. If s and $n(s)$ represent the space frequency and m and n(m) represent the mark frequency, then the peak to peak frequency deviation can be calculated as $F(ref)*(n(s)-n(m))$. This method can produce smaller deviations with fewer dividers than the previous method but offers fewer selections from which to chose.

A simple form of this technique is described in Figure 1. It is implemented with a 4-bit counter and the values of s and m are chosen such that only 1 of the 4 bits is different. Therefore, the data to be modulated onto the carrier is used to set or clear that divider every cycle. An infinite numbers of cycles can occur at either the mark of space frequency without correction by the PLL therefore making this modulator accurate down to DC.

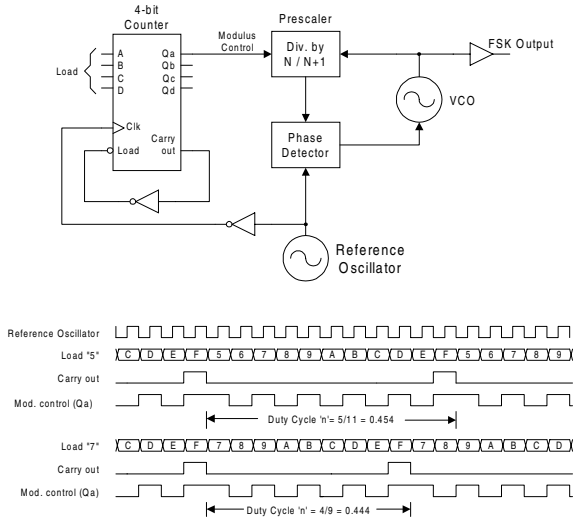

Figure 1. DC Accurate FSK Modulator

In the example of Figure 1, a 4-bit counter is used to control the divider ratio of the prescaler in a PLL synthesizer. The Qa output toggles high and low except when the carry out is asserted. Then the Qa output stays high with the correct load value. For a loaded value of '5', the Qa output will be low for 5 out of the 11 states of the counter, (16-5-1)/2. This sets up a ratio or duty cycle of n=.454. The 'B' bit of the counter can be changed from a 0 to a 1 to change the load value from 5 to 7. In this case the Qa output is low for 4 out of 9 states, ((16-7-1)/2) for a duty cycle of n=.444. The ratios modify the prescaler to produce an output frequency with a fractional divide by ratio, that is 128.454 or 128.444. Therefore the output frequencies differ by (128.454 - 128.444) times the reference oscillator. The rate of change on the modulus control pin is very high relative to the PLL loop bandwidth so the changes are averaged or smoothed out over time.

A simple hardware implementation of a radio link using this method is described here. A family of transmitter or transceiver ICs from RF Micro Devices offer the internal PLL and dual modulus prescaler which can be used in this design. The RF2513 was chosen to demonstrate a simple low cost transmitter for USA ISM band applications. The RF2513 contains all the active circuitry necessary to implement a single IC FSK transmitter; a reference crystal oscillator, PLL, dual modulus prescaler, VCO, TX buffer amp, and PA. The RF2513 also has an internal varactor for tuning the VCO. By using printed inductors for the resonators, the external component count is minimized. A 74HC161 4-bit counter is used to implement the counter and a 74HC04 is used for the necessary inversion to load the counter and to buffer the reference oscillator used for the clock. The schematic of the final circuit is shown in Figure 2.

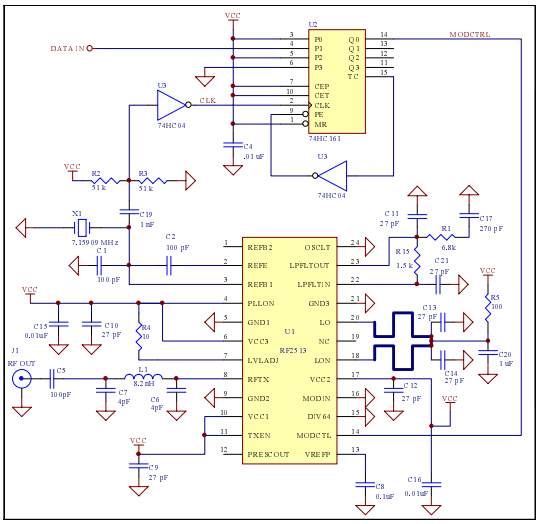

Figure 2. Example Schematic of DC Accurate Modulator

Copyright 1997-2000 RF Micro Devices, Inc.

The reference crystal which is supplied with the RF2513 eval board is 7.15909MHz,. This normally produces a transmit frequency of 916.4MHz for a divide by 128 setting. Other values could easily be substituted. Since the divider ratios are 128.454 and 128.444, the output frequencies are 919.6137MHz for a logic “0” and 919.5421MHz for a logic “1” input. Thus, peak to peak deviation is fixed at 71.6kHz. Since the deviation is derived by numerical means as a fraction of the crystal frequency, it is very accurate and repeatable without the tuning. This deviation allows for a wide range of data rates, from 1bps to 100kbps by using different modulation indices. The upper limit is actually limited by the loop bandwidth of the PLL, up to the point where the modulation index becomes too small. In Figure 3, a pseudo random data pattern clocked at a 100bps bit rate is shown as an example of the low data rate capability. The recovered data maintains its DC level through several consecutive data bits providing evidence of the DC accuracy of this modulator. In Figure 4, the same pseudo random data pattern at 72kbps is shown. In each instance, a RF2917 evaluation board tuned for 919.578MHz was used to demodulate the data.

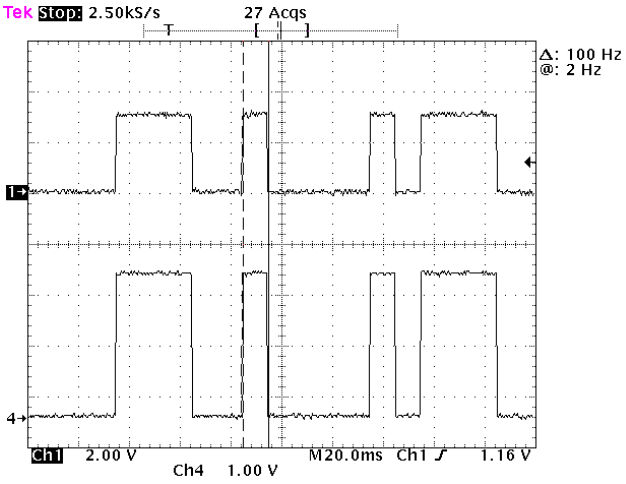

Figure 3. Transmitted Data (top) and Recovered Data (bottom) at 100Bps

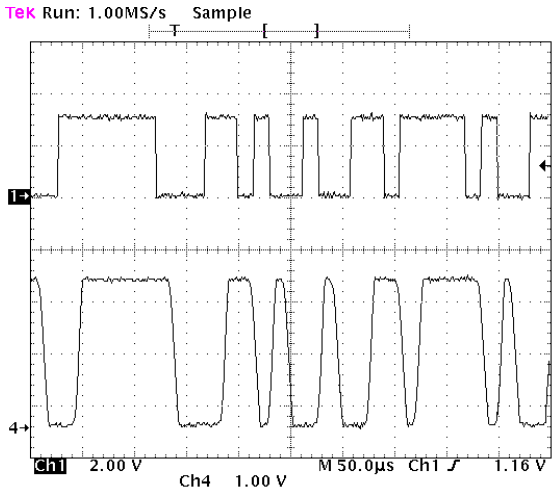

Figure 4. Transmitted Data (top) and Recovered Data (bottom) at 72Kbps

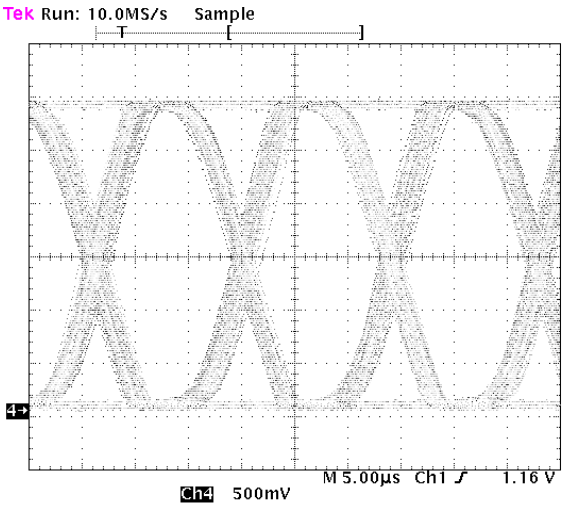

Figure 5. Kbps Eye Pattern

The PLL loop bandwidth is designed to be reasonably wide and yet still provide reasonable spurious rejection. The loop bandwidth is one of the factors that determine the rate at which the VCO changes from one frequency to the other and, thus, the upper data rates. As data rates exceed the loop bandwidth, the modulation waveform becomes band-limited and takes on the appearance of inter-symbol interference. Figure 5 shows the eye pattern of this modulator as seen at the RF2917 receiver output. The flatness of the eye pattern attests to immunity of this modulator to random

Copyright 1997-2000 RF Micro Devices, Inc.

data patterns. The slew rate due to the PLL loop bandwidth is also evident here. the high loop bandwidth offers a couple of advantages. First, the close-in phase noise of the VCO is corrected for by the PLL, at best to that of the crystal. More importantly, though, is that the PLL synthesizer will have a faster lock time because of the higher bandwidth. This is useful for systems that occasionally burst a packet of data and then shut down to conserve battery life. Burst type systems are also affected by load pulling when the PA is turned on. The faster loop response can minimize or eliminate out of band spurs due to turn on transients that would be problematic for low data rate systems that use lower loop bandwidths.

For this design, the loop bandwidth is set at 50kHz and a type II, 3rd order loop is used to help with suppression of the crystal reference spurs. Please refer to technical article TA0031 in the 1999 RFMD catalog for more information on designing the loop filters. Figure 6 demonstrates the close in phase noise and Figure 7 shows the spurious output. Also seen in Figure 7 are the modulation spurs that result from the counter cycles. The primary source for these modulation spurs are voltage spikes caused by the gates and flip-flops changing states during the carry over which then get coupled into the VCO. Careful isolation and decoupling are needing to the best suppression of these spurs. The modulated signal, shown in Figure 8, shows an occupied bandwidth (99%) of 150kHz for the 72kbps data rate. The loop filter acts as a smoothing filter and helps shape the frequency spectrum even though the input signal is digital. This bandwidth works well with a receiver using low cost 180kHz ceramic IF filters.

The RF2513 transmitter IC has a companion single IC receiver, the RF2917, for low cost FM or FSK simplex links. The RF2917 incorporates the reference oscillator, PLL, VCO, LNA, downconverting mixer, 94dB limiting IF amps, frequency discriminating demodulator, and data slicer in a single chip. With the addition of a few external, discrete components, a complete FSK receiver can be built. One of the features of this part is the differential connection of the demodulator to the data slicer. A DC averaging circuit is not needed, therefore, the response to receiver data is 1 or 2 bit times and a lengthy preamble is not required. This approach is also immune to the low frequency components in the data pattern that plague the DC averaging circuits. This makes it a perfect receiver to complement the DC-accurate modulator. A fully assembled evaluation board for the RF2917 is available with 180kHz IF filters. By using this bandwidth for low data rates, sensitivity is lost due to the increased noise power over the signal power resulting in less than optimum range. The higher bandwidth and larger deviations do not reduce the frequency accuracy needed, thereby allowing lower-cost crystals to be used.

There are a variety of applications that can benefit from this type of modulation. Computer peripherals, for example, tend to send data in bursts with indeterminate pauses in-between. Wireless keyboards, mice and joysticks are migrating from infra-red to RF, but the immunity to random data patterns and pauses is necessary to guarantee reliable operation. It is generally preferred that remote controls for satellite receivers be RF as opposed to infra-red so that the TV does not have to be co-located with the receiver. The range of infra-red remote controls can be augmented by RF repeaters. An IR receiver data output can be used to modulate this RF2513 circuit and an RF2917 receiver data output can be buffered to drive the IR LEDs. Telemetry sensor outputs such as temperature or fluid level can be transmitted directly from the A/D output with this transmitter without concern for the data pattern. This modulator can also be implemented with the RF2905 transceiver IC to create a low cost half duplex two way radio link.

Conclusions

In conclusion, the enticements of low cost single chip solutions get many people entangled by the problems that random data patterns can cause when modulating VCOs. Veteran radio designers are aware of the problem and several methods for working with it. With so many new applications that need low to moderate data rates at a low cost, this modulator provides a low cost, easy to implement alternative to existing schemes. This modulation scheme is being patented and will be incorporated into new IC which can reduce the overall cost of the transmitter even lower.

Copyright 1997-2000 RF Micro Devices, Inc.

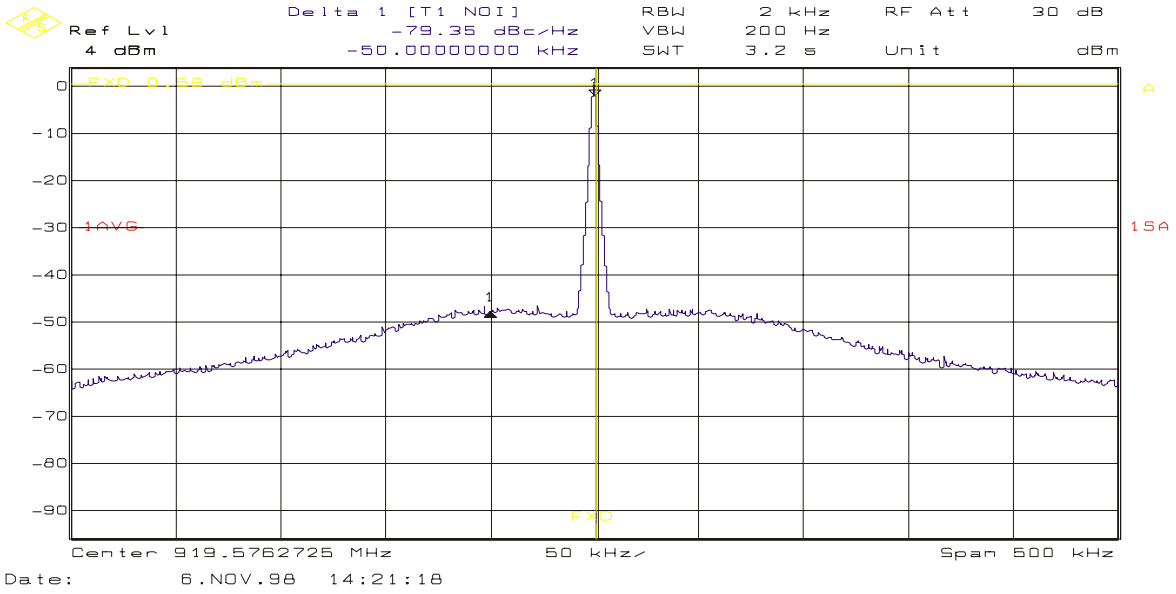

Figure 6. Linear Final Stage RMS Collector Currents for the Two Cases as the Input Signal is Varied

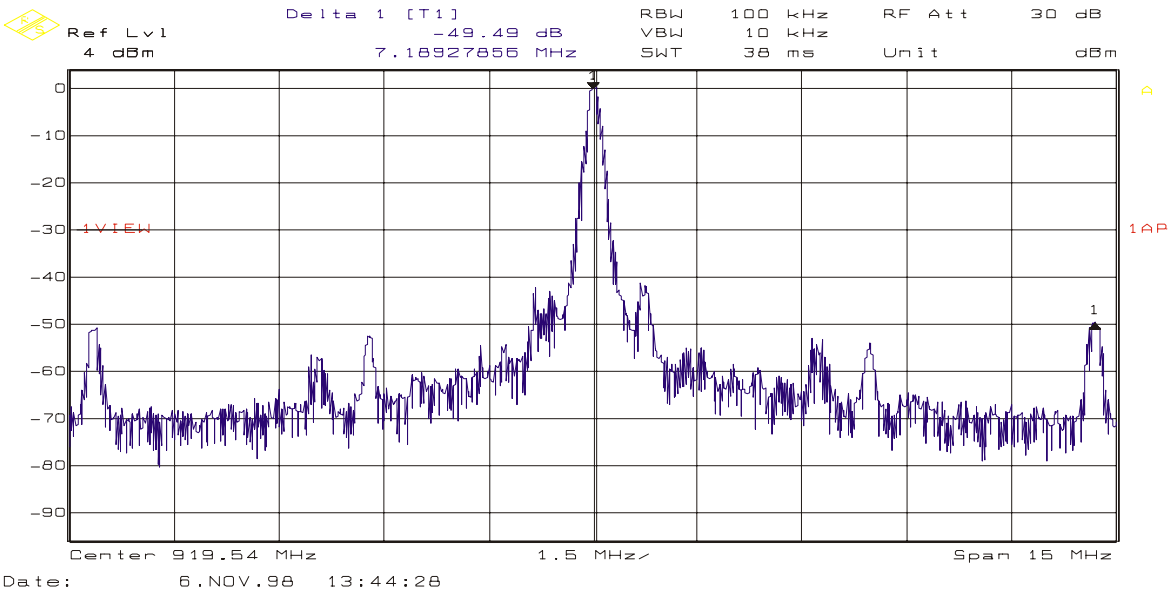

Figure 7. RF2510 Spurious Output with Modulation

Copyright 1997-2000 RF Micro Devices, Inc.

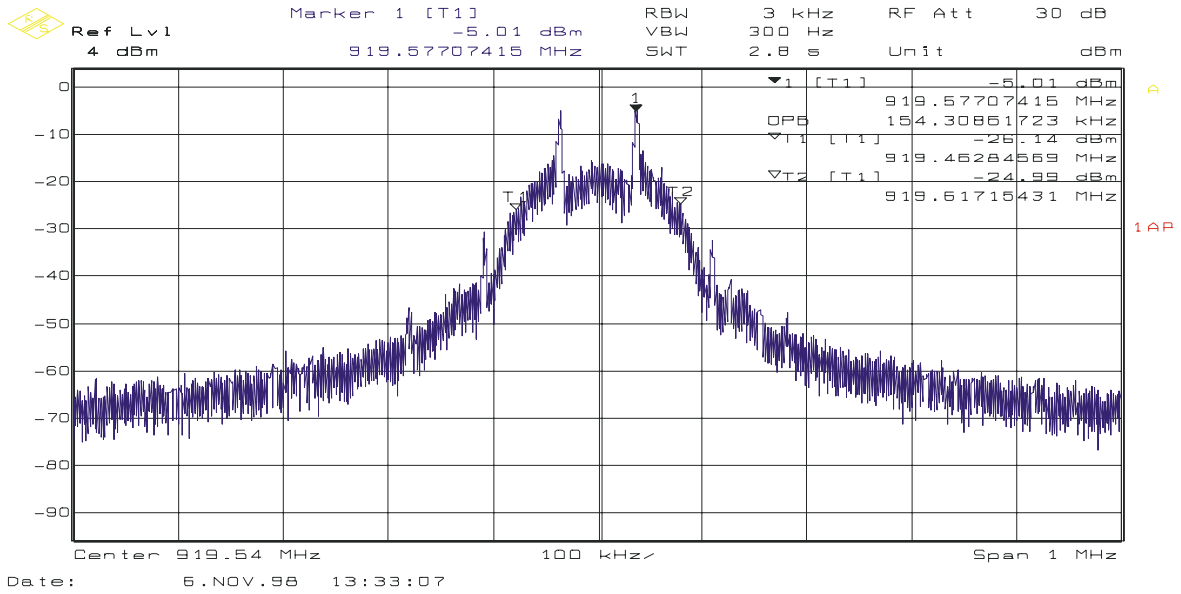

Figure 8. Modulated Spectrum with 72 Kbps Pseudo Random Data

Copyright 1997-2000 RF Micro Devices, Inc.