TA449..W

Asymmetric Thyristor

Replaces March 1998 version, DS4681-4.1

DS4681-5.0 January 2000

APPLICATIONS

- UPS
- Induction Heating
- A.C. Motor Drives
- Switch Mode Power Supplies
- Choppers

KEY PARAMETERS

V_{DRM}	1400V
$I_{T(RMS)}$	400A
I_{TSM}	4000A
dV/dt	1000V/µs
dI/dt	1000A/µs
t_q	10.0µs

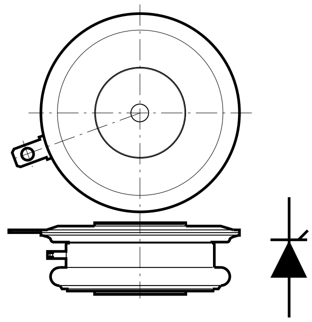
FEATURES

- Low Loss Asymmetrical Diffusion Structure
- Fully Characterised For Operation up to 20kHz
- High dI/dt and dV/dt ratings

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} V	Repetitive Peak Reverse Voltage V_{RRM} V
TA449 14 W	1400	10
TA449 12 W	1200	10
TA449 10 W	1000	10

Lower voltage grades available.



Outline type code: MU86.
See Package Details for further information.

CURRENT AND SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half sine wave, duty cycle 50%, T_{case} = 80°C, T_j = 125°C.	255	A
$I_{T(RMS)}$	RMS value		400	A
I_{TSM}	Surge (non-repetitive) on-state current	T_j = 125°C, t_p = 1ms, V_R = 0	4000	A
I^2t	I^2t for fusing	$t_p \geq$ 10ms	80×10^3	A^2s

THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	dc	-	0.07	°C/W
		Single side cooled	Anode dc	-	0.133	°C/W
			Cathode dc	-	0.154	°C/W
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 5.0kN with mounting compound	Double side	-	0.02	°C/W
			Single side	-	0.04	°C/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	°C
		Reverse (blocking)		-	125	°C
T_{stg}	Storage temperature range			-40	150	°C
-	Clamping force			4.5	5.5	kN

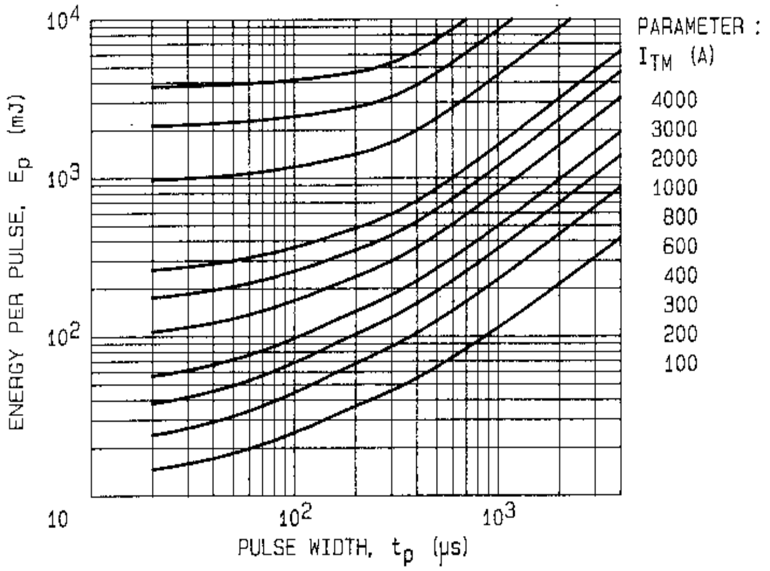
DYNAMIC CHARACTERISTICS

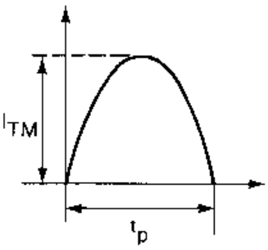
Symbol	Parameter	Conditions		Typ.	Max.	Units
V_{TM}	Maximum on-state voltage	At 600A peak, T_{case} = 125°C		-	2.9	V
I_{RRM}	Peak reverse current	At V_{RRM}, T_{case} = 125°C		-	40	mA
I_{DRM}	Off-state current	At V_{DRM}, T_{case} = 125°C		-	1	mA
dV/dt	Maximum linear rate of rise of off-state voltage	To 60% V_{DRM} T_j = 125°C, Gate open circuit		-	1000	V/µs
dI/dt	Rate of rise of on-state current	Gate source 20V, 20Ω $t_r \leq$ 5µs.	Non-repetitive	-	1000	A/µs
			Repetitive	-	500	A/µs
I_H	Holding current	T_j = 25°C, I_{TM} = 1A, V_D = 12V		-	80	mA
I_L	Latching current	T_j = 25°C, I_G = 0.5A, V_D = 12V		-	300	mA
t_q	Max. turn-off time	VR = DF451 voltage drop, T_j = 125°C, I_{TM} = 200A, dV/dt = 400V/µs (linear to 60% V_{DRM}), tdI_R/dt = 30A/µs Gate open.		-	10	µs
t_{gt}	Typ. turn-on time (total)	T_j = 25°C, I_T = 50A, V_D = 300V, I_G = 1A, dI/dt = 50A/µs, dI_G/dt = 1A/µs		3	-	µs
t_{gd}	Typ. delay time			1.5	-	µs

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{GT}	Gate trigger voltage	V_{DWM} = 12V, R_L = 3Ω, T_{case} = 25ºC	-	5	V
I_{GT}	Gate trigger current	V_{DWM} = 12V, R_L = 3Ω, T_{case} = 25ºC	-	400	mA
V_{GD}	Min. non trigger voltage	-	0.2	-	V
V_{RGM}	Peak reverse gate voltage	-	-	5	V
I_{FGM}	Peak forward gate current	-	-	4	A
P_{GM}	Peak gate power	-	-	16	W
$P_{G(AV)}$	Average gate power	Average time 10ms max	-	3	W

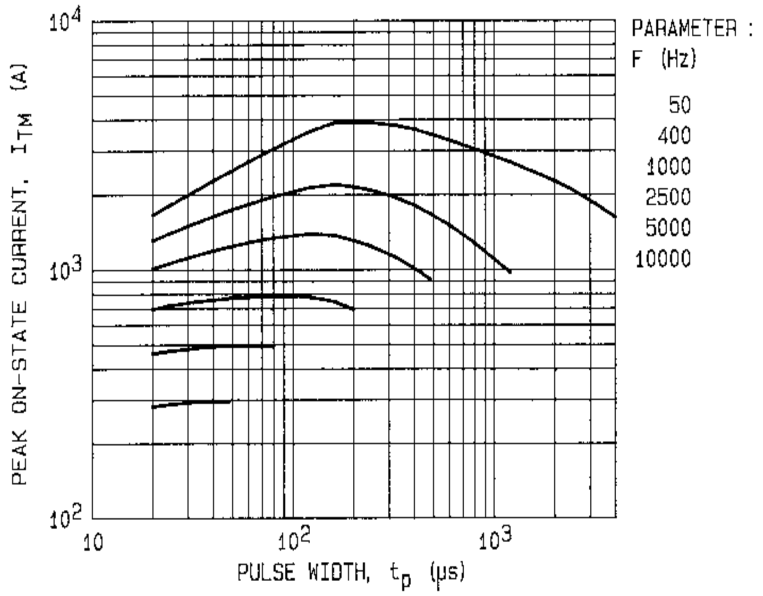
CURVES

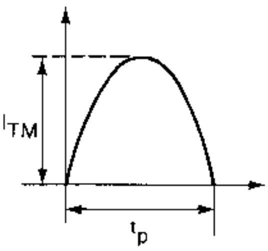




Notes:
1. $V_D \leq 600V$.
2. $V_R \leq 1V$.
3. R.C. snubber. C = 0.22µF, R = 4.7Ω.
4. Double side cooled.

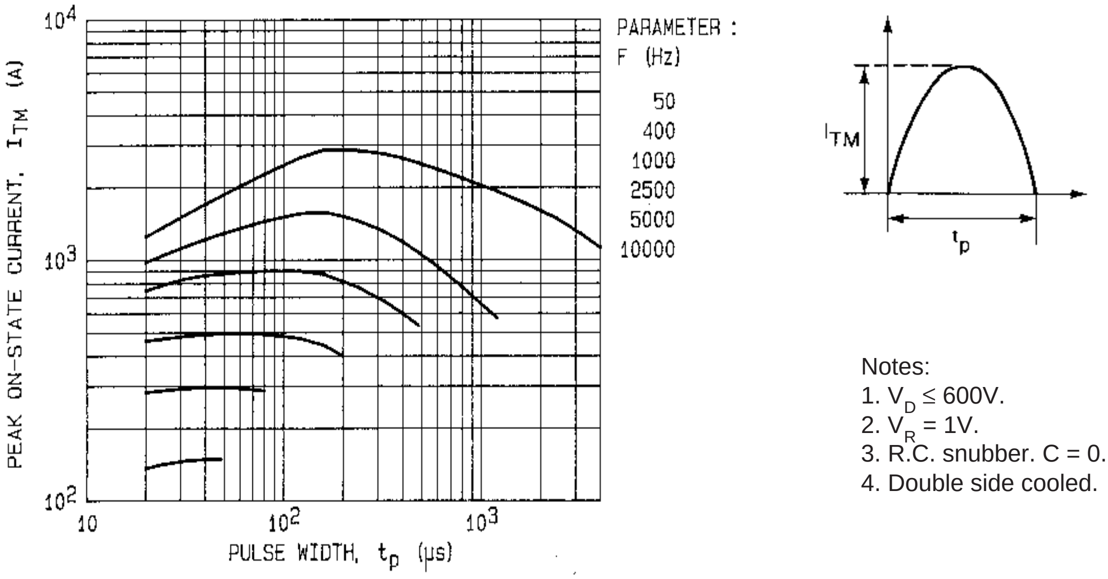
Fig.1 Energy per pulse for sinusoidal pulses.





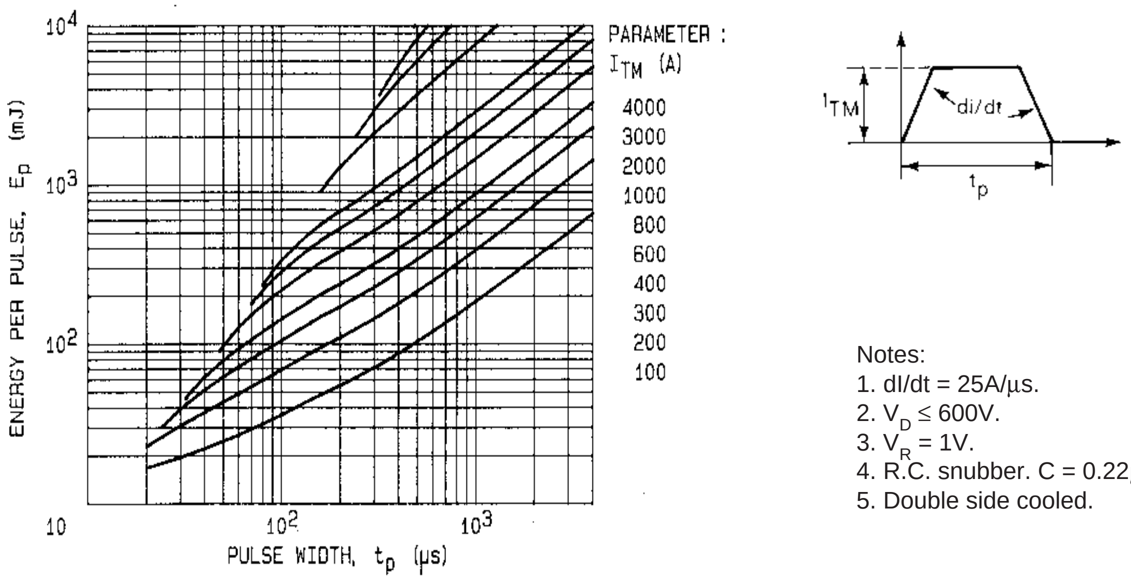
Notes:
1. $V_D \leq 600V$.
2. $V_R = 1V$.
3. R.C. snubber. C = 0.22µF, R = 4.7Ω.
4. Double side cooled.

Fig.2 Maximum allowable peak on-state current vs pulse width for T_{case} = 65°C.



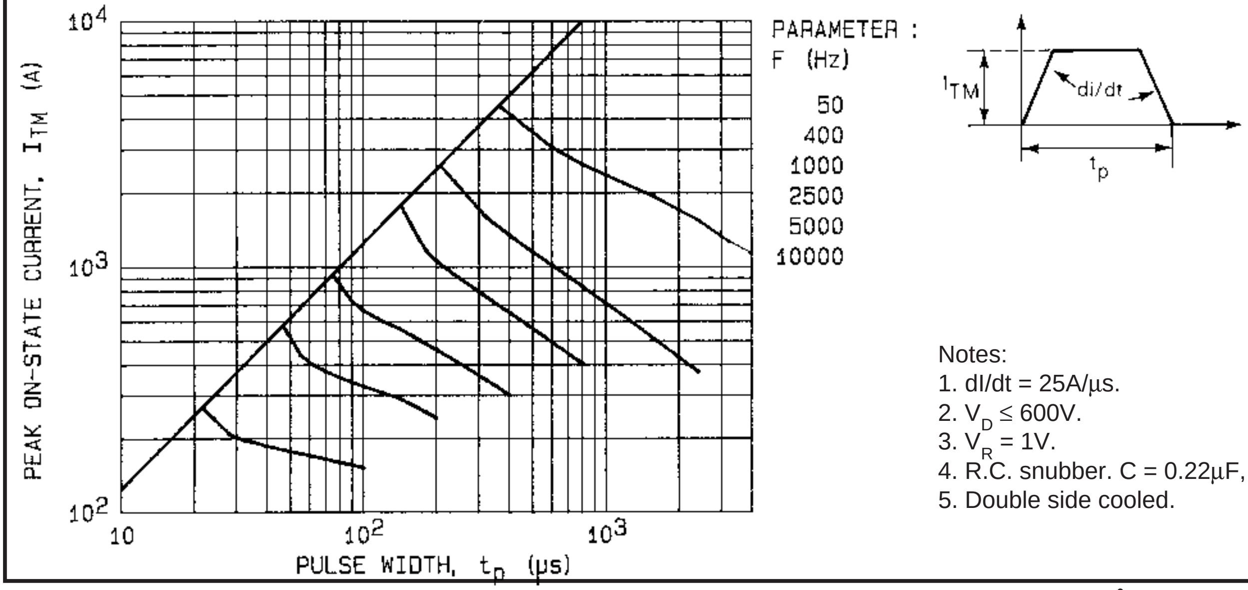
Notes:
1. $V_D \leq 600V$.
2. $V_R = 1V$.
3. R.C. snubber. C = 0.22µF, R = 4.7Ω.
4. Double side cooled.

Fig.3 Maximum allowable peak on-state current vs pulse width for T_{case} = 90˚C.



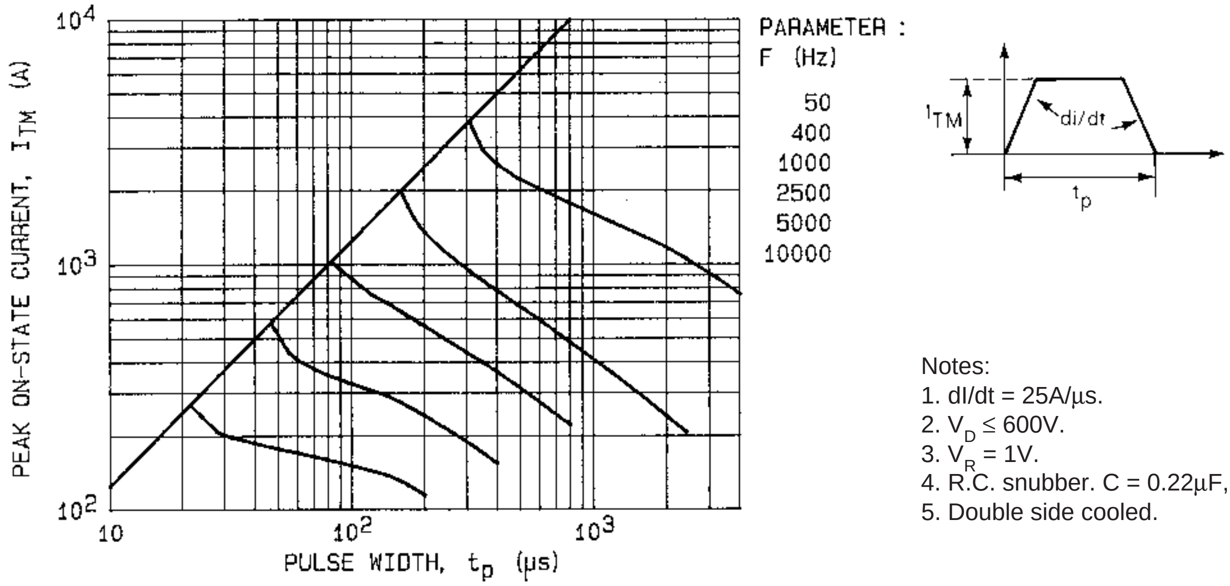
Notes:
1. dI/dt = 25A/µs.
2. $V_D \leq 600V$.
3. $V_R = 1V$.
4. R.C. snubber. C = 0.22µF, R = 4.7Ω.
5. Double side cooled.

Fig.4 Energy per pulse for trapezoidal pulses



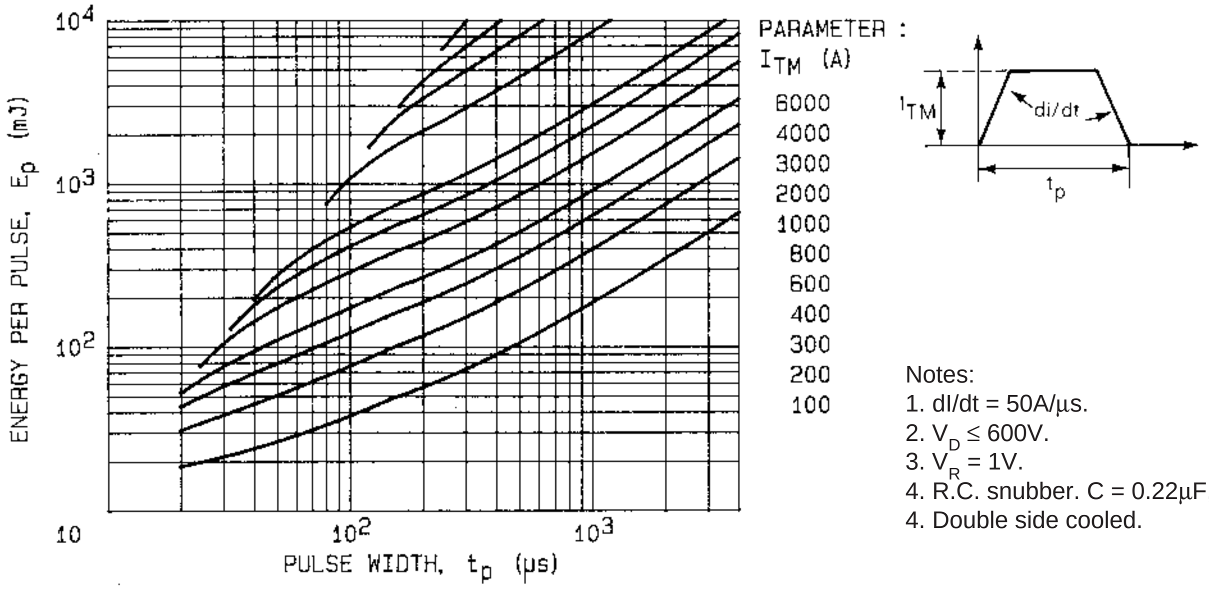
Notes:
1. dI/dt = 25A/µs.
2. $V_D \leq 600V$.
3. $V_R = 1V$.
4. R.C. snubber. C = 0.22µF, R = 4.7Ω.
5. Double side cooled.

Fig.5 Maximum allowable peak on-state current vs pulse width for T_{case} = 65˚C.



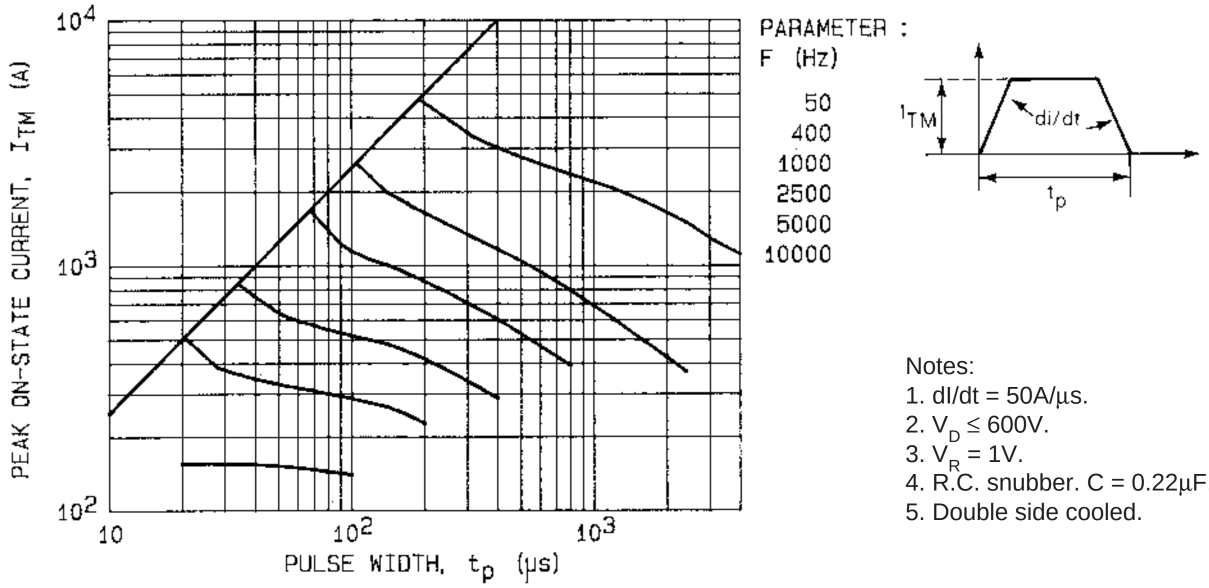
Notes:
1. dI/dt = 25A/µs.
2. $V_D \leq 600V$.
3. $V_R = 1V$.
4. R.C. snubber. C = 0.22µF, R = 4.7Ω.
5. Double side cooled.

Fig.6 Maximum allowable peak on-state current vs pulse width for T_{case} = 90˚C.



Notes:
1. dI/dt = 50A/μs.
2. $V_D \leq 600V$.
3. $V_R = 1V$.
4. R.C. snubber. C = 0.22μF, R = 4.7Ω.
4. Double side cooled.

Fig.7 Energy per pulse for trapezoidal pulses.



Notes:
1. dI/dt = 50A/μs.
2. $V_D \leq 600V$.
3. $V_R = 1V$.
4. R.C. snubber. C = 0.22μF, R = 4.7Ω.
5. Double side cooled.

Fig.6 Maximum allowable peak on-state current vs pulse width for T_{case} = 90˚C.

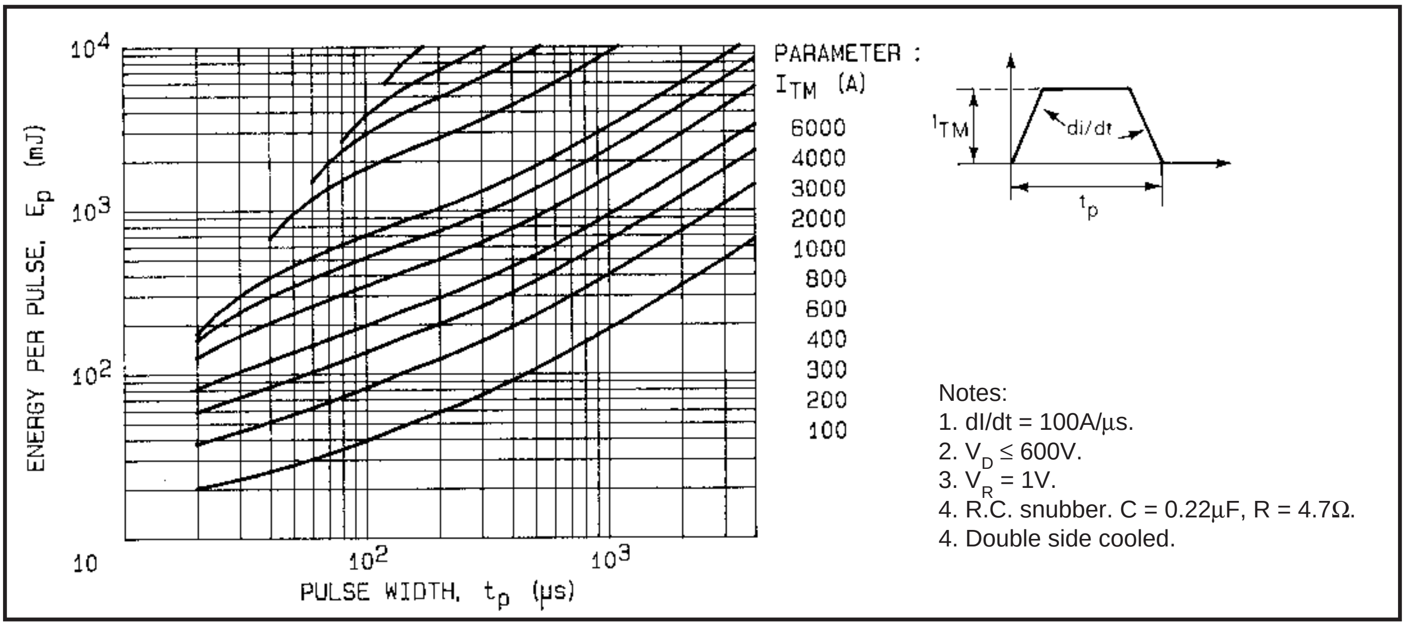


Fig.10 Energy per pulse for trapezoidal pulses.

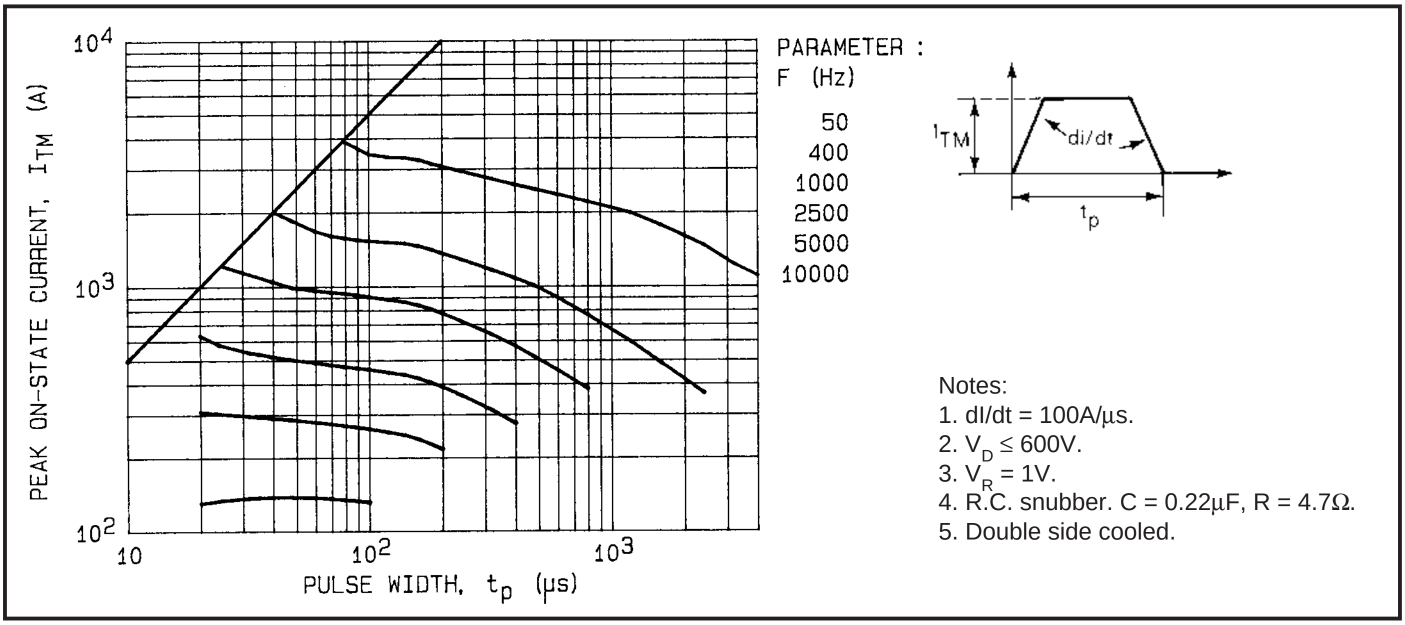


Fig.11 Maximum allowable peak on-state current vs pulse width for T_{case} = 65˚C.

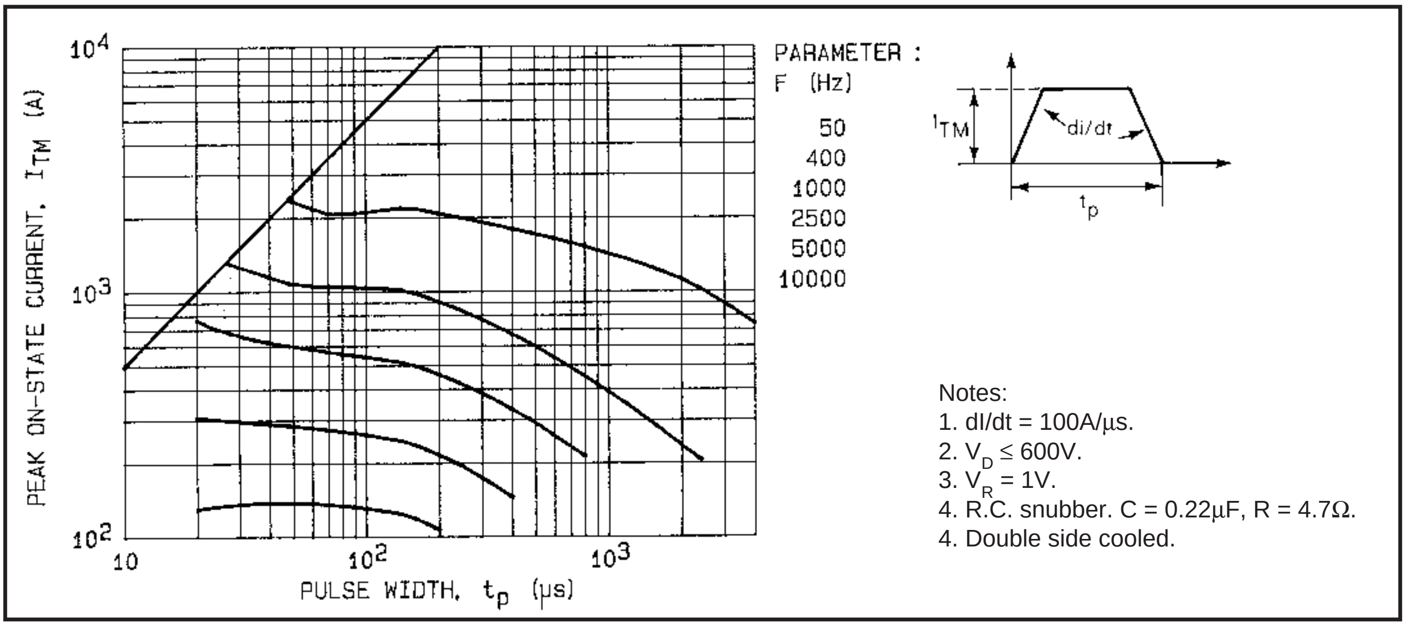


Fig.12 Maximum allowable peak on-state current vs pulse width for T_{case} = 90˚C.

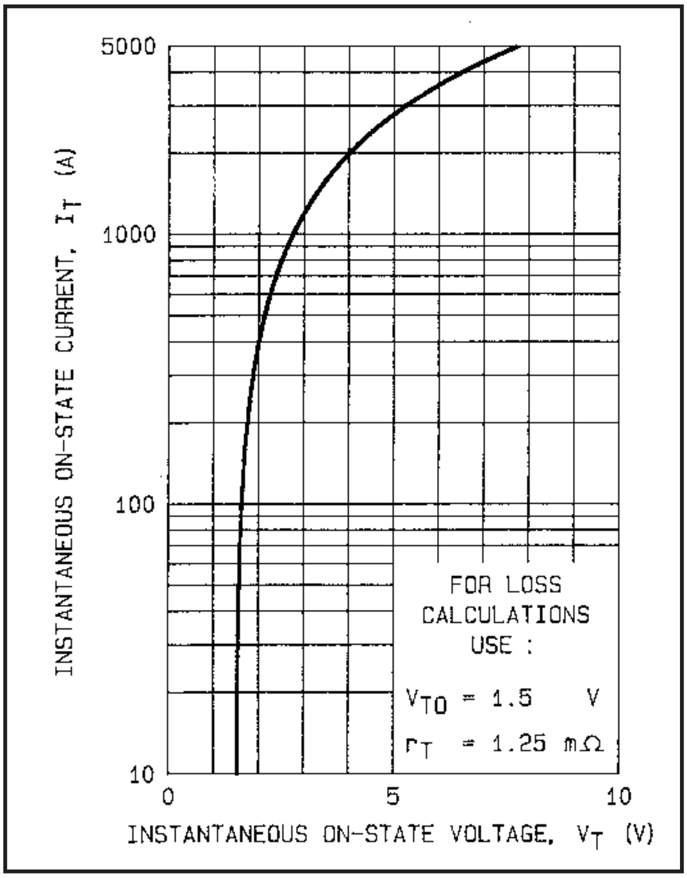


Fig.13 Maximum on-state conduction characteristic (T_j = 125˚C)

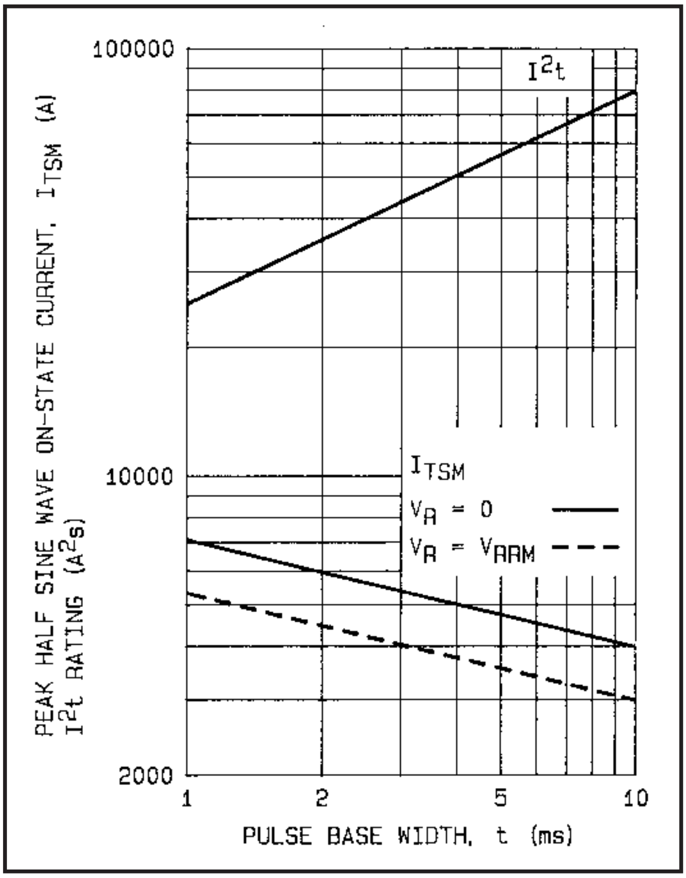


Fig.14 Non-repetitove sub-cycle surge on-state current and I^2t rating. (Initial T_j = 125˚C)

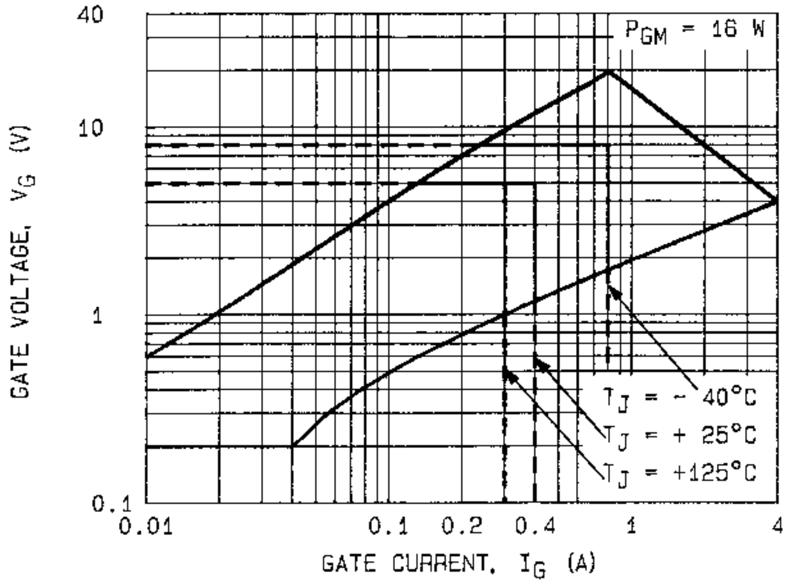


Fig.15 Gate trigger characteristics

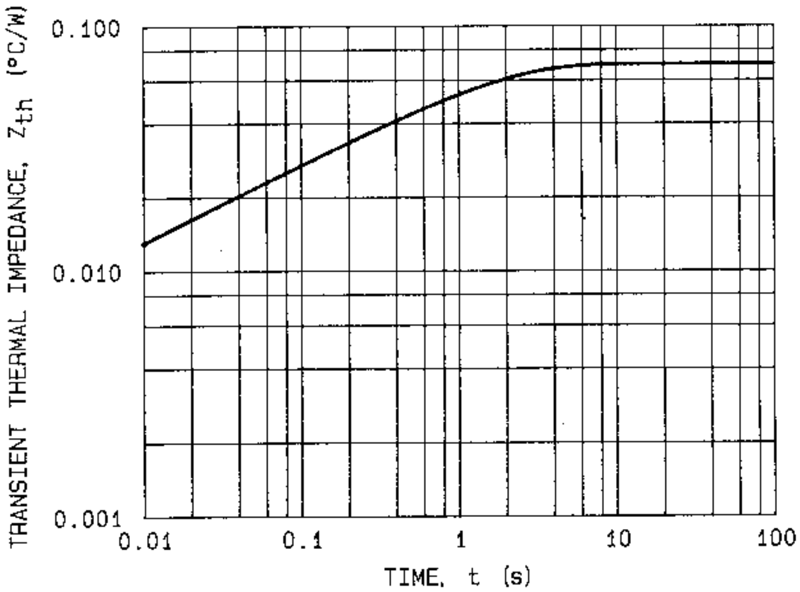
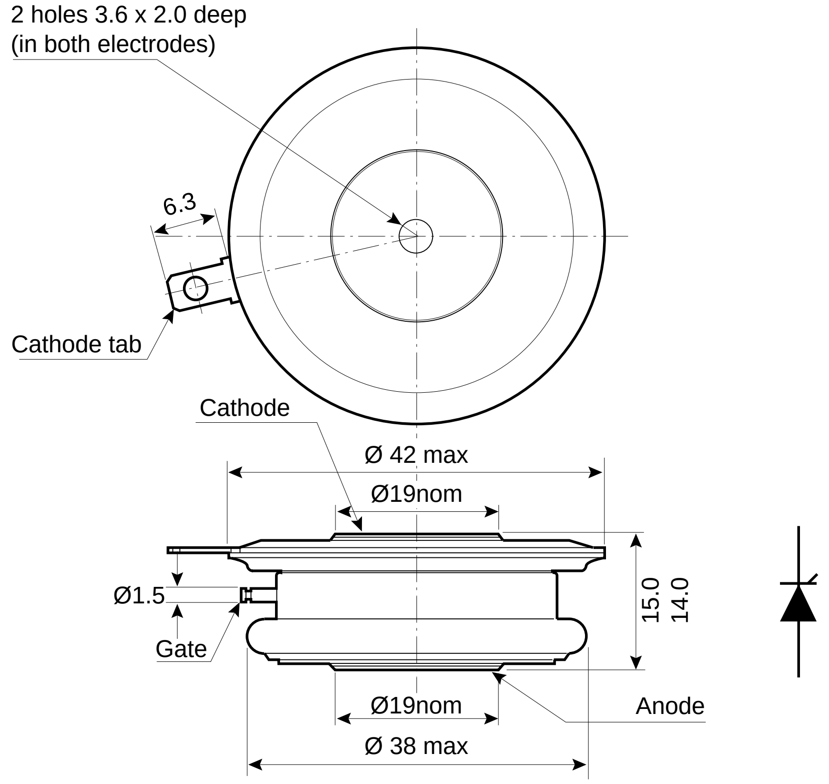


Fig.16 Transient thermal impedance - junction to case (double side cooled)

PACKAGE DETAILS

For further package information, please contact your local Customer Service Centre. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Nominal weight: 50g
Clamping force: 3.5kN ±10%
Lead length: 250mm

Package outine type code: MU86

ASSOCIATED PUBLICATIONS

Title	Application Note Number
Calculating the junction temperature or power semiconductors	AN4506
Gate triggering and the use of gate characteristics	AN4840
Recommendations for clamping power semiconductors	AN4839
The effect of temperature on thyristor performance	AN4870
Thyristor and diode measurement with a multi-meter	AN4853
Turn-on performance of thyristors in parallel	AN4999
Use of V_{TO}, r_T on-state characteristic	AN5001

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink / clamping systems in line with advances in device types and the voltage and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group continues to offer high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the up to date CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete solution (PACs).

DEVICE CLAMPS

Disc devices require the correct clamping force to ensure their safe operation. The PACs range offers a varied selection of pre-loaded clamps to suit all of our manufactured devices. This include cube clamps for single side cooling of ‘T’ 22mm

Clamps are available for single or double side cooling, with high insulation versions for high voltage assemblies.

Please refer to our application note on device clamping, AN4839

HEATSINKS

Power Assembly has it’s own proprietary range of extruded aluminium heatsinks. They have been designed to optimise the performance or our semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest Sales Representative or the factory.

DYNEX SEMICONDUCTOR

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Target Information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.

Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand.

No Annotation: The product parameters are fixed and the product is available to datasheet specification.