



TOSHIBA Bi-CMOS Constant Current Interface Driver

TB62706BN/BF

16 Bit Constant Current LED Driver with Shift Register and Latch Functions

Product Description:

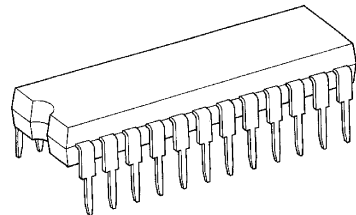
The TB62706BN/BF is specifically designed for LED display applications. The Bi-CMOS device has 16 Bi-polar constant current output channels and includes CMOS shift register and latch functions.

The LED drive current is programmed by the installation of a single resistor per device. Current is programmable from 5-90mA and is held constant across all 16 outputs effectively compensating for the inherent circuit and component variables which affect the brightness of the LEDs.

Features:

- 16 Constant Current Output Channels
- Current Programmable from 5-90mA
- 5V CMOS Compatible Inputs
- 15MHz Max Clock Frequency (Cascade)

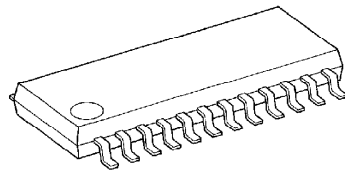
TB62706BN



SDIP24-P-300

Weight: 1.22g(typ)

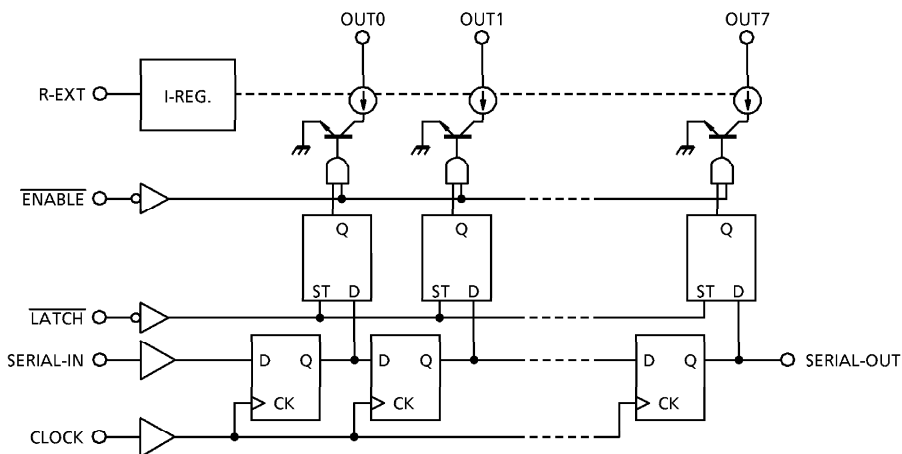
TB62706BF



SSOP24-P-300B

Weight: 0.32g(typ)

Block Diagram:



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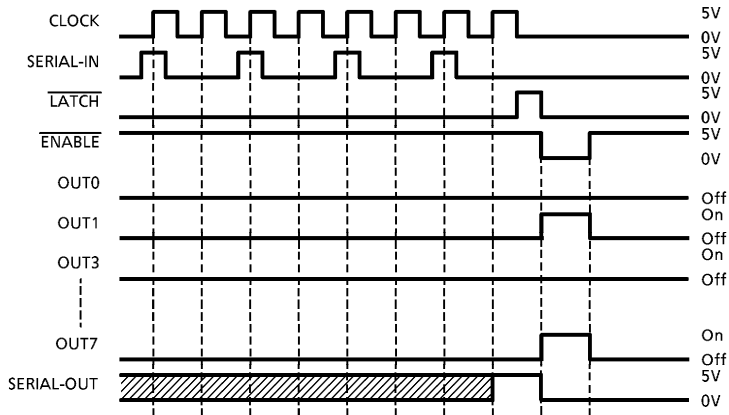
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Timing Diagram:



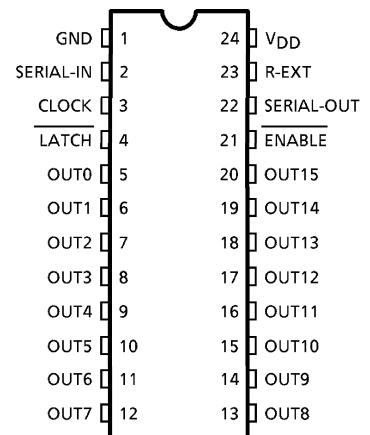
Latches are:

1. Level Sensitive
2. Not edge sensitive
3. Not clock synchronous
4. Passing Data when $\overline{\text{LATCH}}$ is H
5. Hold Data when $\overline{\text{LATCH}}$ is L

All Outputs are OFF when $\overline{\text{ENABLE}}$ is H and ON when $\overline{\text{ENABLE}}$ is L.

Terminal Description & Pin Out:

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal of a serial-data for shift-register
3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	$\overline{\text{LATCH}}$	Input terminal of a data strobe. Latches passes data with "H" level input of $\overline{\text{LATCH}}$ -terminal, and hold data with "L" level input.
5-20	$\overline{\text{OUT0-15}}$	Output terminals
21	$\overline{\text{ENABLE}}$	Input terminal of output enable. All outputs (OUT-15) do off with "H" level input of $\overline{\text{ENABLE}}$ -terminal, and do on with "L" level input.
22	SERIAL-OUT	Output terminal of a serial-data for next SERIAL-IN terminal.
23	R-EXT	Input terminal of connects with a resistor for to set up all output current.
24	VDD	5V Supply voltage terminal



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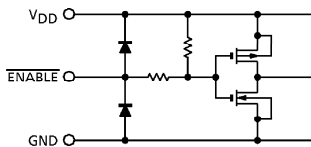
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Truth Table:

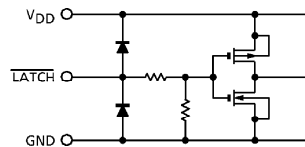
CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0	OUT5	OUT7	SERIAL-OUT
UP	H	L	Dn	Dn	Dn-7	Dn-15	Dn-15
UP	L	L	Dn+1	No Change			Dn-14
UP	H	L	Dn+2	Dn+2	Dn-5	Dn-13	Dn-13
DOWN	X	L	Dn+3	Dn+2	Dn-5	Dn-13	Dn-13
DOWN	X	H	DN+3	Off			Dn-13

Equivalent Circuit of Inputs and Outputs:

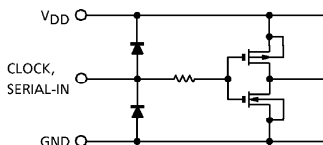
1. $\overline{\text{ENABLE}}$ terminal



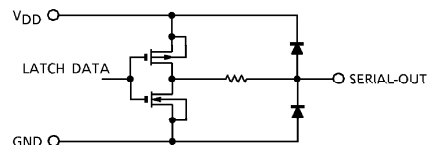
2. $\overline{\text{LATCH}}$ terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



Maximum Ratings:

CHARACTER	SYMBOL	RATING	UNIT
Supply Voltage	VDD	0~7.0	V
Input Voltage	VIN	-0.4~VDD + 0.4	V
Output Current	IOUT	+90	mA
Output Voltage	VOUT	-0.5~+17.0	V
Clock Frequency	FCLK	15	MHz
GND Terminal Current	IGND	1440	mA
Power Dissipation	PD	1.78 (BN type: ON PCB, Ta=25°C)	W
		1.00 (BF type: ON PCB, Ta=25°C)	
Thermal Resistance	Rth(j-a)	70 (BN type: On PCB)	°C/W
		120 (BF type: On PCB)	
Operating Temperature	Topr	-40~+85	°C
Storage Temperature	Tstg	-55~+150	°C

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Recommended Operating Condition:

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	—	4.5	5.0	5.5	V
Output Voltage	VOUT	—	—	—	15.0	V
Output Current	IOUT	DC 1 Circuit	5	—	88	mA
	IOH	SERIAL-OUT	—	—	1.0	mA
	IOL	SERIAL-OUT	—	—	-1.0	mA
Input Voltage	VIH	—	0.7VDD	—	VDD+0.3	V
	VIL	—	-0.3	—	0.3VDD	
LATCH Pulse Width	tw LAT	VDD=4.5 ~ 5.5V	100	—	—	ns
CLOCK Pulse Width	tw CLK		50	—	—	ns
ENABLE Pulse Width	tw EN		4500	—	—	ns
Set-up Time for DATA	tsetup(D)		60	—	—	ns
Hold Time for Data	tthold(D)		20	—	—	ns
Set-up Time for LATCH	tsetup(L)		100	—	—	ns
Hold Time for ENABLE	tthold(L)		60	—	—	ns
Clock Frequency	FCLK	Cascade Operation	—	—	10.0	MHz
Power Dissipation	PD	Ta=85°C (BN type)	—	—	0.92	W
		Ta=85°C (BF type)	—	—	0.50	

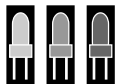


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Electrical Characteristics:

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" level	VIH	—	Ta = -40~85°C		0.7VDD	—	VDD	V
	"L" level	VIL	—	Ta = -40~85°C		GND	—	0.3VDD	
Output Leakage Current		IOH	—	VOH=15.0V		—	—	10	μA
Output Voltage	SERIAL-- OUT	VOL	—	IOL=+1.0mA		—	—	0.4	V
		VOH	—	IOH=-1.0mA		4.6	—	—	V
Output Current 1		IOL1	—	VCE=0.7V	REXT=470Ω (include Current Matching)	34.1	40.0	45.9	mA
		IOL2	—	VCE=0.4V		33.7	39.5	45.3	
Current Skew		dIOL1	—	IO=40mA, VCE=0.4V	REXT=470Ω	—	±1.5	±6.0	%
Output Current 2		IOL3	—	VCE=0.7V	REXT=250Ω (include Current Matching)	64.2	75.5	86.8	mA
		IOL4	—	VCE=0.4V		63.8	75.0	86.2	
Current Skew		dIOL2	—	IO=75mA, VCE=0.7V	REXT=250Ω	—	1.5	6.0	%
Supply Voltage Regulation		% / VDD	—	REXT=470Ω	Ta = -40~+85°C	—	±1.5	±5.0	% / V
Pull Up Resistor		RIN(up)	—	—		150	300	600	KΩ
Pull-down Resistor		RIN(down)	—	—		100	200	400	KΩ
Supply Current	"OFF"	IIDD (off) 1	—	REXT=OPEN	OUT~8=off	—	0.6	1.2	mA
		IIDD (off) 2	—	REXT=470Ω	OUT~8=off	3.5	5.8	8	
		IIDD (off) 3	—	REXT=250Ω	OUT~8=off	6.5	10.2	15	
	"ON"	IIDD (on)1	—	REXT=470Ω	OUT~8=on	10	16	22	
		IIDD (on)2	—	REXT=250Ω	OUT~8=on	18	28.3	38.5	



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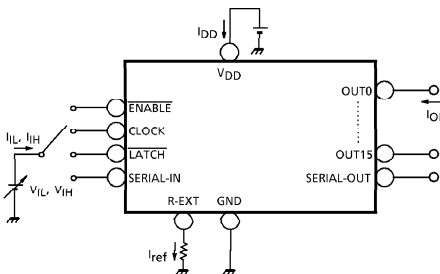


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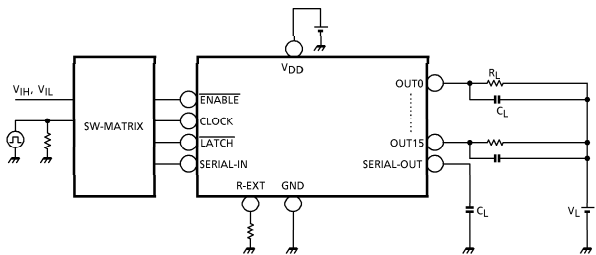
Switching Characteristics:

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CLK-OUTn	tpLH	—	VDD = 5.0V VCE = 0.4V VIH = VDD VIL = GND REXT = 470Ω VL = 3.0V RL = 65Ω CL = 10.5pF	—	1200	1500	ns
	LATCH-OUTn				—	1200	1500	ns
	ENABLE-OUTn				—	1200	1500	ns
	CLK-SOUT				—	30	70	ns
Propagation Delay Time ("H" to "L")	CLK-OUTn	tpHL	—		—	700	1000	ns
	LATCH-OUTn				—	700	1000	ns
	ENABLE-OUTn				—	700	1000	ns
	CLK-SOUT				—	30	70	ns
Pulse Width	CLK	tw CLK,CLK	—		—	20	30	ns
	LATCH	tw LAT,LAT	—		—	10	25	ns
Set-up Time for Latch	L-H	tsetup LAT	—		—	25	50	ns
	H-L		—		—	25	50	ns
Hold Time for LATCH	L-H	thold LAT	—	—	0	15	ns	
	H-L		—	—	0	15	ns	
Maximum CLOCK Rise Time		tr	—	—	—	10	μs	
Maximum CLOCK Fall Time		tf	—	—	—	10	μs	
Output Rise Time		tor	—	—	150	300	600	ns
Output Fall Time		tof	—	—	150	300	600	ns

DC Characteristic Test Circuit:



AC Characteristic Test Circuit:



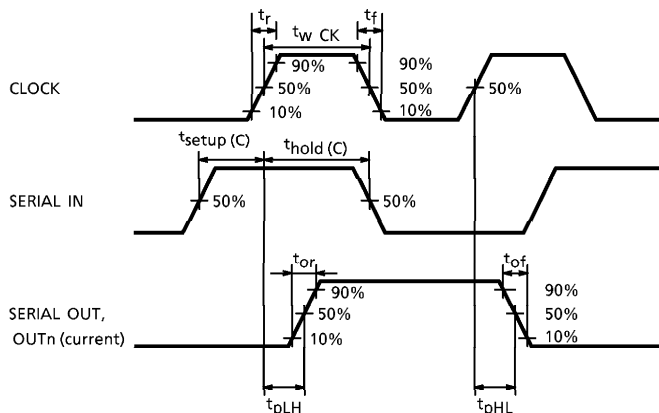


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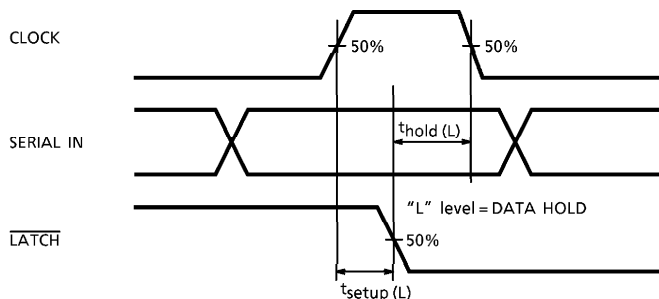
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Timing Wave Form:

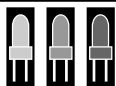
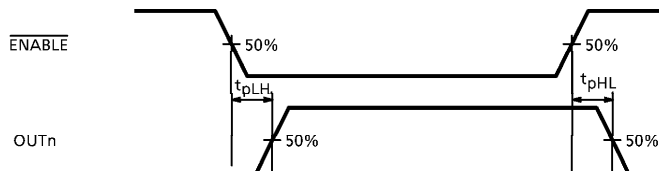
1. CLOCK-SERIAL OUT, OUTn



2. CLOCK-LATCH



3. ENABLE-OUTn



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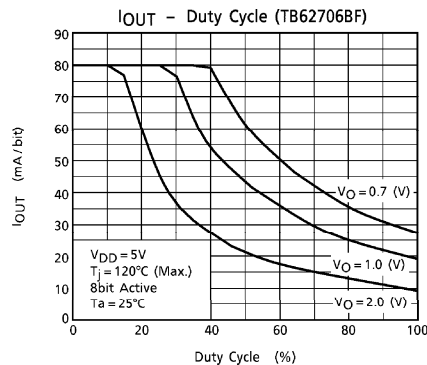
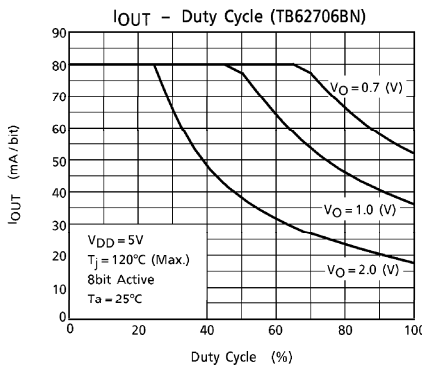
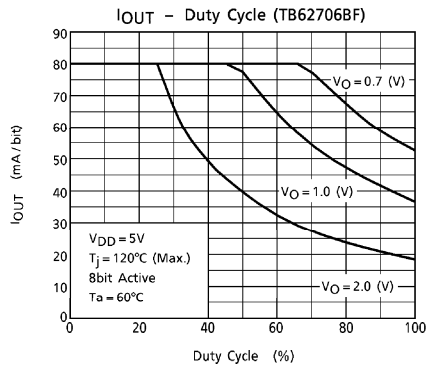
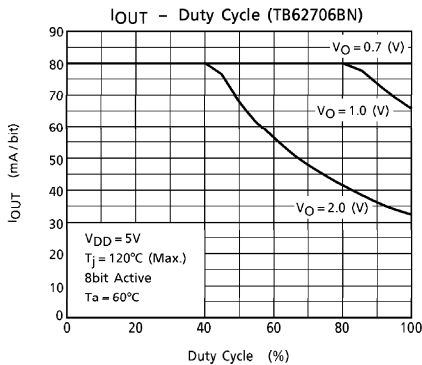
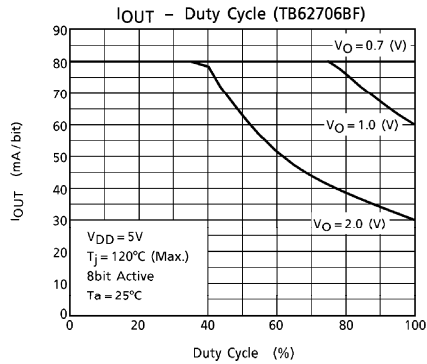
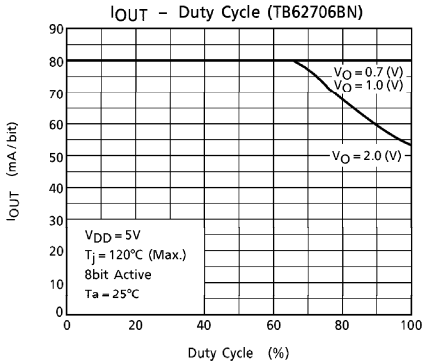
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Graphs:

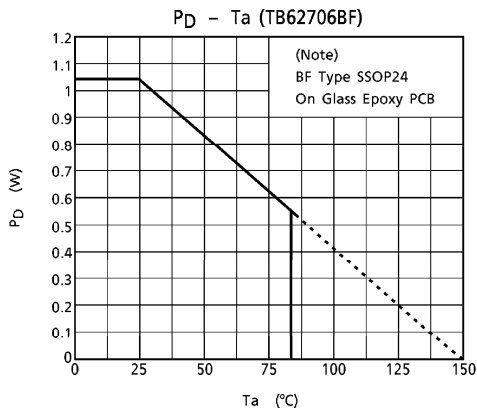
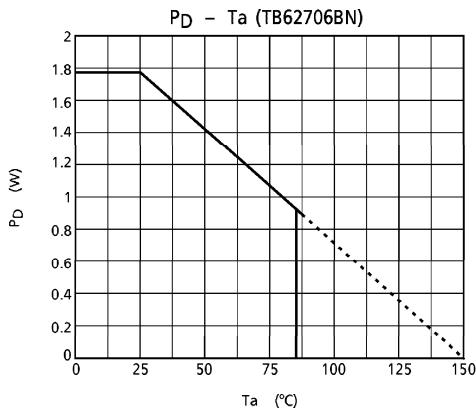




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Graphs:



Current Programming Resistor Selection:

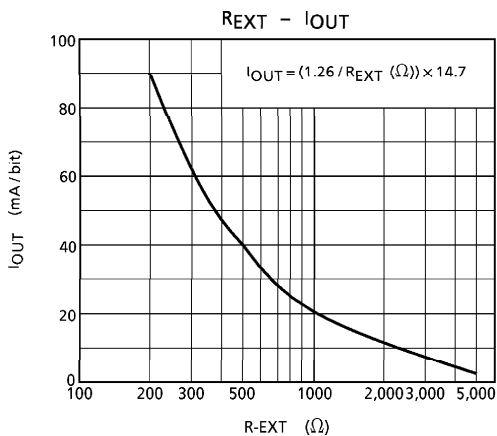
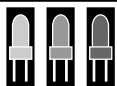


Fig. 1



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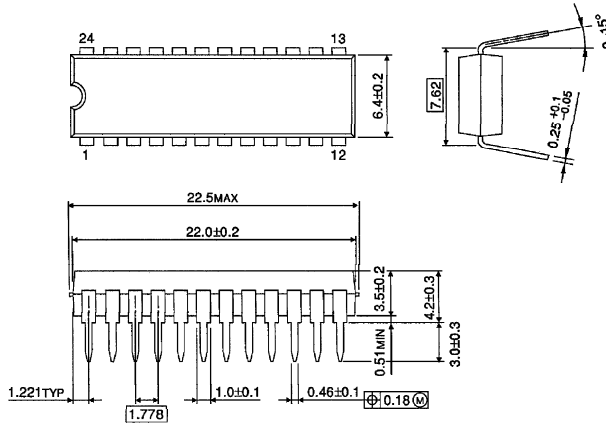


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Outline Drawings:

SDIP24-P-300-1.78

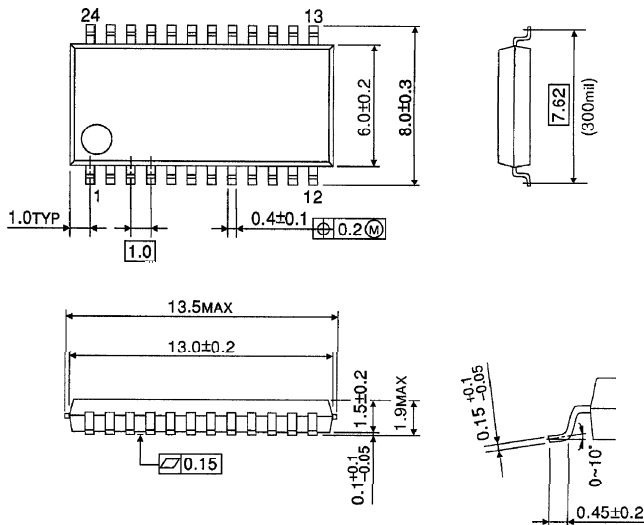
Unit : mm



Weight : 1.22g (Typ.)

SSOP24-P-300-1.008

Unit : mm



Weight : 0.32g (Typ.)



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All specifications subject to change.