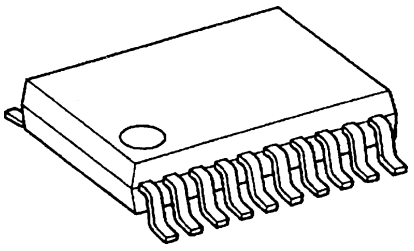
TOSHIBA Bi-CMOS
Constant Current Interface Driver

TB62715F/FN

8 Bit Constant Current LED Source Driver with Shift Register and Latch Functions

TB62715F/FN



Weight: 0.14g (typ)

Product Description:

The TB62715F/FN are specifically designed for LED display applications. The Bi-CMOS device has 8 Bipolar constant current output source channels and includes CMOS shift register and latch functions.

The LED drive current is programmed by the installation of a single resistor per device. Current is programmable from 2-150mA and is held constant across all 8 source outputs effectively compensating for the inherent circuit and component variables which affect the brightness of the LEDs.

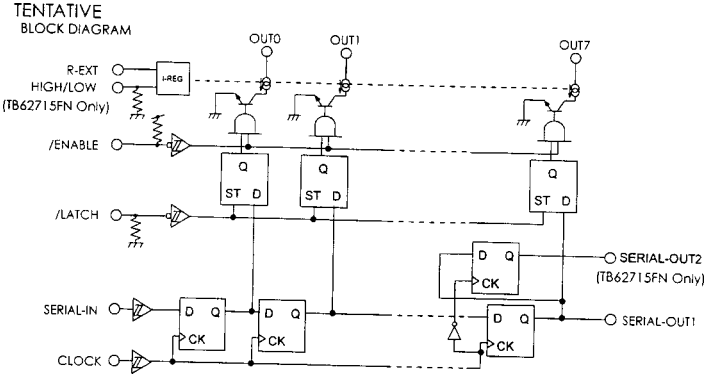
Features:

- Current Source Device
- 8 Constant Current Output Channels
- Current Programmable from 2-150mA
  - F type - 70mA max
  - FN type - 150mA max
- 5V CMOS Compatible Inputs
- 15Mhz max Clock Frequency

Constant Output Current Matching:

High/Low Terminal	OUT-GND Voltage	Current Skew (BIT)	Current Skew (LOT)	Output Current
"L"	≥ 0.4[V]	± 6.0 [%]	±15.0 [%]	2~70[mA]
"H"	≥ 1.0[V]			50~150[mA]
TB67215F Only	≥ 0.4[V]			2~70[mA]

Block Diagram:



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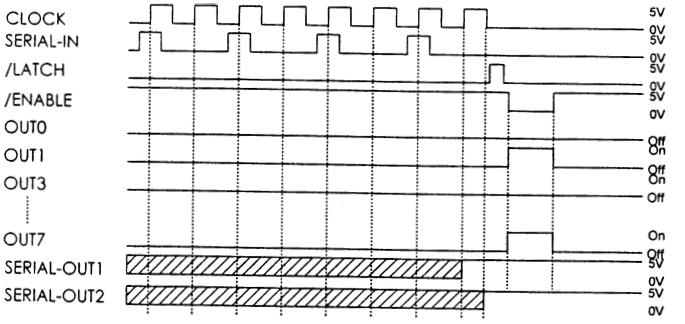
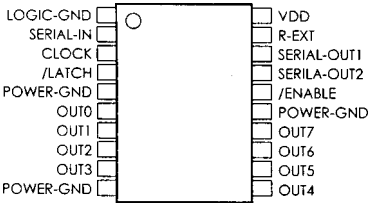
Timing Diagram:

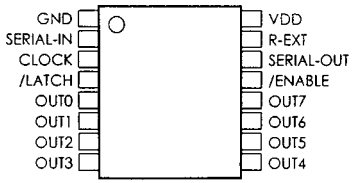


note) Latches are level sensitive,not rising edge sensitive and not syncronus CLOCK.
Input of LATCH-terminal to H level, data passes latches,and input to L level,data hold latches.
Input of ENABLE-terminal to H level,all output (OUT0~7) do off.

Terminal Description & Pin Out:

PIN No.		PIN NAME	FUNCTION
SSOP20	SSOP16		
5	—	HIGH/LOW	Use Current Select.
6, 15	—	POWER-GND	GND terminal for control output
1	1	LOGIC-GND	GND terminal for control logic
2	2	SERIAL-IN	Input terminal of a serial-data for shift-register
3	3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	4	/LATCH	Input terminal of a data strobe. Latches passes data with "H" level input of LATCH-terminal, and hold data with "L" level input.
7~10, 11~14	5~12	OUT0~7	Output terminals.
16	13	/ENABLE	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of ENABLE-terminal, and do on with "L" level input.
18	14	SERIAL-OUT1	Output terminal of a serial-data for next SERIAL-IN terminal.
17	—	SERIAL-OUT2	
19	15	R-EXT	Input terminal of connects with a resister for to set up all output current.
20	16	VDD	5V Supply voltage terminal



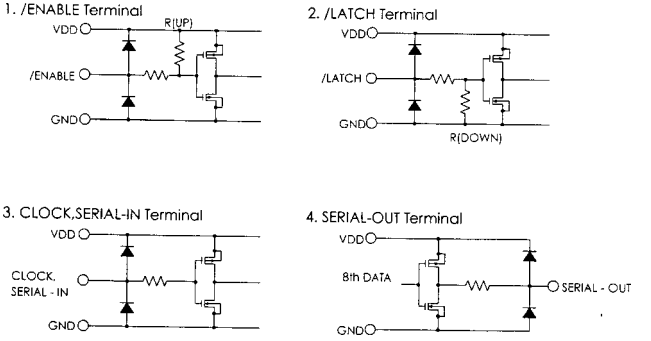


TB62715F/FN

Truth Table:

CLOCK	/LATCH	/ENABLE	SERIAL-IN	OUT0	OUT3	OUT7	SERIAL-OUT
UP	H	L	Dn	Dn	Dn-5	Dn-7	Dn-7
UP	L	L	Dn+1	No Change (data hold)			Dn-6
UP	H	L	Dn+2	Dn+2	Dn-3	Dn-5	Dn-5
DOWN	X	L	Dn+3	Dn+2	Dn-3	Dn-5	Dn-5
DOWN	X	H	Dn+3	Off			Dn-5

Equivalent Circuit of Inputs and Outputs:



Maximum Ratings:

CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	VDD	0 ~ +7.0	V
Input Voltage	VIN	-0.4 ~ VDD +0.4	V
Output Current	IOUT	+150 (High/Low="H")	mA/ch
		+70 (High/Low="L")	
		+70 (TB62715F Only)	
Output Voltage	VCEO	-0.5 ~ +17.0	V
Clock Frequency	FCK	15.0	MHz
Power Dissipation	Pd1	0.71 (FREE AIR) / 0.96 (On PCB)	W
	Pd2	0.37 (FREE AIR) / 0.78 (On PCB)	
Thermal Resistance	Rth(j-a)1	175 (FREE AIR) / 130 (On PCB)	°C/W
	Rth(j-a)2	330 (FREE AIR) / 160 (On PCB)	
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-55 ~+150	°C

NOTE:
F type: Ambient temperature delated above 25°C in the proportion of 7.69mW/°C (On PCB)
FN type: Ambient temperature delated above 25°C in the proportion of 6.25mW/°C (On PCB)

TB62715F/FN

Recommended Operating Condition:

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD		4.5	5.0	5.5	V
Outout Voltage	VOUT		—	—	15	V
Output Current	IOUT1	DC 1 Circuit	50	—	130	mA/ch
	IOUT2	DC 1 Circuit	2	—	60	
	IOH	SERIAL-OUT1,2	—	—	-1.0	mA
	IOL	SERIAL-OUT1,2	—	—	1.0	
Input Voltage	VIH	VDD=4.5 ~ 5.5V	0.7VDD	—	VDD+0.3	V
	VIL		-0.3	—	0.3VDD	
LATCH Pulse Width	tw LAT		100	—	—	ns
CLOCK Pulse Width	tw CLK		50	—	—	
ENABLE Pulse Width	tw EN		1000	—	—	
Set-up Time for DATA	tsetup(D)		—	—	25	
Hold Time for Data	thold(D)		—	—	20	
Set-up Time for LATCH	tsetup(L)		—	—	50	
Hold Time for LATCH	thold(L)		—	—	40	
Clock Frequency	fCLK	Cascade Operation	10.0	—	—	
Power Dissipation	Pd1	FN type: Ta=85°C	—	—	0.50	W
	Pd2	F type: Ta=85°C	—	—	0.40	

TB62715F/FN

Electrical Characteristics:

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" level	VIH	—	—		0.7VDD	—	VDD	V
	"L" level	VIL	—	—		GND	—	0.3VDD	
Output Leakage Current		I LEAK	—	VOH=15.0V		—	—	10	μA
Output Voltage	SERIAL-OUT 1,2	VOL	—	IOL=+1.0mA		—	—	0.4	V
		VOH		IOH=-1.0mA		4.6	—	—	V
Output Current 1	Current Skew	IOL1	—	VCE=0.4V REXT=470Ω	F-Type and High/Low="L"	31.8	37.5	43.1	mA
		dIOL1	—			—	±1.5	±6.0	%
Output Current 2	Current Skew	IOL2	—	VCE=1.0V REXT=160Ω	High/Low="H"	103.7	122.0	140.3	mA
		dIOL2	—			—	±1.5	±6.0	%
Supply Voltage Regulation		% / VDD	—	REXT=160Ω Ta=40~+85°C		—	±1.5	±5.0	% /V
Pull Up Resistor		RIN(up)	—	—		150	300	600	kΩ
Pull Down Resistor		RIN(down)	—	—		100	200	400	kΩ
Supply Current	VDD	IDD (off)1	—	REXT=OPEN	OUT1~8=off	—	1.0	2.0	mA
		IDD (off)2	—	REXT=500Ω	OUT1~8=off	—	5.8	8.0	
		IDD (off)3	—	REXT=160Ω,	OUT1~8=off	—	16.1	21.4	
	VCC	IDD (on)1	—	REXT=500Ω,	OUT1~8=off	—	12.7	20.0	
		IDD (on)2	—	REXT=160Ω,	OUT1~8=on	—	32.5	49.1	

(VLED=17V, VDD=5V, Ta=25ºC unless otherwise noted.)

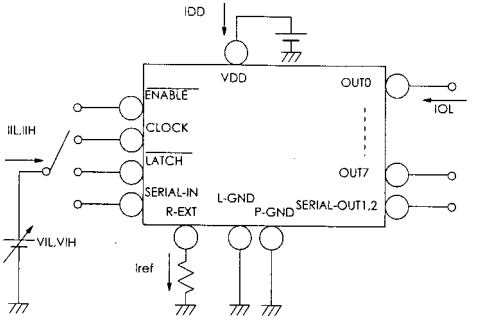
TB62715F/FN

Switching Characteristics:

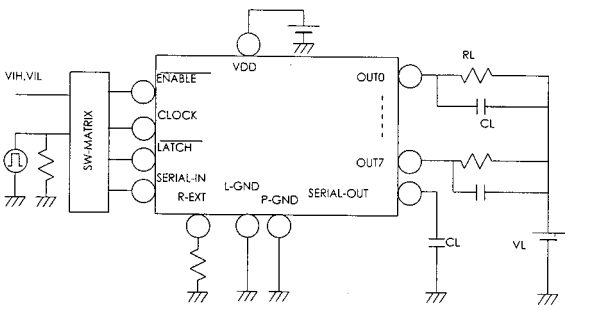
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CLK-OUTn	tpLH	—	VDD = 5.0V VCE = 1.0V VIH = VDD VIL = GND REXT = 160Ω IOUT=125mA VL=3.0V RL = 32Ω CL = 10.5pF tor : 10% to 90% tof : 90% 10% tpLH : 50% to 10% tpHL : 50% to 90%	—	800	1200	ns
	LATCH-OUTn				—	800	1200	ns
	ENABLE-OUTn				—	800	1200	ns
	CLK-SOUT				—	35	40	ns
Propagation Delay Time ("H" to "L")	INn-OUTn	tpHL	—		—	500	750	ns
	LATCH-OUTn				—	500	750	ns
	ENABLE-OUTn				—	500	750	ns
	CLK-SOUT				—	35	40	ns
Pulse Width	CLK	tw CLK,CLK	—		—	20	30	ns
	LATCH	tw LAT,LAT	—		—	10	20	ns
Set-up Time for LATCH/SIN	L-H	tsetup LAT/SIN	—		—	10	20	ns
	H-L		—		—	10	20	ns
Hold Time for LATCH/SIN	L-H	thold LAT/SIN	—		—	0	15	ns
	H-L		—		—	0	15	ns
Maximum CLOCK Rise Time		tr	—		—	—	10	μs
Maximum CLOCK Fall Time		tf	—		—	—	10	μs
Output Rise Time		tor	—		300	600	1000	ns
Output Fall Time		tof	—		300	600	1000	ns

(Ta=25ºC unless otherwise noted)

DC Characteristic Test Circuit:

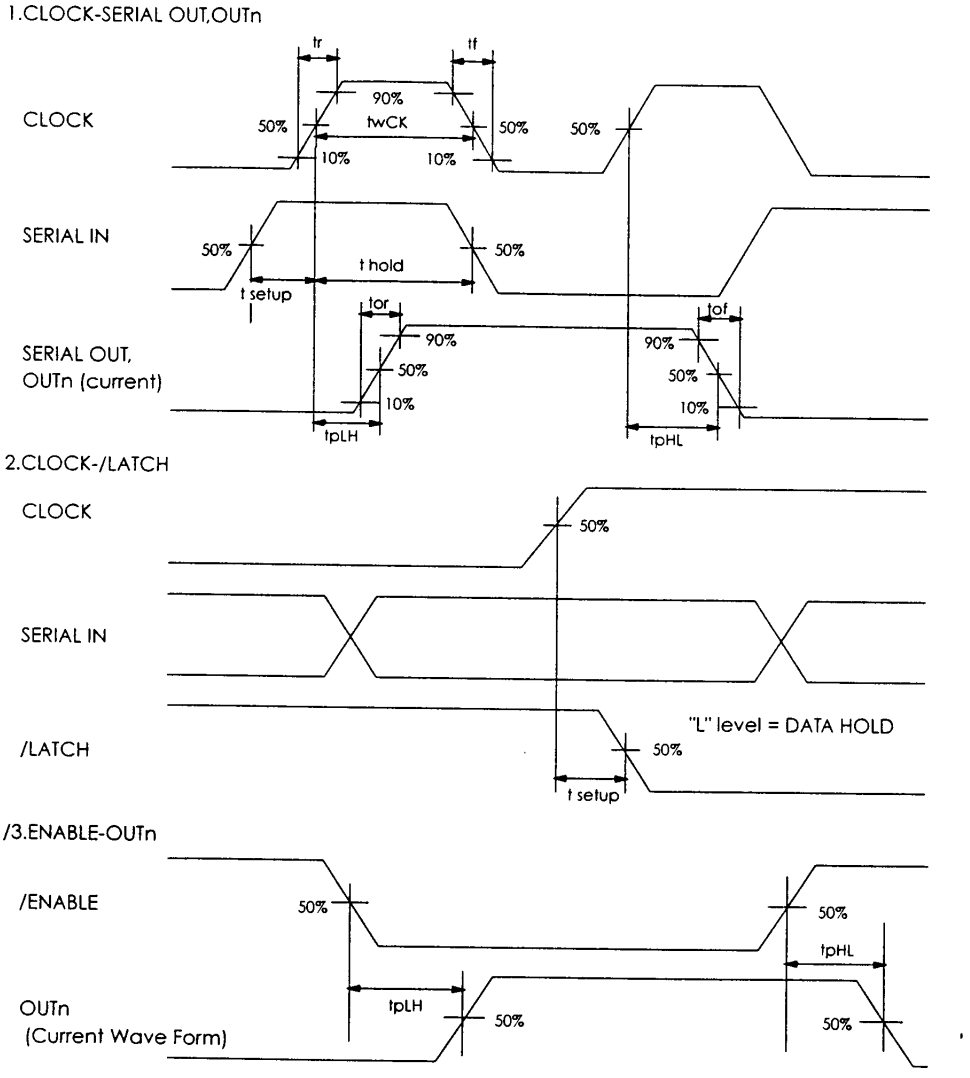


AC Characteristic Test Circuit:



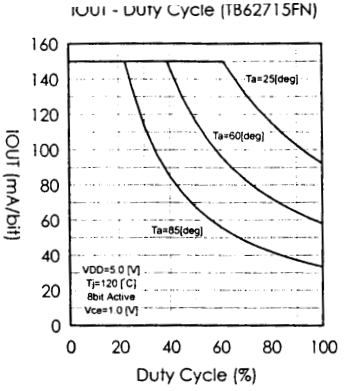
TB62715F/FN

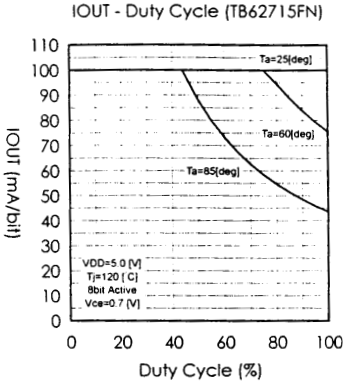
Timing Wave Form:

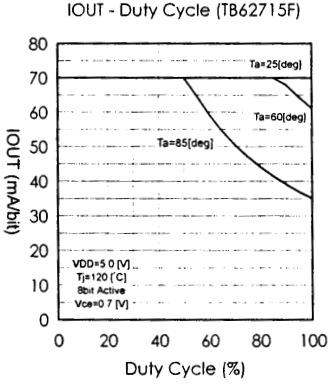


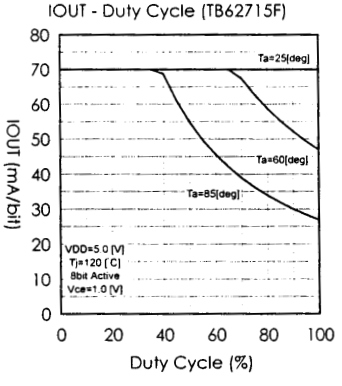
TB62715F/FN

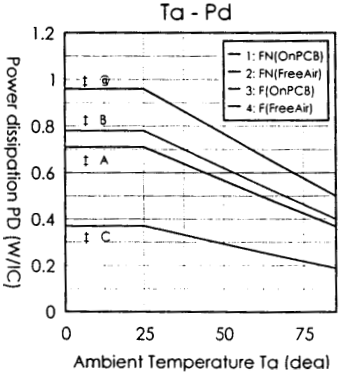
Graphs:





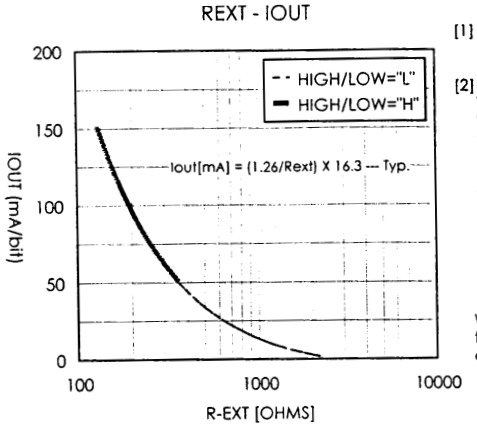






TB62715F/FN

Application Circuit:

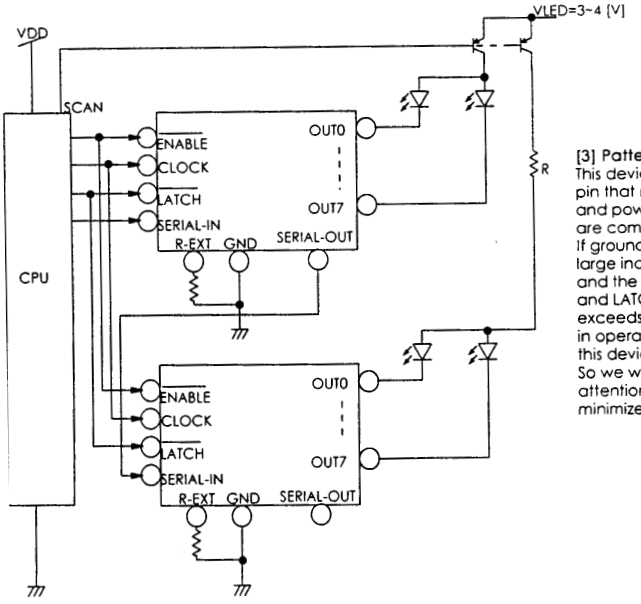


[1] Output Current (Iout)
Iout is set by the enternal resistor (R-EXT) as shown in FIG-1.

[2] Total Supply Voltage (VLED)
This device can opperate 0.7~1.0V(VO).
When a higher voltage is input to the devide, the excess voltage is consumed inside the device, that leads to power dissipation.
In order to monimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

VLED (total supply voltage)
= VCE (Tr Vsat) + Vf (LED Forward voltage)
+ VO (IC suuply voltage)

When the total supply is too high considering the power dissipation of this devide, an additional R can decreace the supply voltage(VO).

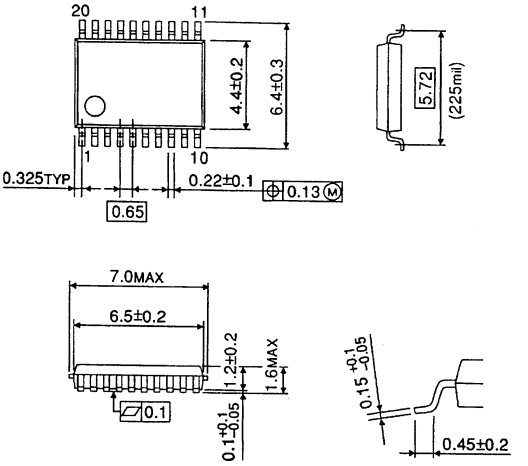


[3] Pattern Layout
This device owns only one ground pin that means signal ground pin and power ground pin are common.
If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH,CLOCK terminals exceeds 2.5V by switching noise in operation, this device may miss-operate.
So we would lile you to pay attention to pattern layout to minimize inductance.

TB62715F/FN

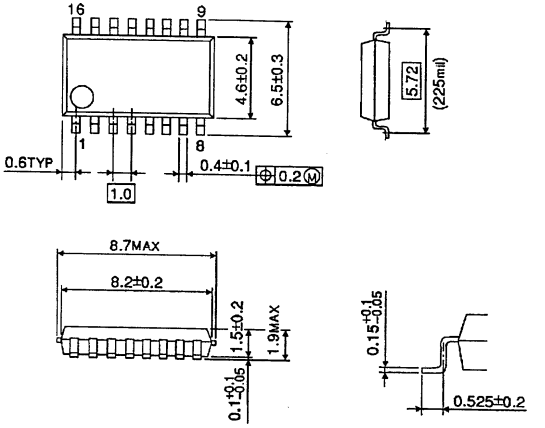
Outline Drawing:

SSOP20-P-225-0.65 Unit: [mm]



Outline Drawing:

SSOP16-P-225-1.00 Unit: [mm]



質量：0.14g (標準)