TBA 540

REFERENCE COMBINATION

The TBA540 is an integrated reference oscillator circuit for colour television receivers incorporating an automatic phase and amplitude controlled oscillator employing a quartz crystal, together with a half-line frequency synchronous demodulator circuit. The latter compares the phases and amplitude of the swinging burst ripple and the PAL flip-flop waveform, and generates appropriate ACC, colour killer and identification signals. The use of synchronous demodulation for these functions permits a high standard of noise immunity.

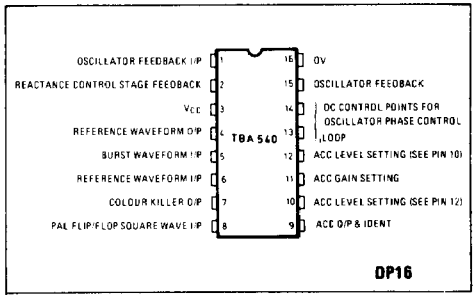

Fig. 1 Pin connections

QUICK REFERENCE DATA

- Supply Voltage, V_{3-16} : 12V (Nom.)
- Total Current Drain, I_3 : 38mA (Typ.)
- R-Y Ref. Output, V_{4-16} : 1.4Vpp (Typ.)
- Colour Killer Output, V_{7-16}
  Colour ON : 12V (Typ.)
  Colour OFF: 250mV (Max.)
- ACC Output Voltage, V_{9-16} :–
  at Correct Phase of PAL Switch : +0.2 to +4V
  at Incorrect Phase of PAL Switch : +4 to +11V

ABSOLUTE MAXIMUM RATINGS

Voltages are referred to pin 16

Electrical

Supply voltage V_3 (V_{CC})	13.2V
Total power dissipation at T_{amb} = +60°C	700 mW
Surge current, minimum duty cycle 10:1, I_{7max}	50mA

Temperature

Storage temperature, T_{stg}	–55°C to +125°C
Operating temperature, T_{amb}	–10°C to +60°C

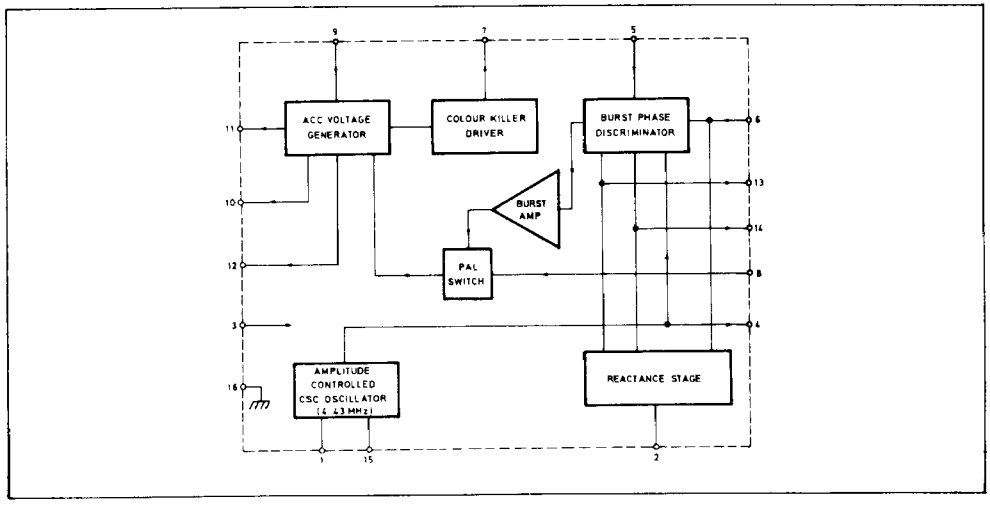

Fig. 2 TBA540 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
V_{CC} (V_3) = +12V, T_{amb} = +25°C, V_5 = 1.5Vp-p burst, V_8 = 2.5Vp-p PAL square wave.
Voltages referred to pin 16

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Output Signals						
B-Y reference signal output	4	1	1.4	2	Vp-p	
Colour killer output	7					
colour 'on'			12		V	
colour 'off'			100	250	mV	
ACC output signal range	9					
at correct phase of PAL switch			+4 to +0.2		V	
at incorrect phase of PAL switch			+4 to +11		V	
Oscillator Section (Amplifier)						
Input resistance	15		3.5		kΩ	
Input capacitance	15		5		pF	
Voltage gain, $G_{15\text{-}1}$	15-1		4.7			
Reactance Control Section						
Voltage gain, $G_{15\text{-}2}$	15-2		1.3			Pins 13 and 14 interconnected
Rate of change of gain with phase difference between burst and reference signal, $\frac{\Delta G_{15\text{-}2}}{\Delta\phi 5\text{-}4}$	15-2		5		rad^{-1}	

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Oscillator Feedback Output

The crystal receives its energy from this pin. The output impedance is approximately 2kΩ in parallel with 5pF.

2. Reactance Control Stage Feedback

This pin is fed internally with a sinewave derived from the reference output (pin 4) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12V Supply

The maximum voltage must not exceed 13.2V.

4. Reference Waveform Output

This pin is driven internally by the regenerated subcarrier waveform in B-Y phase. (The output is in B-Y rather than R-Y phase as the burst phase network produces a lag of 90° of the burst applied to pin 5.) An output amplitude of nominally 1.4V peak-to-peak is produced at low impedance. No DC load to earth is required. A DC connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (-)B-Y)) to that on pin 4. A centre tap on the inductor, connected to earth via a DC blocking capacitor, is therefore necessary.

5. Burst Waveform Input

A burst waveform amplitude of 1.5V peak-to-peak is required to be AC coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the ACC circuit. The input impedance at this pin is approximately 1kΩ and a threshold level of 0.7V must be exceeded before the burst signal becomes effective. A DC bias of 400mV is internally derived for pin 5.

The absolute level of the tip of the burst at pin 5 will normally reach 1.5V.

6. Reference Waveform Input

This pin requires a reference waveform in the -(B-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A DC connection between pins 4 and 6 must be made via the transformer.

7. Colour Killer Output

This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typically 10kΩ) connected to +12V. The unkilled and killed voltages on this pin are then +12V and <250mV respectively. (The voltage range on pin 9 over which switching of the colour killed output on pin 7 occurs is nominally +2.5V.)

8. PAL Flip-Flop Square Wave Input

A 2.5V peak-to-peak square wave derived from the PAL flip-flop (in the TBA520 or TBA990 demodulator IC) is required at this pin, AC – coupled via a capacitor. The input impedance is about 3.3kΩ.

9. ACC Output

An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero burst input signal the DC potential produced at pin 9 is set to be +4V (RV1). The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the PAL flip-flop is identified to be in the correct phase. The range of potential over which full ACC control is exercised at pin 9 is determined by the control characteristic of the ACC amplifier, i.e., for the TBA560 from 0.8 to 1V. The potential on pin 9 will fall to a value within this range as the burst input signal is stabilised to an amplitude of 1.5V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the PAL flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a PAL switch cut-off function in the TBA520 demodulator IC.

10. ACC Level Setting

The network connected between pins 10 and 12 balances the ACC circuit and RV1 is adjusted to give +4V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. ACC Gain Control

RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5V peak-to-peak) under ACC control.

12. See Pin 10.

13. See Pin 14.

14. DC Control Points in Reference Control Loop

Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purpose of DC balancing of the reactance stage and the connection of the bandwidth-determining filter network. Two 2% tolerance 10k resistors with the addition of a 270Ω resistor at pin 13 are used in place of the previous balancing network. The 270Ω resistor may be modified according to the nature of the noise that appears at pin 5.

The filter network consists of R2, C2, C3 and C4. The DC potentials on these pins are nominally +6V.

15. Oscillator Feedback

The input impedance at this pin is nominally 3.5kΩ in parallel with 5pF. No DC connection is required on this pin. The voltage gain in the IC between pins 15 and 1 is nominally 4.7 times.

16. Negative Supply (earth).

OPERATING NOTES

Performance and Comments

Initial adjustment

(a) Remove burst signal.
(b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1.
(c) Set the ACC level adjustment RV1, to give +4V on pin 9. Remove short circuit.
(d) Apply burst signal.
(e) Adjust ACC gain, RV2, to give a burst amplitude of 1.5V peak-to-peak on pin 5.

Phase lock loop performance (with crystal type 4322 152 0110)

(a) Phase difference between reference and burst signals for ±400Hz deviation of crystal frequency, ±10°.
(b) Typical holding range, ±600Hz. (c)
(c) Typical pull-in range ±300Hz.
(d) Temperature coefficient of oscillator frequency, only 2Hz/°C maximum.

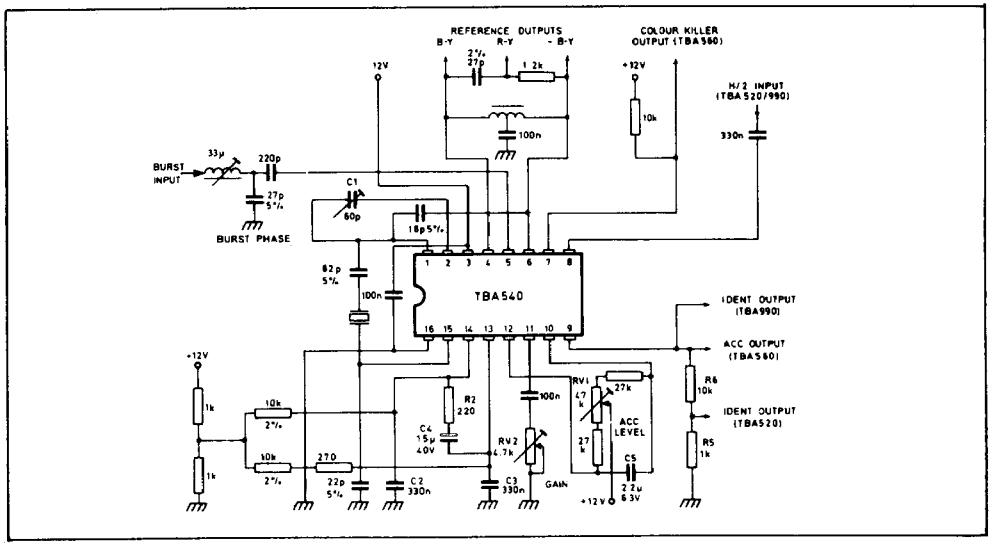

Fig. 3 Typical application diagram