



TC2000

STEREO CLASS-T™ AUDIO CONTROLLER USING DIGITAL POWER PROCESSING (DPP™) TECHNOLOGY

Technical Information

Revision 1.1 – December 2003

GENERAL DESCRIPTION

The TC2000 is a two channel audio controller that uses Tripath's proprietary Digital Power Processing (DPP™) technology. When combined with switching power output stages, the TC2000 allows the implementation of a complete Class-T audio amplifier. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

APPLICATIONS

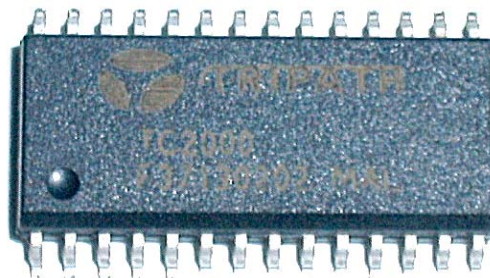
- 5.1-Channel DVD
- Mini/Micro Component Systems
- Home Theater
- Stereo applications

BENEFITS

- High fidelity, high efficiency Class-T
- Analog inputs

FEATURES

- Class-T Architecture
- Audiophile Quality Sound
 - 0.007% THD+N @ 30W 8Ω (with TP2050)
- High Efficiency
 - 92% @ 60W 8Ω (with TP2050)
- Dynamic Range >100 dB



ABSOLUTE MAXIMUM RATINGS (Note 1)

| SYMBOL | PARAMETER | Value | UNITS |
|--------------------|--|----------------------|-------|
| V ₅ | 5V Power Supply | 6 | V |
| V _{logic} | Input Logic Level | V ₅ +0.3V | V |
| T _A | Operating Free-air Temperature Range | -40 to 85 | °C |
| T _{STORE} | Storage Temperature Range | -55 to 150 | °C |
| T _{JMAX} | Maximum Junction Temperature | 150 | °C |
| ESD _{HB} | ESD Susceptibility – Human Body Model (Note 2), all pins | 2000 | V |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

See the table below for Operating Conditions.

Note 2: Human body model, 100pF discharged through a 1.5KΩ resistor.

OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|-----------------|-----------------------------|---------------------|------|------|-------|
| V ₅ | Supply Voltage | 4.5 | 5 | 5.5 | V |
| V _{HI} | Logic Input High | V ₅ -1.0 | | | V |
| V _{LO} | Logic Input Low | | | 1 | V |
| T _A | Operating Temperature Range | -40 | 25 | 85 | °C |

THERMAL CHARACTERISTICS**TC2000**

| SYMBOL | PARAMETER | Value | UNITS |
|-----------------|--|-------|-------|
| θ _{JA} | Junction-to-ambient Thermal Resistance (still air) | 80 | °C/W |

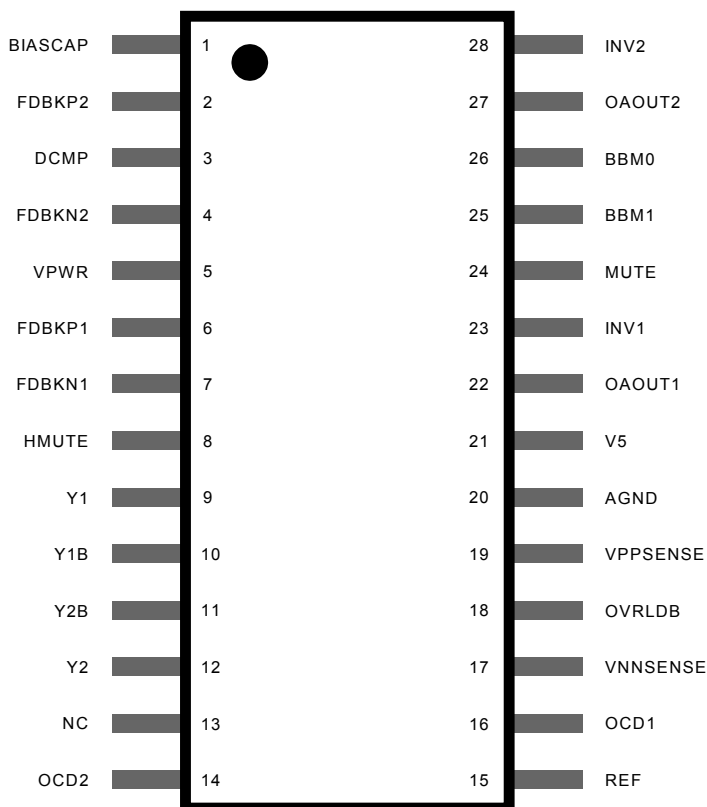
ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|--------------------|--|---------------------|------|------|-------|
| I ₅ | Supply Current | | 60 | | mA |
| f _{sw} | Switching Frequency (adjustable via CFB) | 600 | 650 | | kHz |
| V _{IN} | Input Sensitivity | 0 | | 1.5 | V |
| V _{OUTH} | High Output Voltage | V ₅ -0.5 | | | V |
| V _{OUTLO} | Low Output Voltage | | | 100 | mV |
| R _{IN} | Input Impedance | | 2 | | kΩ |
| | Input DC Bias | | 2.5 | | V |

TC2000 AUDIO SIGNAL PROCESSOR PIN DESCRIPTIONS

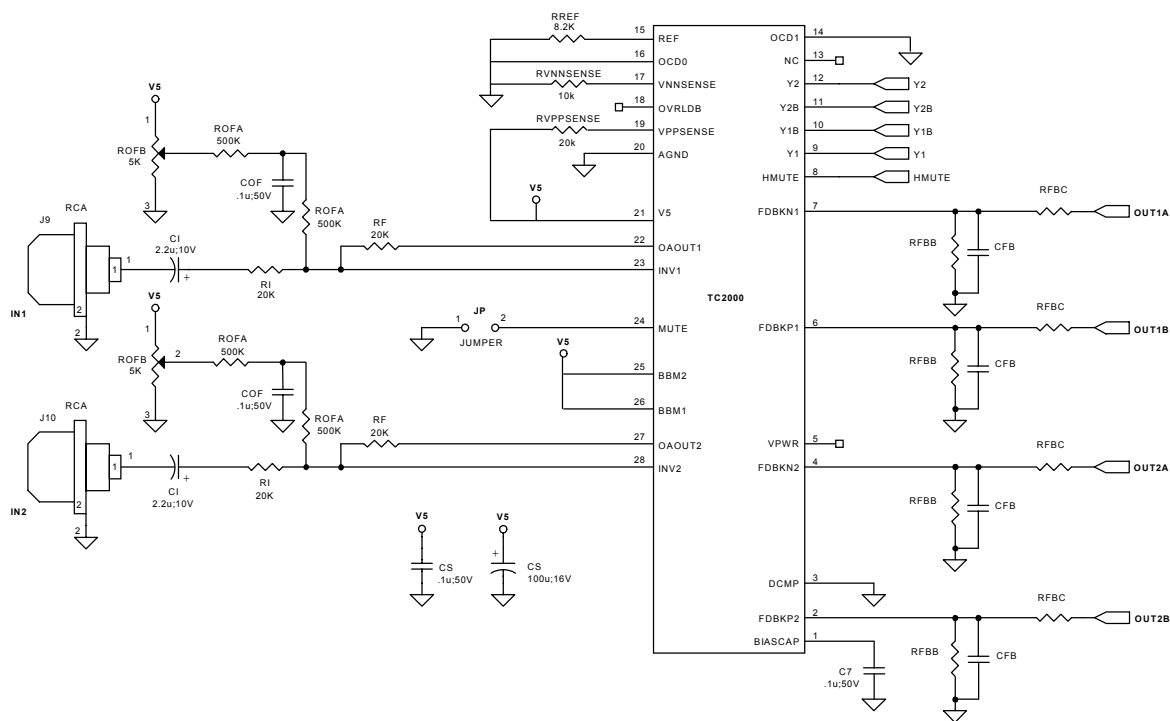
| Pin | Function | Description |
|--------|----------------|--|
| 1 | BIASCAP | Bandgap reference times two (typically 2.5VDC). Used to set the common mode voltage for the input op amps. This pin is not capable of driving external circuitry. |
| 2, 6 | FDBKP2, FDBKP1 | Positive switching feedback. |
| 3 | DCMP | Internal mode selection. This pin must be grounded for proper device operation. |
| 4, 7 | FDBKN2, FDBKN1 | Negative switching feedback. |
| 5 | VPWR | Test pin. Must be left floating. |
| 8 | HMUTE | Logic output. A logic high indicates both amplifiers are muted, due to the mute pin state, or a "fault". |
| 9, 12 | Y1, Y2 | Non-inverted switching modulator outputs. |
| 10, 11 | Y1B, Y2B | Inverted switching modulator outputs. |
| 13 | NC | No connect |
| 14,16 | OCD2, OCD1 | Over Current Detect. Ground if not used. |
| 15 | REF | Internal reference voltage; approximately 1.2 VDC. |
| 17 | VNNSENSE | Negative power stage over/under supply voltage sense resistor tie point. |
| 18 | OVRldb | A logic low output indicates the input signal has overloaded the amplifier. |
| 19 | VPPSENSE | Positive power stage over/under supply voltage sense resistor tie point. |
| 20 | AGND | Ground |
| 21 | V5 | 5 Volt power supply input. |
| 22, 27 | OAOUT1, OAOUT2 | Input stage output pins. |
| 23, 28 | INV1, INV2 | Single-ended inputs. Inputs are a "virtual" ground of an inverting opamp with approximately 2.4VDC bias. |
| 24 | MUTE | When set to logic high, both amplifiers are muted and in idle mode. When low (grounded), both amplifiers are fully operational. If left floating, the device stays in the mute mode. Ground if not used. |
| 25, 26 | BBM1, BBM0 | Break-before-make timing control. |

TC2000 AUDIO SIGNAL PROCESSOR PINOUT



APPLICATION / TEST DIAGRAM

Inputs and TC2000



EXTERNAL COMPONENTS DESCRIPTION (Refer to the Application/Test Circuit)

| Component | Description |
|-----------|---|
| RI | Inverting input resistance to provide AC gain in conjunction with R_F . This input is biased at the BIASCAP voltage (approximately 2.5VDC). |
| RF | Feedback resistor to set AC gain in conjunction with R_I . Please refer to the Amplifier Gain paragraph, in the Application Information section. |
| CI | AC input coupling capacitor, which, in conjunction with R_I , forms a high pass filter at $f_c = 1/(2\pi R_I C_I)$. |
| RFBB | Feedback divider resistor connected to AGND. The value of this resistor depends on the supply voltage setting and helps set gain in conjunction with R_I , R_F , R_{FBB} , and R_{FBC} . Please see the Modulator Feedback Design paragraphs in the Application Information Section. |
| RFBC | Feedback resistor connected from either the OUT1A/OUT2A to FDBKP1/FDBKP2 or OUT1B/OUT2B to FDBKN1/FDBKN2. The value of this resistor depends on the supply voltage setting and helps set gain in conjunction with R_I , R_F , R_{FBB} , and R_{FBC} . It should be noted that the resistor from OUT1/OUT2 to FBKOUT1/FBKOUT2 must have a power rating of greater than $P_{DISS} = VPP^2/(2R_{FBC})$. Please see the Modulator Feedback Design paragraphs in the Application Information Section. |
| CFB | Feedback delay capacitor that both lowers the idle switching frequency and filters very high frequency noise from the feedback signal, which improves amplifier performance. The value of C_{FB} should be offset between channel 1 and channel 2 so that the idle switching difference is greater than 40kHz. Please refer to the Application / Test Circuit. |
| ROFB | Potentiometer used to manually trim the DC offset on the speaker output. |
| ROFA | Resistor that limits the manual DC offset trim range and allows for more precise adjustment. |
| RREF | Bias resistor. Locate close to pin 15 and ground at pin 20. |
| CS | Supply decoupling for the power supply pins. For optimum performance, these components should be located close to the TC2000 and returned to their respective ground as shown in the Application/Test Circuit. |
| RVNSENSE | Resistor used to terminate the VNSENSE pin to AGND. |
| RVPPSENSE | Resistor used to terminate the VPPSENSE pin to 5V. |

APPLICATION INFORMATION**TK2050 Basic Amplifier Operation**

The TC2000 is a 5V CMOS signal processor that amplifies the audio input signal and converts the audio signal to a switching pattern. This switching pattern is spread spectrum with a typical idle switching frequency of about 650kHz externally set by the CFB. The switching patterns for the two channels are not synchronized and the idle switching frequencies should differ by at least 40kHz to avoid increasing the audio band noise floor. The idle frequency difference can be accomplished by offsetting the value of CFB for each channel. Typical values of CFB with the TP2050 are 470pF for channel 1 and 390pF for channel 2.

Complementary copies of the switching pattern are output through the Y1 and Y1B pins and the Y2 and Y2B pins. These signals are used to drive the inputs of a MOSFET driver. In the generation of the patterns for the MOSFET driver the TC2000 inserts a “break-before-make” dead time between the

turn-off of one transistor and the turn-on of the other in order to minimize shoot-through currents. For applications using the TP2050 please tie BBM0 and BBM1 to 5V for optimal operation.

Input Stage Design

The TC2000 input stage is configured as an inverting amplifier, allowing the system designer flexibility in setting the input stage gain and frequency response. Figure 1 shows a typical application where the input stage is a constant gain inverting amplifier. The input stage gain should be set so that the maximum input signal level will drive the input stage output to 4Vpp.

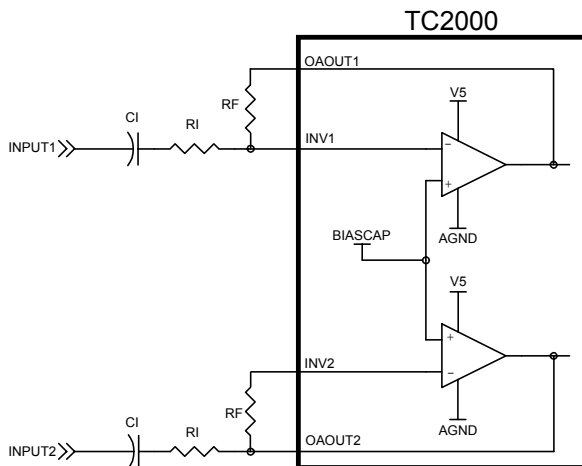


Figure 1: Input Stage

The gain of the input stage, above the low frequency high pass filter point, is that of a simple inverting amplifier: It should be noted that the input amplifiers are biased at approximately 2.5VDC. Thus, the polarity of C₁ must be followed as shown in Figure 1 for a standard ground referenced input signal

$$A_{V \text{ INPUT STAGE}} = - \frac{R_F}{R_I}$$

Input Capacitor Selection

C₁ can be calculated once a value for R₁ has been determined. C₁ and R₁ determine the input low frequency pole. Typically this pole is set below 10Hz. C₁ is calculated according to:

$$C_1 = \frac{1}{2\pi f_P R_1}$$

where:

R₁ = Input resistor value in ohms.

f_P = Input low frequency pole (typically 10Hz or below)

Modulator Feedback Design

The modulator converts the signal from the input stage to the high-voltage output signal. The optimum gain of the modulator is determined from the maximum allowable feedback level for the modulator and maximum supply voltage for the power stage. Depending on the maximum supply voltage, the feedback ratio will need to be adjusted to maximize performance. The values of RFBB and RFBC (see explanation below) define the gain of the modulator. Once these values are chosen, based on the maximum supply voltage, the gain of the modulator will be fixed even as the supply voltage fluctuates due to current draw.

For the best signal-to-noise ratio and lowest distortion, the maximum differential modulator feedback voltage should be approximately 4Vpp. This will keep the gain of the modulator as low as possible and still allow headroom so that the feedback signal does not clip the modulator feedback stage.

The modulator feedback resistors are:

R_{FBB} = User specified; typically 1k Ω

$$R_{FBC} = \left(\frac{V_{CC} * R_{FBB}}{2V} \right) - R_{FBB}$$

Mute Control

When a logic high signal is supplied to MUTE, both amplifier channels are muted (both high- and low-side transistors are turned off). When a logic level low is supplied to MUTE, both amplifiers are fully operational.

Output Voltage Offset

The TC2000 does not have internal compensation for DC offset. If offset is a consideration for the intended application, trimming of the input offset voltage will be required. Tripath has had success with both active and passive circuits for this purpose; please consult with the Tripath Applications team for further information.

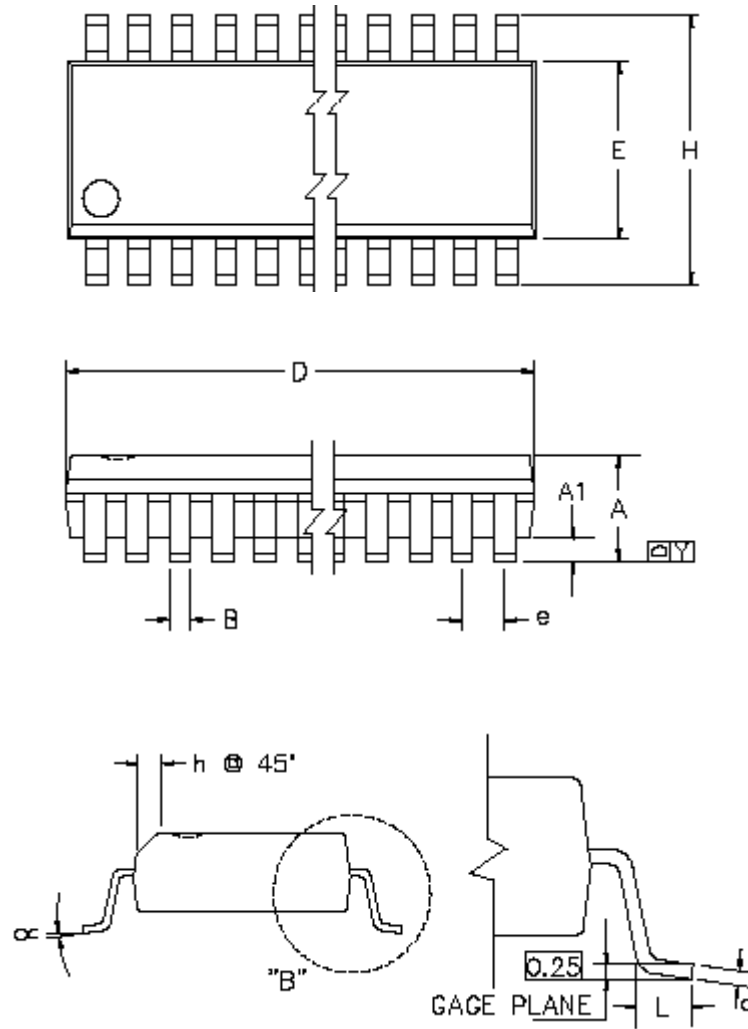
HMUTE

The HMUTE pin is a 5V logic output that indicates various fault conditions within the device.

OVRLDB

The OVRLDB pin is a 5V logic output that is asserted just at the onset of clipping. When low, it indicates that the level of the input signal has overloaded the amplifier resulting in increased distortion at the output. The OVRLDB signal can be used to control a distortion indicator light or LED through a simple buffer circuit, as the OVRLDB cannot drive an LED directly. There is a 20K resistor on chip in series with the OVRLDB output.

PACKAGE INFORMATION - TC2000



| SYMBOL | CONTROL DIMENSIONS ARE IN MM | | | | | |
|--------|------------------------------|-------|-------|-------|-------|-------|
| | MILLIMETER | | | INCH | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 2.35 | 2.54 | 2.65 | 0.092 | 0.100 | 0.104 |
| A1 | 0.10 | 0.17 | 0.30 | 0.004 | 0.006 | 0.012 |
| B | 0.33 | 0.42 | 0.51 | 0.013 | 0.016 | 0.020 |
| C | 0.23 | 0.25 | 0.32 | 0.009 | 0.010 | 0.012 |
| E | 7.40 | 7.50 | 7.60 | 0.291 | 0.295 | 0.299 |
| e | | 1.27 | | | 0.050 | |
| H | 10.00 | 10.30 | 10.65 | 0.394 | 0.406 | 0.419 |
| h | 0.25 | 0.50 | 0.75 | 0.009 | 0.020 | 0.029 |
| L | 0.40 | 0.70 | 1.27 | 0.015 | 0.028 | 0.050 |
| α | 0° | | 8° | 0° | | 8° |
| Y | 0 | | 0.10 | 0 | | 0.004 |
| D | 17.70 | 17.90 | 18.10 | 0.697 | 0.705 | 0.712 |

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