

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC4027BP, TC4027BF, TC4027BFN

TC4027B DUAL J-K MASTER-SLAVE FLIP FLOP

TC4027B is J-K master-slave flip-flop having RESET and SET functions.

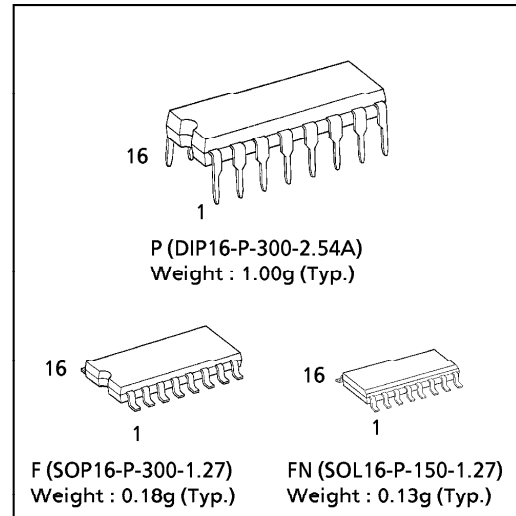
In the case of J-K made, when the clock input is given with both RESET and SET at "L", the output changes at rising edge of the clock according to the states of J and K.

When SET input is placed at "H", and RESET input is placed at "L", outputs become $Q = "H"$, and $\bar{Q} = "L"$.

When RESET input is placed at "H", and SET input is placed at "L", outputs become $Q = "L"$, and $\bar{Q} = "H"$.

When both of RESET input and SET input are at "H", outputs become $Q = "H"$ and $\bar{Q} = "H"$.

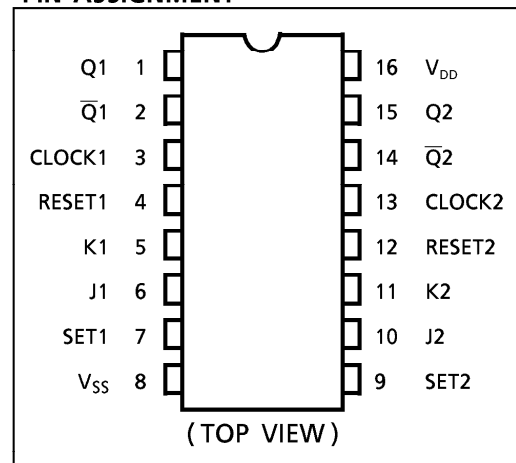
(Note) The JEDEC SOP (FN) is not available in Japan.



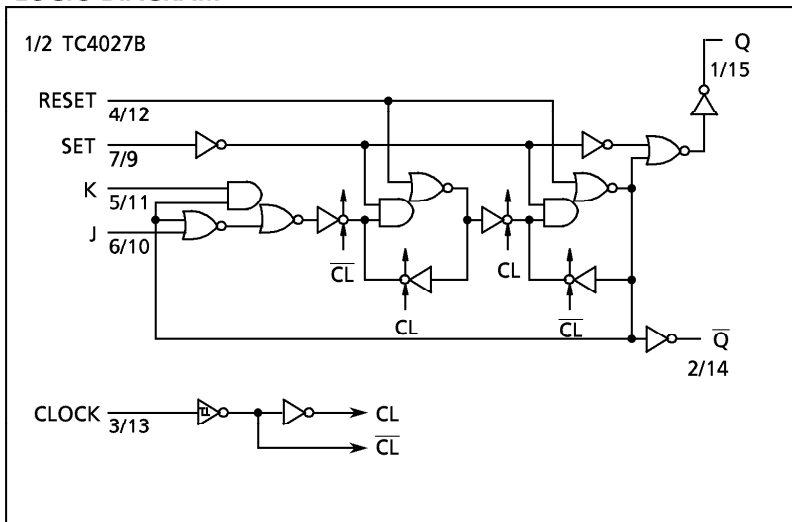
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T_{opr}	$-40 \sim 85$	$^{\circ}C$
Storage Temperature Range	T_{stg}	$-65 \sim 150$	$^{\circ}C$

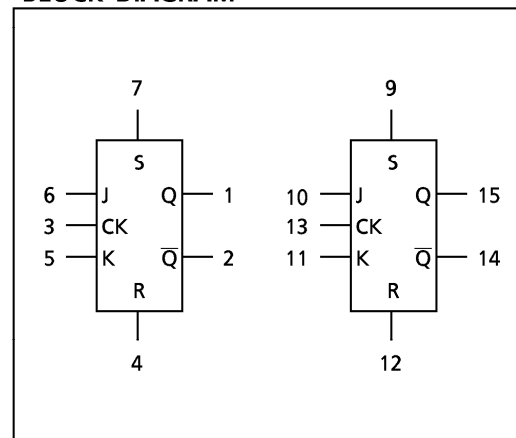
PIN ASSIGNMENT



LOGIC DIAGRAM








BLOCK DIAGRAM



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TRUTH TABLE

INPUTS					OUTPUTS	
RESET	SET	J	K	CLOCK Δ	Q_{n+1}	\bar{Q}_{n+1}
L	H	*	*	*	H	L
H	L	*	*	*	L	H
H	H	*	*	*	H	H
L	L	L	L		Q_n^*	Q_n^*
L	L	L	H		L	H
L	L	H	L		H	L
L	L	H	H		\bar{Q}_n^{**}	Q_n^{**}
L	L	*	*		Q_n^*	\bar{Q}_n^*

* : Don't Care
 Δ : Level Change
 * : No Change
 ** : Change

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RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$)

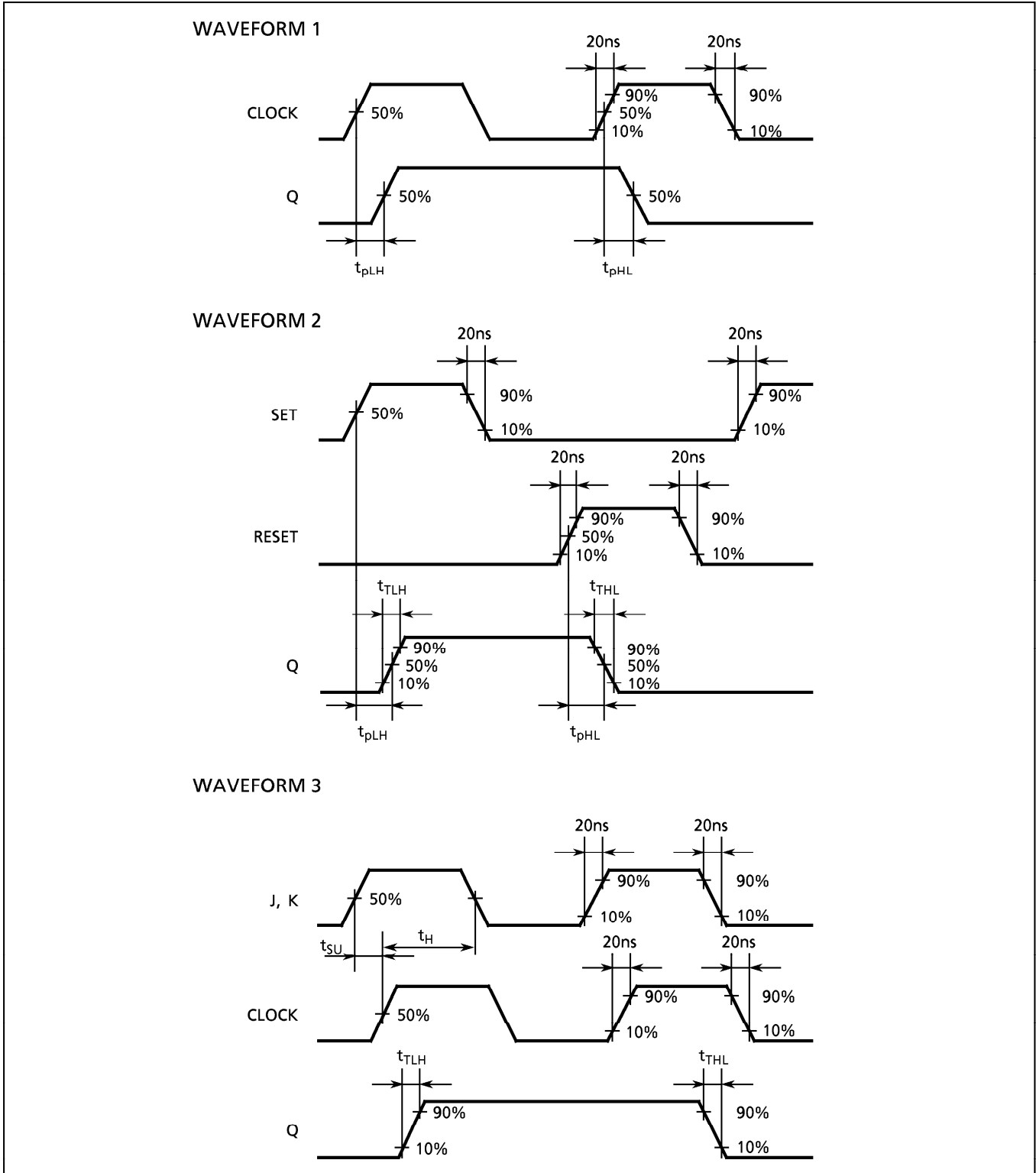
CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Output Voltage	V_{OH}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V	
			10	9.95	—	9.95	10.00	—	9.95	—		
			15	14.95	—	14.95	15.00	—	14.95	—		
Low-Level Output Voltage	V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V	
			10	—	0.05	—	0.00	0.05	—	0.05		
			15	—	0.05	—	0.00	0.05	—	0.05		
Output High Current	I_{OH}	$V_{OH} = 4.6V$ $V_{OH} = 2.5V$ $V_{OH} = 9.5V$ $V_{OH} = 13.5V$ $V_{IN} = V_{SS}, V_{DD}$	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA	
			5	-2.50	—	-2.10	-4.0	—	-1.70	—		
			10	-1.50	—	-1.30	-2.2	—	-1.10	—		
			15	-4.00	—	-3.40	-9.0	—	-2.80	—		
Output Low Current	I_{OL}	$V_{OL} = 0.4V$ $V_{OL} = 0.5V$ $V_{OL} = 1.5V$ $V_{IN} = V_{SS}, V_{DD}$	5	0.61	—	0.51	1.2	—	0.42	—	mA	
			10	1.50	—	1.30	3.2	—	1.10	—		
			15	4.00	—	3.40	12.0	—	2.80	—		
Input High Voltage	V_{IH}	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $ I_{OUT} < 1\mu A$	5	3.5	—	3.5	2.75	—	3.5	—	V	
			10	7.0	—	7.0	5.50	—	7.0	—		
			15	11.0	—	11.0	8.25	—	11.0	—		
Input Low Voltage	V_{IL}	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $ I_{OUT} < 1\mu A$	5	—	1.5	—	2.25	1.5	—	1.5	V	
			10	—	3.0	—	4.50	3.0	—	3.0		
			15	—	4.0	—	6.75	4.0	—	4.0		
Input Current	"H" Level	I_{IH}	$V_{IH} = 18V$	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
	"L" Level	I_{IL}	$V_{IL} = 0V$	18	—	-0.1	—	-10^{-5}	-0.1	—	-1.0	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}^*$	5	—	1	—	0.002	1	—	30	μA	
			10	—	2	—	0.004	2	—	60		
			15	—	4	—	0.008	4	—	120		

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, CL = 50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t _{TLH}		5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output Transition Time (High to Low)	t _{THL}		5	—	70	200	
			10	—	35	100	
			15	—	30	80	
Propagation Delay Time (CLOCK - Q, \bar{Q})	t _{pLH} t _{pHL}		5	—	150	300	
			10	—	75	130	
			15	—	60	90	
Propagation Delay Time (SET, RESET - Q, \bar{Q})	t _{pLH} t _{pHL}		5	—	120	300	
			10	—	60	130	
			15	—	45	90	
Max. Clock Frequency	f _{CL}		5	3.5	8	—	MHz
			10	8.0	16	—	
			15	12.0	20	—	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t _{rCL} t _{fCL}		5	No Limit			μs
			10				
			15				
Min. Pulse Width (SET, RESET)	t _w		5	—	60	180	ns
			10	—	35	80	
			15	—	25	50	
Min. Clock Pulse Width	t _w		5	—	60	140	
			10	—	35	60	
			15	—	25	40	
Min. Set-up Time (J, K - CLOCK)	t _{SU}		5	—	30	140	
			10	—	10	50	
			15	—	5	35	
Min. Hold Time (J, K - CLOCK)	t _H		5	—	—	140	
			10	—	—	50	
			15	—	—	35	
Min. Removal Time (SET, RESET - CLOCK)	t _{rem}		5	—	—	40	
			10	—	—	20	
			15	—	—	15	
Input Capacitance	C _{IN}			—	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



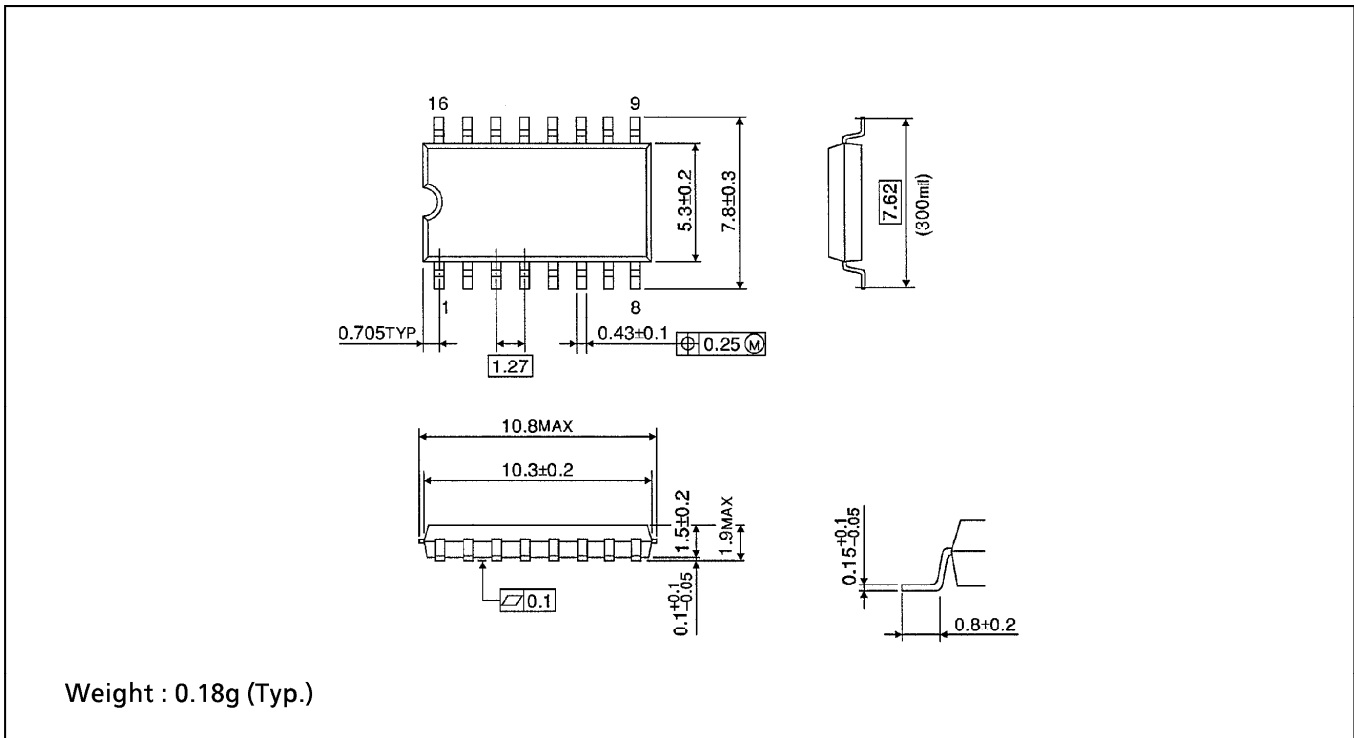
DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

Unit in mm



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

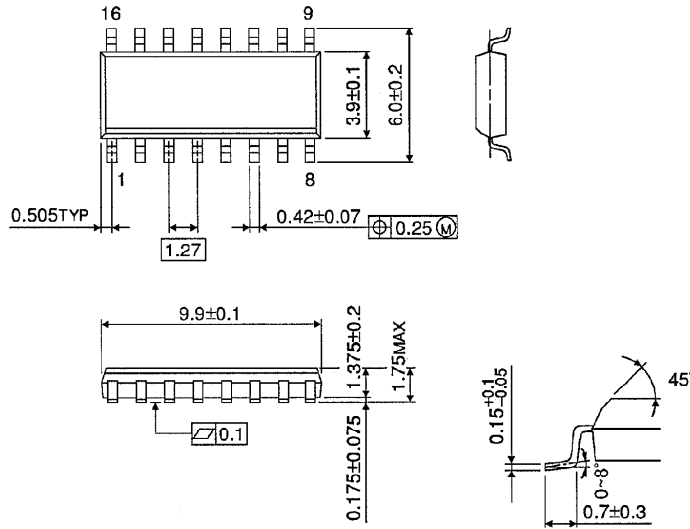
Unit in mm



SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)