TC7135

4-1/2 Digit A/D Converter

Features

- Low Rollover Error: ±1 Count Max
- Nonlinearity Error: ±1 Count Max
- Reading for 0V Input
- True Polarity Indication at Zero for Null Detection
- Multiplexed BCD Data Output
- TTL-Compatible Outputs
- Differential Input
- Control Signals Permit Interface to UARTs and Microprocessors
- Blinking Display Visually Indicates Overrange Condition
- Low Input Current: 1 pA
- Low Zero Reading Drift: 2 µV/°C
- Auto-Ranging Supported with Overrange and Underrange Signals
- Available in PDIP and Surface-Mount Packages

Applications

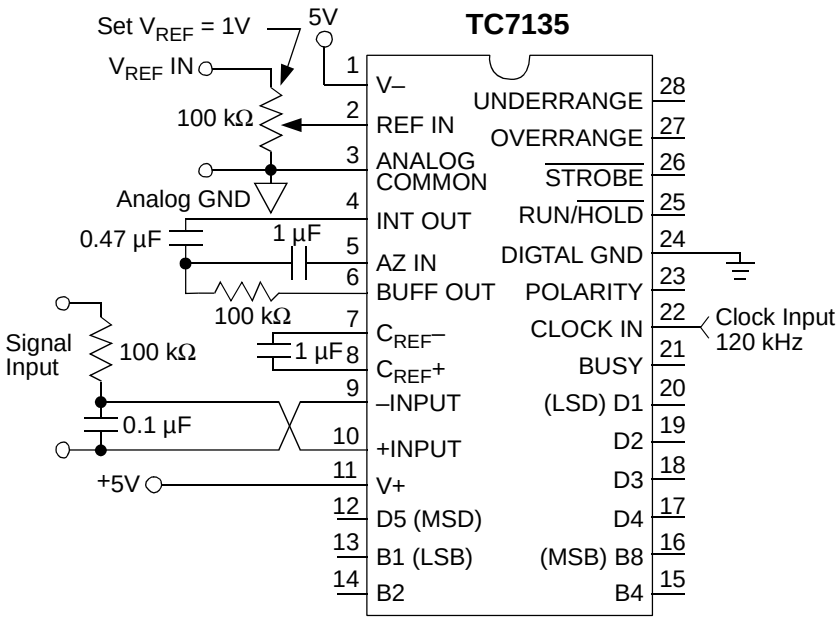
- Precision Analog Signal Processor
- Precision Sensor Interface
- High Accuracy DC Measurements

General Description

The TC7135 4-1/2 digit A/D Converter (ADC) offers 50 ppm (1 part in 20,000) resolution with a maximum nonlinearity error of 1 count. An auto-zero cycle reduces zero error to below 10 µV and zero drift to 0.5 µV/°C. Source impedance errors are minimized by a 10 pA maximum input current. Rollover error is limited to ±1 count.

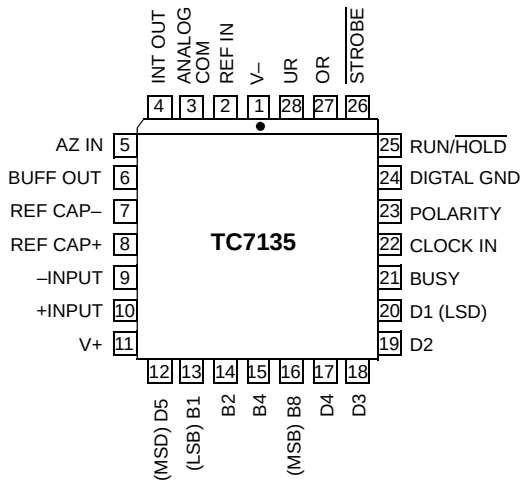
Microprocessor-based measurement systems are supported by the BUSY, $\overline{\text{STROBE}}$ and RUN/$\overline{\text{HOLD}}$ control signals. Remote data acquisition systems with data transfer via UARTs are also possible. The additional control pins and multiplexed BCD outputs make the TC7135 the ideal converter for display or microprocessor-based measurement systems.

Functional Block Diagram

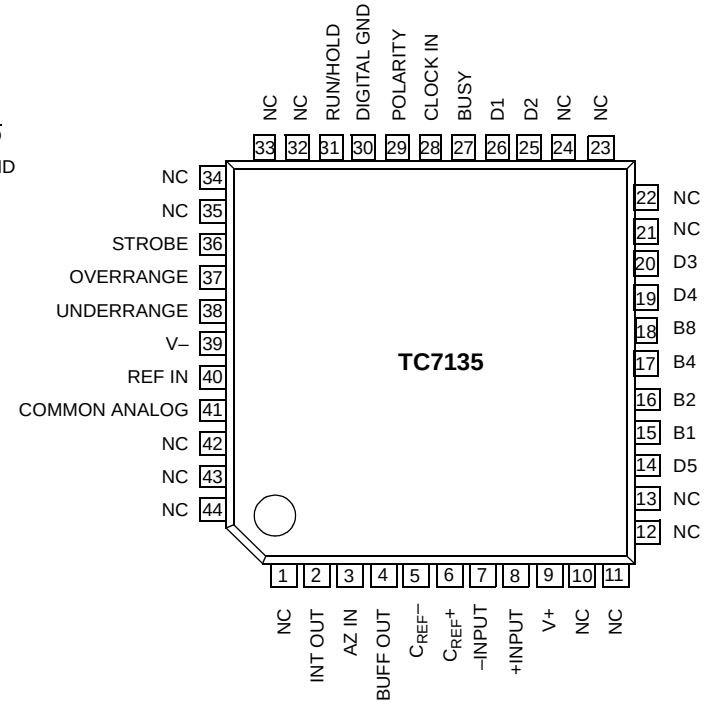


Package Types

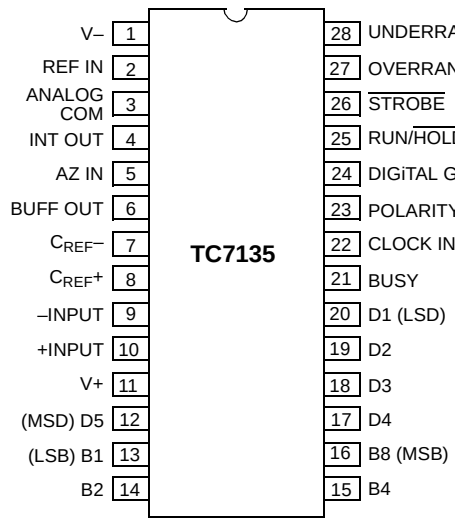
28-Pin PLCC



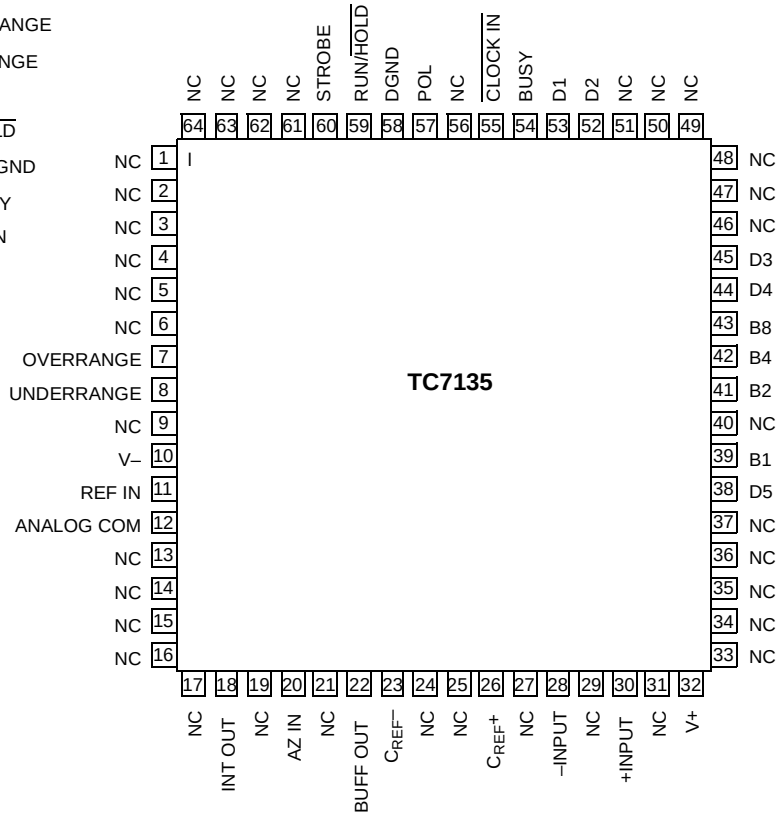
44-Pin MQFP



28-Pin PDIP



64-Pin MQFP



NOTE: NC = No internal connection.

1.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Positive Supply Voltage.....+6V
Negative Supply Voltage.....- 9V
Analog Input Voltage (Pin 9 or 10) .....V+ to V- **(Note 2)**
Reference Input Voltage (Pin 2)..... V+ to V-
Clock Input Voltage ..... 0V to V+
Operating Temperature Range .....0°C to +70°C
Storage Temperature Range.....–65°C to +150°C
Package Power Dissipation; ($T_A \leq 70°C$)
28-Pin PDIP 1.14Ω
28-Pin PLCC 1.00Ω
44-Pin MQFP.....
64-Pin MQFP 1.14Ω

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, F_{CLOCK} = 120 kHz, V+ = +5V, V- = -5V. (see **Functional Block Diagram**).

Parameters	Sym	Min.	Typ.	Max.	Units	Conditions
Analog						
Display Reading with Zero Volt Input		-0.0000	±0.0000	+0.0000	Display Reading	**Note 2**, **Note 3**
Zero Reading Temperature Coefficient	TC_Z	—	0.5	2	µV/°C	V_{IN} = 0V, **(Note 4)**
Full Scale Temperature Coefficient	TC_{FS}	—	—	5	ppm/°C	V_{IN} = 2V, **(Note 4, Note 5)**
Nonlinearity Error	NL	—	0.5	1	Count	**Note 6**
Differential Linearity Error	DNL	—	0.01	—	LSB	**Note 6**
Display Reading in Ratiometric Operation		+0.9996	+0.9999	+1.0000	Display Reading	$V_{IN} = V_{REF,}$ **(Note 2)**
± Full Scale Symmetry Error (Rollover Error)	±FSE	—	0.5	1	Count	$-V_{IN} = +V_{IN,}$ **(Note 7)**
Input Leakage Current	I_{IN}	—	1	10	pA	**Note 3**
Noise	e_N	—	15	—	μV_{P-P}	Peak-to-Peak Value not Exceeded 95% of Time
Digital						
Input Low Current	I_{IL}	—	10	100	µA	V_{IN} = 0V
Input High Current	I_{IH}	—	0.08	10	µA	V_{IN} = +5V
Output Low Voltage	V_{OL}	—	0.2	0.4	V	I_{OL} = 1.6 mA
Output High Voltage;	V_{OH}	2.4	4.4	5	V	I_{OH} = 1 mA
B_1, B_2, B_4, B_8, D_1 –D_5 Busy, Polarity, Overrange, Underrange, Strobe		4.9	4.99	5	V	I_{OH} = 10 µA
Clock Frequency	F_{CLK}	0	200	1200	kHz	**Note 8**

Note 1: Limit input current to under 100 µA if input voltages exceed supply voltage.
2: Full-scale voltage = 2V
3: V_{IN} = 0V
4: 30°C ≤ T_A ≤ +70°C
5: External reference temperature coefficient less than 0.01 ppm/°C.
6: -2V ≤ V_{IN} ≤ +2V. Error of reading from best fit straight line.
7: $|V_{IN}|$ = 1.9959
8: Specification related to clock frequency range over which the TC7135 correctly performs its various functions. Increased errors result at higher operating frequencies.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, F_{CLOCK} = 120 kHz, V+ = +5V, V- = -5V. (see **Functional Block Diagram**).

Parameters	Sym	Min.	Typ.	Max.	Units	Conditions
Power Supply						
Positive Supply Voltage	V+	4	5	6	V	
Negative Supply Voltage	V-	-3	-5	-8	V	
Positive Supply Current	I+	—	1	3	mA	F_{CLK} = 0 Hz
Negative Supply Current	I-	—	0.7	3	mA	F_{CLK} = 0 Hz
Power Dissipation	PD	—	8.5	30	mW	F_{CLK} = 0 Hz

Note 1: Limit input current to under 100 µA if input voltages exceed supply voltage.

2: Full-scale voltage = 2V

3: V_{IN} = 0V

4: 30°C ≤ T_A ≤ +70°C

5: External reference temperature coefficient less than 0.01 ppm/°C.

6: -2V ≤ V_{IN} ≤ +2V. Error of reading from best fit straight line.

7: $|V_{IN}|$ = 1.9959

8: Specification related to clock frequency range over which the TC7135 correctly performs its various functions. Increased errors result at higher operating frequencies.

2.0 PIN DESCRIPTIONS

The description of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number 28-Pin PDIP, 28-Pin PLCC	Pin Number 44-Pin MQFP*	Pin Number 64-Pin MQFP*	Symbol	Description
1	39	10	V–	Negative power supply input.
2	40	11	REF IN	External reference input.
3	41	12	ANALOG COMMON	Reference point for REF IN.
4	2	18	INT OUT	Integrator output. Integrator capacitor connection.
5	3	20	AZ IN	Auto-zero inpt. Auto-zero capacitor connection.
6	4	22	BUFF OUT	Analog input buffer output. Integrator resistor connection.
7	5	23	$C_{REF}-$	Reference capacitor input. Reference capacitor negative connection.
8	6	26	$C_{REF}+$	Reference capacitor input. Reference capacitor positive connection.
9	7	28	–INPUT	Analog input. Analog input negative connection.
10	8	30	+INPUT	Analog input. Analog input positive connection.
11	9	32	V+	Positive power supply input.
12	14	38	D5	Digit drive output. Most Significant Digit (MSD)
13	15	39	B1	Binary Coded Decimal (BCD) output. Least Significant bit (LSb).
14	16	41	B2	BCD output.
15	17	42	B4	BCD output.
16	18	43	B8	BCD output. Most Significant bit (MSb).
17	19	44	D4	Digit drive output.
18	20	45	D3	Digit drive output.
19	25	52	D2	Digit drive output.
20	26	53	D1	Digit drive output. Least Significant Digit (LSD).
21	27	54	BUSY	Busy output. At the beginning of the signal-integration phase, BUSY goes high and remains high until the first clock pulse after the integrator zero crossing.
22	28	55	CLOCK IN	Clock input. Conversion clock connection.
23	29	57	POLARITY	Polarity output. A positive input is indicated by a logic high output. The polarity output is valid at the beginning of the reference integrate phase and remains valid until determined during the next conversion.
24	30	58	DGND	Digital logic reference input.
25	31	59	RUN/$\overline{\text{HOLD}}$	Run/Hold input. When at a logic high, conversions are performed continuously. A logic low holds the current data as long as the low condition exists.
26	36	60	$\overline{\text{STROBE}}$	Strobe output. The STROBE output pulses low in the center of the digit drive outputs.
27	37	7	OVERRANGE	Overrange output. A logic high indicates that the analog input exceeds the full-scale input range.
28	38	8	UNDERRANGE	Underrange output. A logic high indicates that the analog input is less than 9% of the full-scale input range.

***** Pins not identified or documented are NC (no connects).

3.0 DETAILED DESCRIPTION

All pin designations refer to the 28-pin PDIP package.

3.1 Dual-Slope Conversion Principles

The TC7135 is a dual-slope, integrating A/D converter. An understanding of the dual-slope conversion technique will aid in following the detailed TC7135 operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

1. Input signal integration.
2. Reference voltage integration (de-integration).

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter, a complete conversion requires the integrator output to “ramp-up” and “ramp-down”.

A simple mathematical equation relates the input signal, reference voltage and integration time:

EQUATION 3-1:

$$\frac{1}{R_{INT}C_{INT}}\int_0^{T_{INT}} V_{IN}(T)DT = \frac{V_{REF}T_{DEINT}}{R_{INT}C_{INT}}$$

Where:

V_{REF} = Reference voltage
T_{INT} = Signal integration time (fixed)
T_{DEINT} = Reference voltage integration time (variable)

For a constant V_{IN}:

EQUATION 3-2:

$$V_{IN} = \frac{V_{REF}T_{DEINT}}{T_{INT}}$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated, or averaged, to zero during the integration periods.

Integrated ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments (see Figure 3-1).

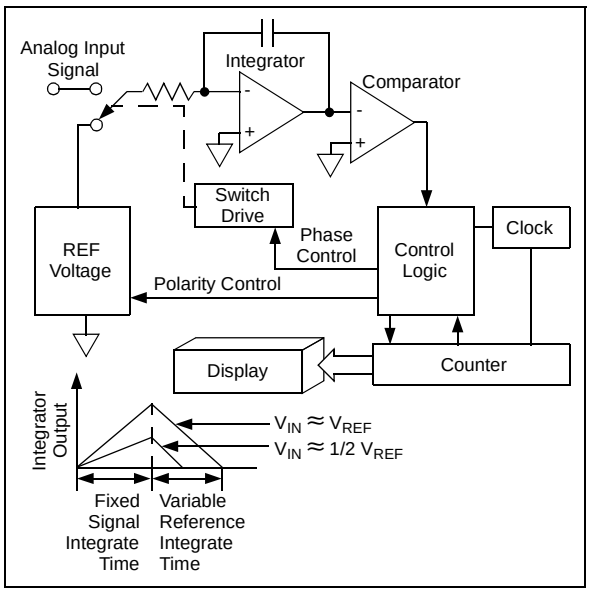


FIGURE 3-1: *Basic Dual-Slope Converter.*

3.2 TC7135 Operational Theory

The TC7135 incorporates a system zero phase and integrator output voltage zero phase to the normal two-phase dual-slope measurement cycle. Reduced system errors, fewer calibration steps and a shorter overrange recovery time result.

The TC7135 measurement cycle contains four phases:

1. System zero.
2. Analog input signal integration.
3. Reference voltage integration.
4. Integrator output zero.

Internal analog gate status for each phase is shown in Figure 3-1.

TABLE 3-1: INTERNAL ANALOG GATE STATUS

Conversion Cycle Phase	SW_I	SW_{RI}+	SW_{RI}-	SW_Z	SW_R	SW_1	SW_{IZ}	Reference Figures
System Zero	—	—	—	Closed	Closed	Closed	—	**Figure 3-2**
Input Signal Integration	Closed	—	—	—	—	—	—	**Figure 3-3**
Reference Voltage Integration	—	Closed*	—	—	—	Closed	—	**Figure 3-4**
Integrator Output Zero	—	—	—	—	—	Closed	Closed	**Figure 3-5**

* Assumes a positive polarity input signal. SW_{RI} would be closed for a negative input signal.

3.2.1 SYSTEM ZERO

During this phase, errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With a zero input voltage, the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to the ANALOG COMMON pin. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages (see Figure 3-2).

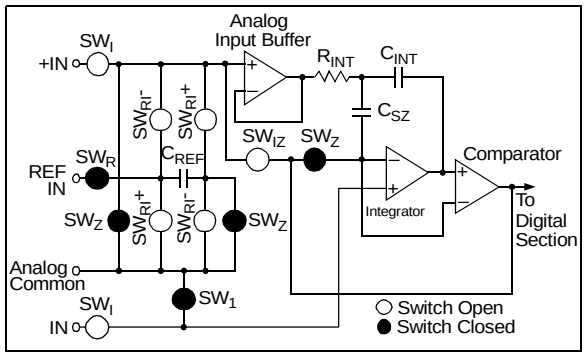


FIGURE 3-2: *System Zero Phase.*

3.2.2 ANALOG INPUT SIGNAL INTEGRATION

The TC7135 integrates the differential voltage between the +INPUT and -INPUT pins. The differential voltage must be within the device Common mode range; -1V from either supply rail, typically. The input signal polarity is determined at the end of this phase.

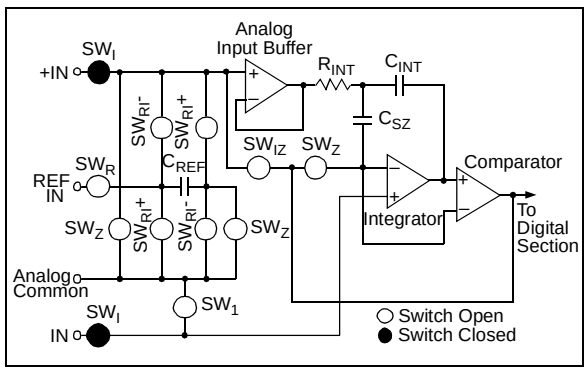


FIGURE 3-3: *Input Signal Integration Phase.*

3.2.3 REFERENCE VOLTAGE INTEGRATION

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero **(**see Figure 3-4). The digital reading displayed is:

EQUATION 3-3:

$$Reading = 10,000\frac{[Differential\ Input]}{V_{REF}}$$

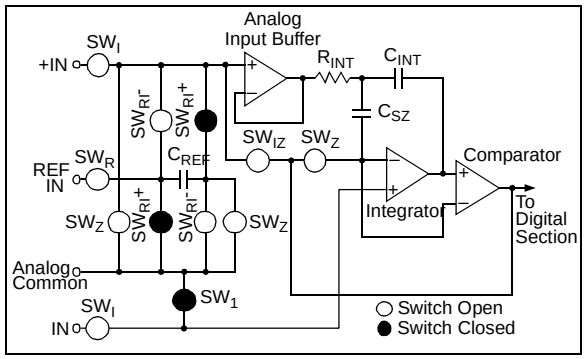


FIGURE 3-4: *Reference Voltage Integration Cycle.*

3.2.4 INTEGRATOR OUTPUT ZERO

This phase ensures the integrator output is at 0V when the system zero phase is entered. It also ensures that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists, the phase is extended to 6200 clock cycles (see Figure 3-5).

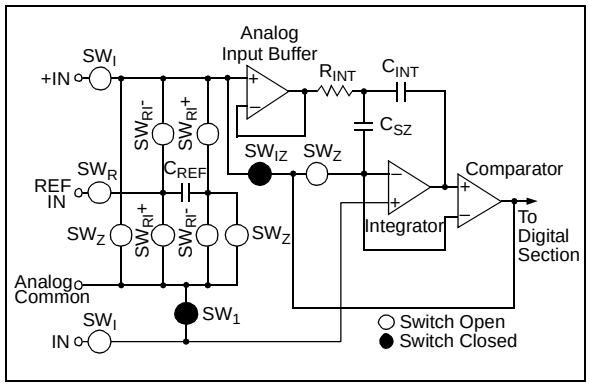


FIGURE 3-5: *Integrator Output Zero Phase.*

4.0 ANALOG SECTION FUNCTIONAL DESCRIPTION

4.1 Differential Inputs

The TC7135 operates with differential voltages (+INPUT, pin 10 and -INPUT, pin 9) within the input amplifier Common mode range, which extends from 1V below the positive supply to 1V above the negative supply. Within this Common mode voltage range, an 86 dB Common mode rejection ratio is typical.

The integrator output also follows the Common mode voltage and must not be allowed to saturate. A worst-case condition exists, for example, when a large positive Common mode voltage with a near full scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive Common mode voltage. For these critical applications, the integrator swing can be reduced to less than the recommended 4V full scale swing, resulting in some loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

4.2 Analog Common Input

The ANALOG COMMON pin is used as the -INPUT return during auto-zero and de-integrate. If -INPUT is different from ANALOG COMMON, a Common mode voltage exists in the system. However, this signal is rejected by the excellent CMRR of the converter. In most applications, –INPUT will be set at a fixed, known voltage (power supply common, for instance). In this application, ANALOG COMMON should be tied to the same point, thus removing the Common mode voltage from the converter. The reference voltage is referenced to ANALOG COMMON.

4.3 Reference Voltage Input

The reference voltage input (REF IN) must be a positive voltage with respect to ANALOG COMMON. A reference voltage circuit is shown in Figure 4-1.

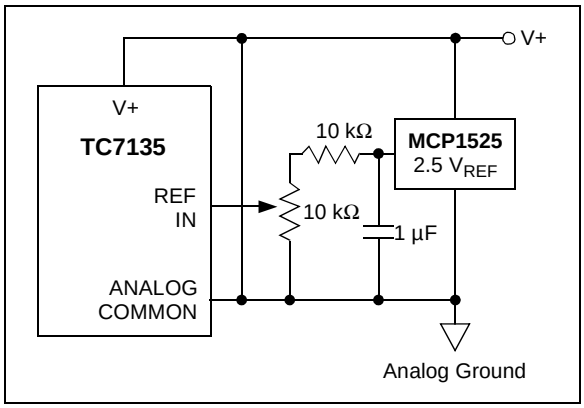


FIGURE 4-1: *Using An External Reference.*

5.0 DIGITAL SECTION FUNCTIONAL DESCRIPTION

The major digital subsystems within the TC7135 are illustrated in Figure 5-1, with timing relationships shown in Figure 5-2. The multiplexed BCD output data can be displayed on LCD or LED displays. The digital section is best described through a discussion of the control signals and data outputs.

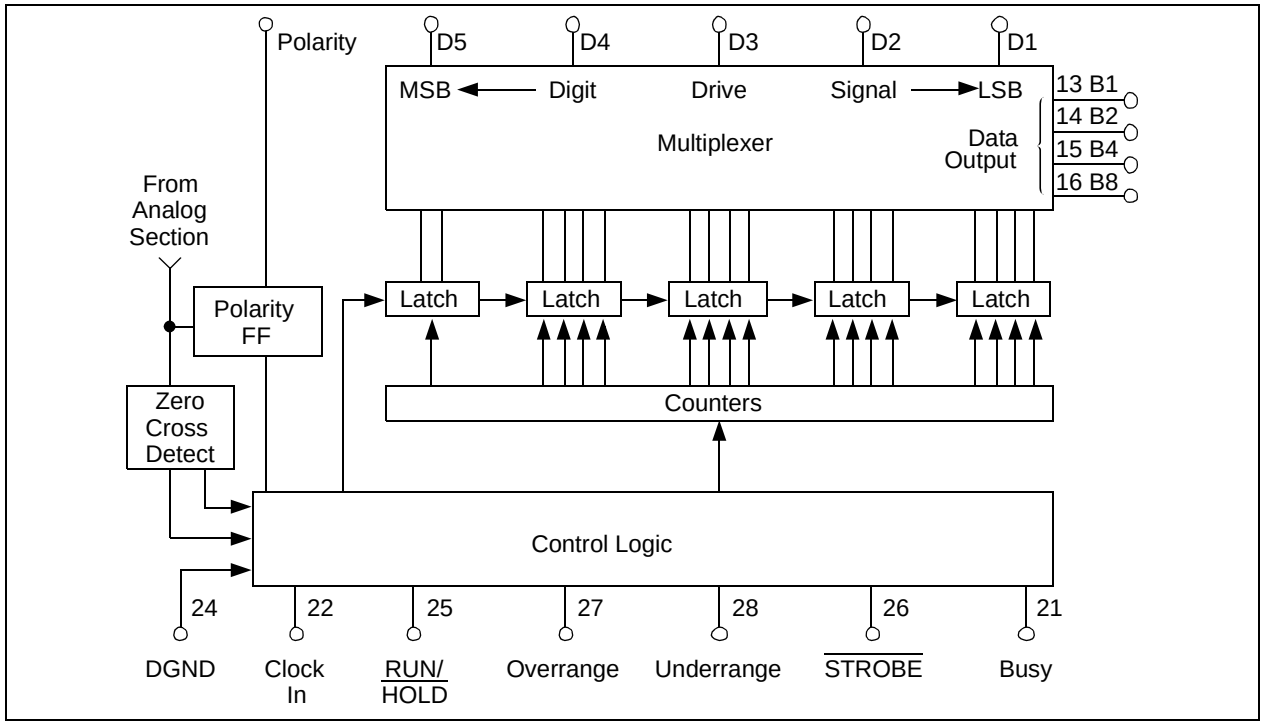


FIGURE 5-1: *Digital Section Functional Diagram.*

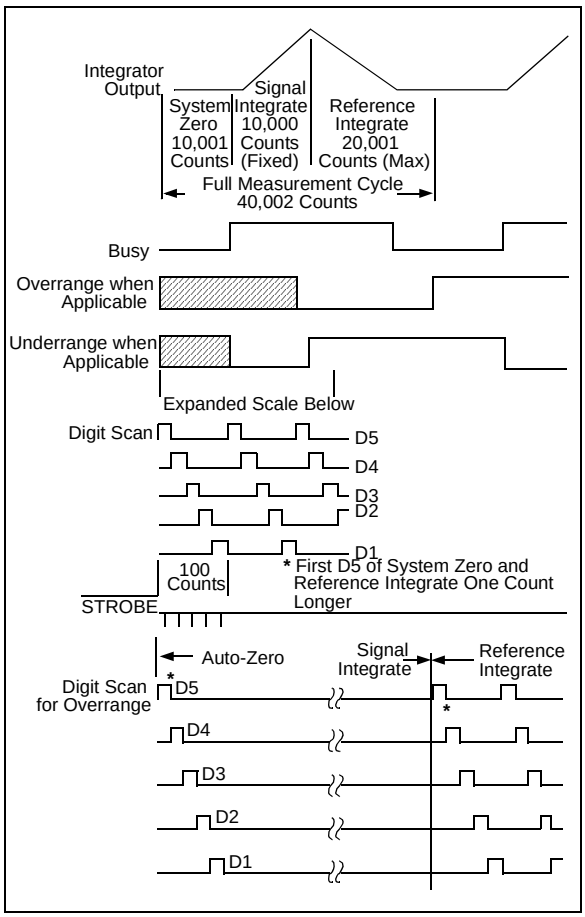


FIGURE 5-2: *Timing Diagrams For Outputs.*

5.1 RUN/$\overline{\text{HOLD}}$ Input

When left open, this pin assumes a logic '1' level. With a RUN/$\overline{\text{HOLD}}$ = 1, the TC7135 performs conversions continuously, with a new measurement cycle beginning every 40,002 clock pulses.

When RUN/$\overline{\text{HOLD}}$ changes to a logic '0', the measurement cycle in progress will be completed, with the data held and displayed as long as the logic '0' condition exists.

A positive pulse (>300 nsec) at RUN/$\overline{\text{HOLD}}$ initiates a new measurement cycle. The measurement cycle in progress when RUN/$\overline{\text{HOLD}}$ initially assumed the logic '0' state must be completed before the positive pulse can be recognized as a single conversion run command.

The new measurement cycle begins with a 10,001 count auto-zero phase. At the end of this phase, the busy signal goes high.

5.2 $\overline{\text{STROBE}}$ Output

During the measurement cycle, the $\overline{\text{STROBE}}$ control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_5) (see Figure 5-3).

D_5 (MSD) goes high for 201 counts when the measurement cycles end. In the center of the D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first $\overline{\text{STROBE}}$ occurs for one half clock pulse. After the D_5 digit strobe, D_4 goes high for 200 clock pulses. The $\overline{\text{STROBE}}$ then goes low 100 clock pulses after D_4 goes high. This continues through the D_1 digit drive pulse.

The digit drive signals will continue to permit display scanning. $\overline{\text{STROBE}}$ pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active-low $\overline{\text{STROBE}}$ pulses aid BCD data transfer to UARTs, processors and external latches. For more information, please refer to Application Note 784 (DS00784).

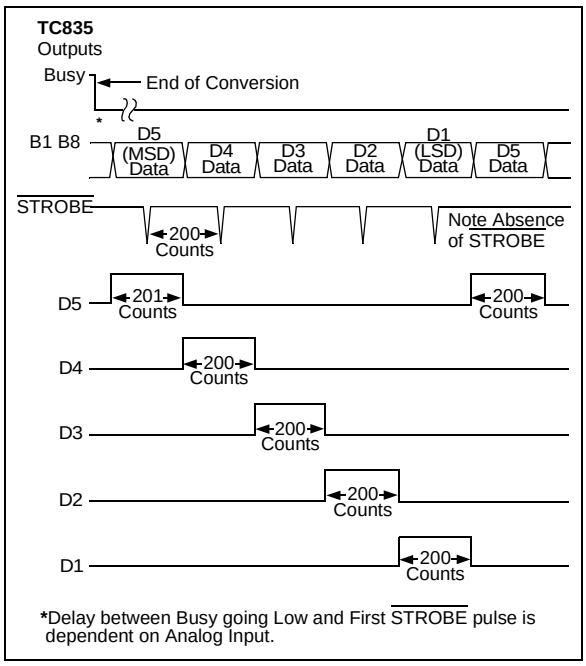


FIGURE 5-3: *Strobe Signal Low Five Times Per Conversion.*

5.3 BUSY Output

At the beginning of the signal integration phase, BUSY goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to the logic '0' state once the measurement cycle ends in an overrange condition. The internal display latches are loaded during the first clock pulse after BUSY and are latched at the clock pulse end. The BUSY signal does not go high at the beginning of the measurement cycle, which starts with the auto-zero cycle.

5.4 OVERRANGE Output

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses, the OVERRANGE output is set to a logic '1'. The OVERRANGE output register is set when BUSY goes low and is reset at the beginning of the next reference integration phase.

5.5 UNDERRANGE Output

If the output count is 9% of full scale or less (-1800 counts), the UNDERRANGE register bit is set at the end of BUSY. The bit is set low at the next signal integration phase.

5.6 POLARITY Output

A positive input is registered by a logic '1' polarity signal. The polarity bit is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

The polarity bit is valid even for a zero reading. Signals less than the converter's LSB will have the signal polarity determined correctly. This is useful in null applications.

5.7 Digit Drive Outputs

Digit drive signals are positive-going signals. The scan sequence is D_5 to D_1. All positive pulses are 200 clock pulses wide, with the exception D_5, which is 201 clock pulses wide.

All five digits are scanned continuously, unless an overrange condition occurs. In an overrange condition, all digit drives are held low from the final $\overline{\text{STROBE}}$ pulse until the beginning of the next reference integrate phase. The scanning sequence is then repeated. This provides a blinking visual display indication.

5.8 BCD Data Outputs

The binary coded decimal (BCD) bits B_8, B_4, B_2 and B_1 are positive-true logic signals. The data bits become active at the same time as the digit drive signals. In an overrange condition, all data bits are at a logic '0' state.

6.0 TYPICAL APPLICATIONS

6.1 Component Value Selection

6.1.1 INTEGRATING RESISTOR

The integrating resistor R_{INT} is determined by the full-scale input voltage and the output current of the buffer used to charge the integrator capacitor (C_{INT}). Both the buffer amplifier and the integrator have a class A output stage, with 100 µA of quiescent current. A 20 µA drive current gives negligible linearity errors. Values of 5 µA to 40 µA give good results. The exact value of an integrating resistor for a 20 µA current is easily calculated.

EQUATION 6-1:

$$R_{INT} = \frac{Full\ Scale\ Voltage}{20\mu A}$$

6.1.2 INTEGRATING CAPACITOR (C_{INT})

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing that ensures the tolerance build-up will not saturate the integrator swing (approximately 0.3V from either supply). For ±5V supplies and ANALOG COMMON tied to supply ground, a ±3.5V to ±4V full scale integrator swing is adequate. A 0.10 µF to 0.47 µF is recommended. In general, the value of C_{INT} is given by:

EQUATION 6-2:

$$C_{INT} = \frac{[10,000 \times clock\ period] \times I_{INT}}{integrator\ output\ voltage\ swing} = \frac{(10,000)(clock\ period) \times 20\mu A}{integrator\ output\ voltage\ swing}$$

A very important characteristic of the integrating capacitor C_{INT} is that it has low dielectric absorption to prevent rollover or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half scale 0.9999, with any deviation probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

6.1.3 AUTO-ZERO AND REFERENCE CAPACITORS

The size of the auto-zero capacitor has some influence on the noise of the system, with a larger capacitor reducing the noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference and auto-zero capacitors are only important at power-on or when the circuit is recovering from an overload. Smaller or cheaper capacitors can be used if accurate readings are not required for the first few seconds of recovery.

6.1.4 REFERENCE VOLTAGE

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high-quality reference be used where high-accuracy absolute measurements are being made.

6.2 Conversion Timing

6.2.1 LINE FREQUENCY REJECTION

A signal integration period at a multiple of the 60 Hz line frequency will maximize 60 Hz “line noise” rejection. A 100 kHz clock frequency will reject 50 Hz, 60 Hz and 400 Hz noise. This corresponds to five readings per second (see Table 6-1 and Table 6-2).

TABLE 6-1: CONVERSION RATE VS. CLOCK FREQUENCY

Oscillator Frequency (kHz)	Conversion Rate (Conv./Sec.)
100	2.5
120	3
200	5
300	7.5
400	10
800	20
1200	30

TABLE 6-2: LINE FREQUENCY REJECTION VS. CLOCK FREQUENCY

Oscillator Frequency (kHz)	Line Frequency Rejection (Hz)
300	60
200	
150	
120	
100	
40	
33-1/3	
250	50
166-2/3	
125	
100	
100	50, 60,400

The conversion rate is easily calculated:

EQUATION 6-3:

$$Reading\ 1/sec = \frac{Clock\ Frequency\ (Hz)}{4000}$$

6.3 High Speed Operation

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 µsec delay, at a clock frequency of 160 kHz (6 µsec period). Half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50 µV input, 1 to 2 with 150 µV, 2 to 3 at 250 µV, etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above 200 kHz, the instrument will flash "1" on noise peaks, even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the nonlinearity and noise do not increase substantially with frequency, clock rates of up to ~1 MHz may be used. For a fixed clock frequency, the extra count (or counts) caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 160 kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second-order breaks will cause significant nonlinearities in the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in **Section 6.0 "Typical Applications"**. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

6.4 Zero Crossing Flip Flop

The flip flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half clock pulse have died down. False zero crossings caused by clock pulses are not recognized. Of course, the flip flop delays the true zero crossing by up to one count in every instance. If a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of the reference integrate (de-integrate) phase. This one-count delay compensates for the delay of the zero crossing flip flop and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto-zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate so that true ratiometric readings result.

6.5 Generating a Negative Supply

A negative voltage can be generated from the positive supply by using a TC7135 (see Figure 6-1).

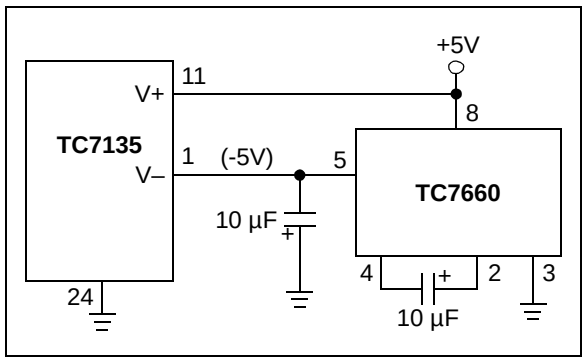


FIGURE 6-1: *Negative Supply Voltage Generator.*

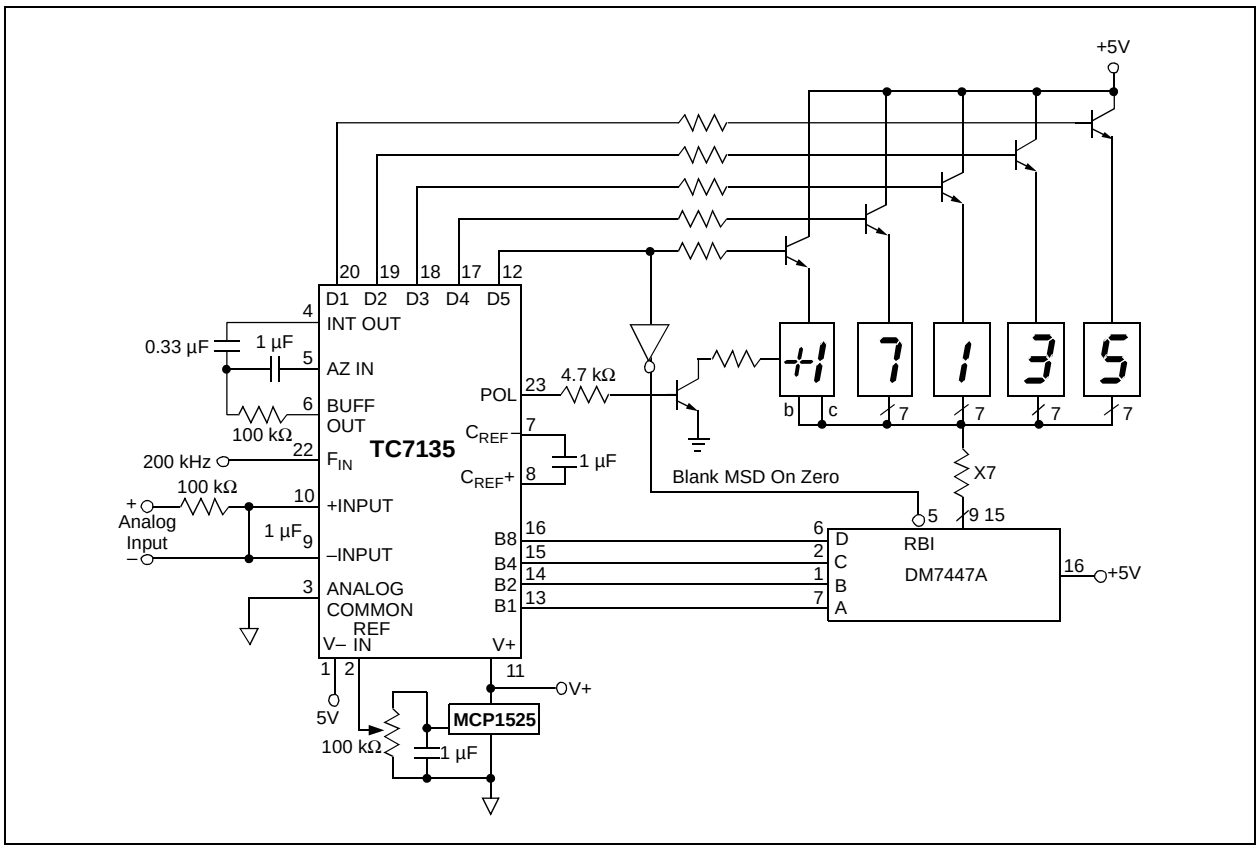
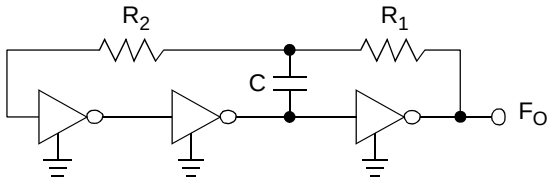


FIGURE 6-2: *4-1/2 Digit ADC With Multiplexed Common Anode Led Display.*



Gates are 74C04

1. $F_O = \frac{1}{2C(0.41R_P + 0.7R_1)}$, $R_P = \frac{R_1 R_2}{R_1 + R_2}$

   a. If $R_1 = R_2 = R_1$, F≅ 0.55/RC
   b. If $R_2 >> R_1$, F ≅ 0.45/R_1C
   c. If $R_2 << R_1$, F ≅ 0.72/R_1C

2. Examples:
   a. F = 120 kHz, C = 420 pF
      $R_1 = R_2 \approx 10.9$ kΩ
   b. F = 120 kHz, C = 420pF, R_2 = 50 kΩ
      R_1 = 8.93 kΩ
   c. F = 120 kHz, C = 220 pF, R_2 = 5 kΩ
      R_1 = 27.3 kΩ

FIGURE 6-3: *RC Oscillator Circuit.*

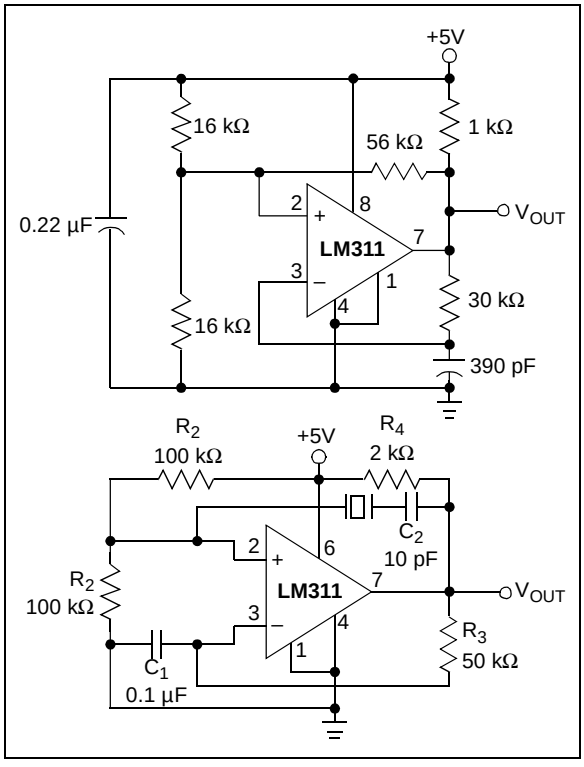


FIGURE 6-4: *Comparator Clock Circuits.*

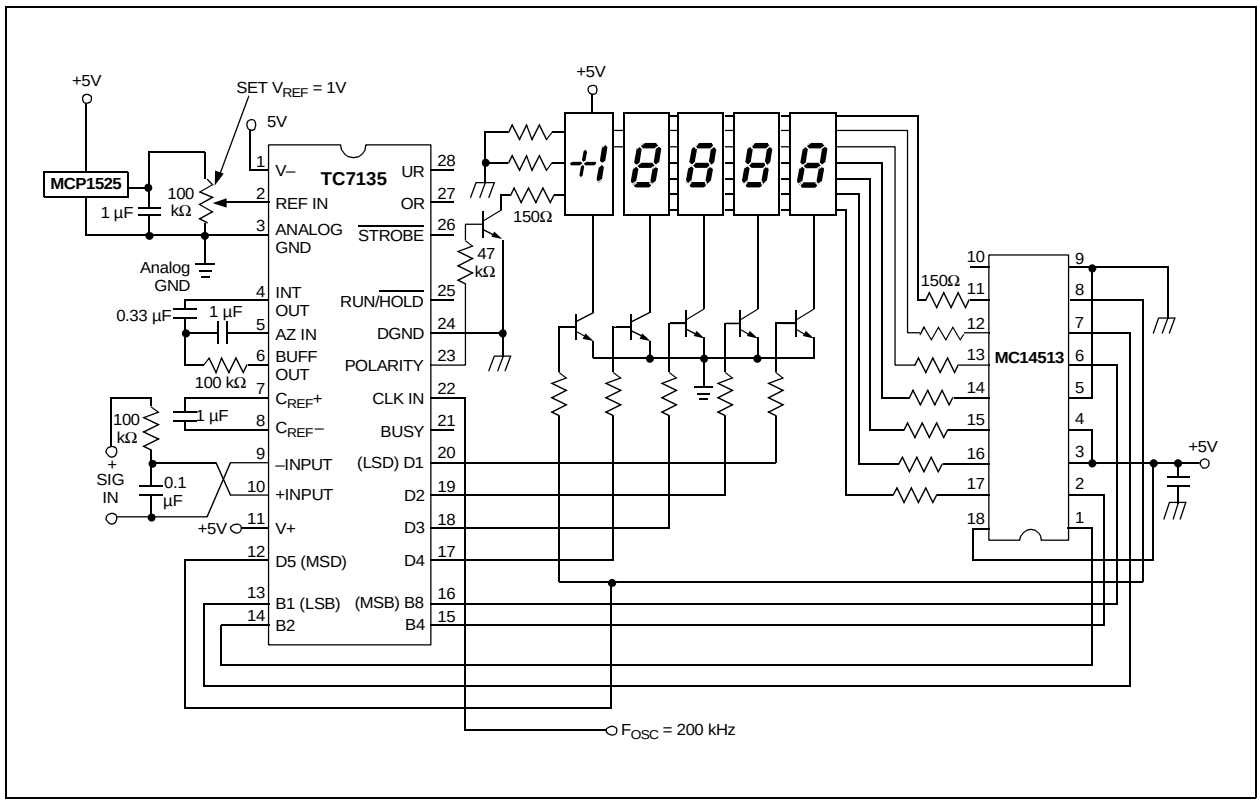
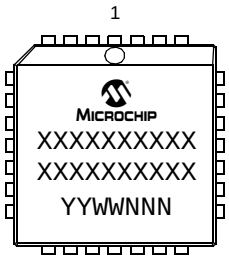


FIGURE 6-5: *4-1/2 Digit ADC With Multiplexed Common Cathode LED Display.*

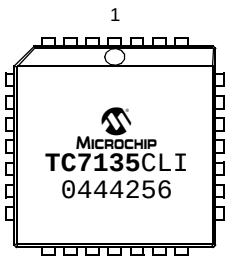
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

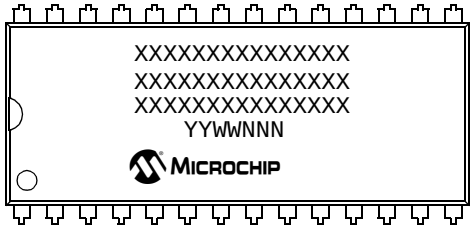
28-Pin PLCC



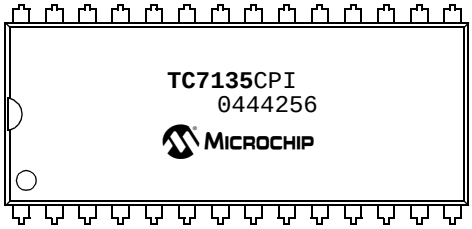
Example:



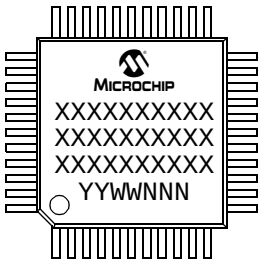
28-Pin PDIP (Wide)



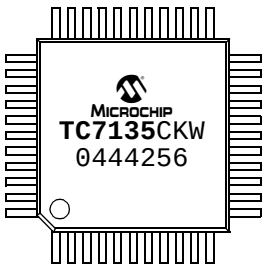
Example:



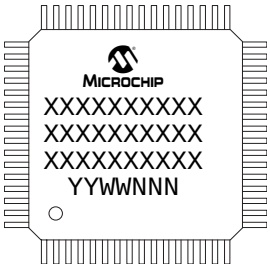
44-Pin MQFP



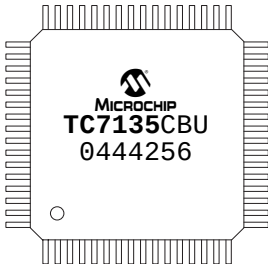
Example:



64-Pin MQFP



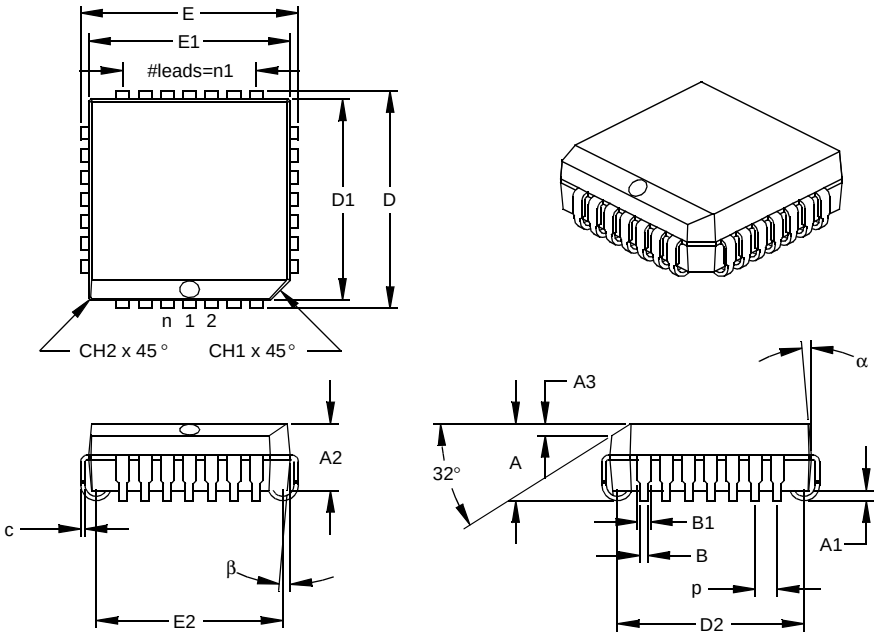
Example:



Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

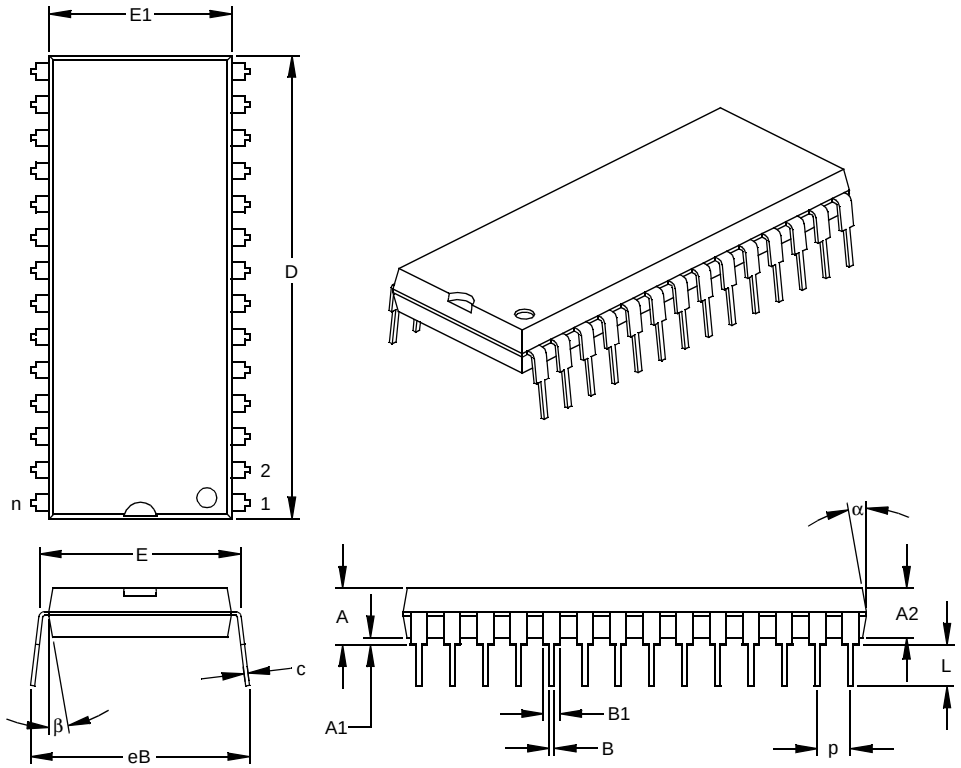
28-Lead Plastic Leaded Chip Carrier (LI) – Square (PLCC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.050			1.27	
Pins per Side	n1		7			7	
Overall Height	A	.165	.173	.180	4.19	4.39	4.57
Molded Package Thickness	A2	.145	.153	.160	3.68	3.87	4.06
Standoff §	A1	.020	.028	.035	0.51	0.71	0.89
Side 1 Chamfer Height	A3	.021	.026	.031	0.53	0.66	0.79
Corner Chamfer 1	CH1	.035	.045	.055	0.89	1.14	1.40
Corner Chamfer (others)	CH2	.000	.005	.010	0.00	0.13	0.25
Overall Width	E	.485	.490	.495	12.32	12.45	12.57
Overall Length	D	.485	.490	.495	12.32	12.45	12.57
Molded Package Width	E1	.450	.453	.456	11.43	11.51	11.58
Molded Package Length	D1	.450	.453	.456	11.43	11.51	11.58
Footprint Width	E2	.410	.420	.430	10.41	10.67	10.92
Footprint Length	D2	.410	.420	.430	10.41	10.67	10.92
Lead Thickness	c	.008	.011	.013	0.20	0.27	0.33
Upper Lead Width	B1	.026	.029	.032	0.66	0.74	0.81
Lower Lead Width	B	.013	.020	.021	0.33	0.51	0.53
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MO-047
Drawing No. C04-026

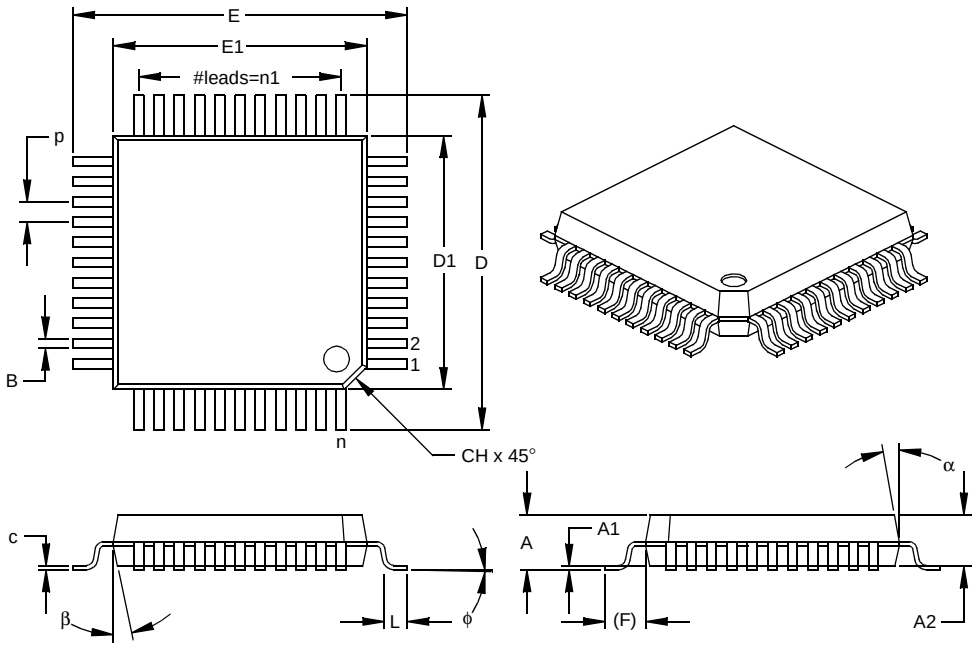
28-Lead Plastic Dual In-line (PI) – 600 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.175	.190	4.06	4.45	4.83
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.505	.545	.560	12.83	13.84	14.22
Overall Length	D	1.395	1.430	1.465	35.43	36.32	37.21
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-011
Drawing No. C04-079

44-Lead Plastic Metric Quad Flatpack (KW) 10x10x2 mm Body, Lead Form (MQFP)

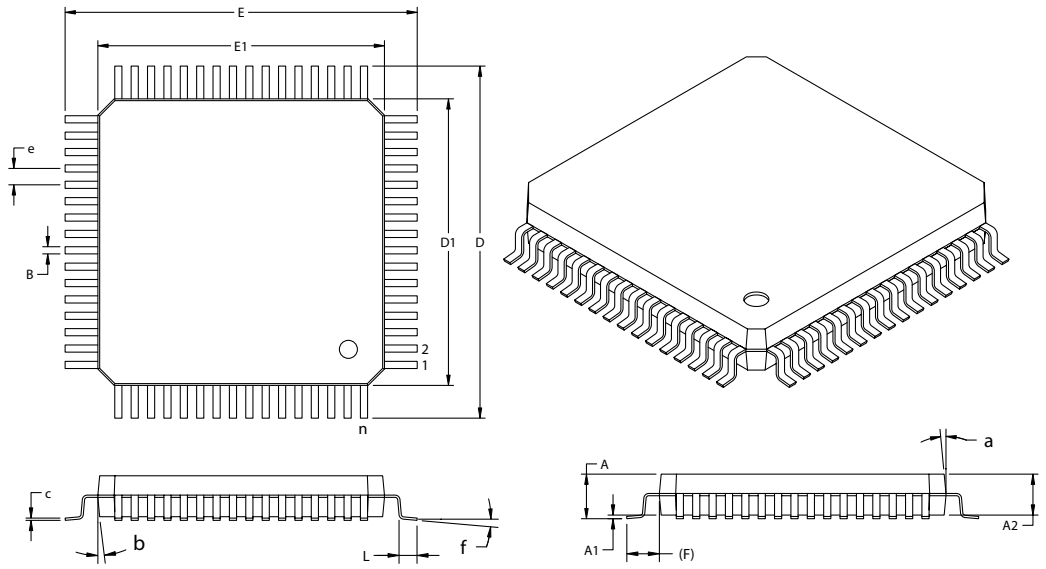


Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	p		.031			0.80	
Pins per Side	n1		11			11	
Overall Height	A	.079	.086	.093	2.00	2.18	2.35
Molded Package Thickness	A2	.077	.080	.083	1.95	2.03	2.10
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Foot Length	L	.029	.035	.041	0.73	0.88	1.03
Footprint (Reference)	(F)		.063			1.60	
Foot Angle	φ	0	3.5	7	0	3.5	7
Overall Width	E	.510	.520	.530	12.95	13.20	13.45
Overall Length	D	.510	.520	.530	12.95	13.20	13.45
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	c	.005	.007	.009	0.13	0.18	0.23
Lead Width	B	.012	.015	.018	0.30	0.38	0.45
Pin 1 Corner Chamfer	CH	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-022
Drawing No. C04-071

64 Lead Metric Plastic Quad Flat (BU) (MQFP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		64			64	
Pitch	e		.031 BSC			0.80 BSC	
Overall Height	A	.098	--	.124	2.50	--	3.15
Molded Package Thickness	A2	.098	.106	.114	2.50	2.70	2.90
Standoff §	A1	.000	--	.010	0.00	--	0.25
Overall Width	E		.677 BSC			17.20 BSC	
Molded Package Width	E1		.551 BSC			14.00 BSC	
Overall Length	D		.677 BSC			17.20 BSC	
Molded Package Length	D1		.551 BSC			14.00 BSC	
Foot Length	L	.029	.035	.041	0.73	0.88	1.03
Footprint (Reference)	(F)		.063 REF			1.60 REF	
Foot Angle	f	0°	--	6°	0°	--	7°
Lead Thickness	c	.004	--	.009	0.11	--	0.23
Lead Width	B	.011	--	.018	0.29	--	0.45
Mold Draft Angle Top	a	5°	--	16°	5°	--	16°
Mold Draft Angle Bottom	b	5°	--	16°	5°	--	16°

*Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC equivalent: MS-022 BE.

Formerly TelCom PQFP package.

Drawing No. C04-022

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device	TC7135: 4-1/2 Digit A/D, BCD Output	
Temperature Range	C	= 0°C to +70°C
Package	LI	= Plastic Leaded Chip Carrier (PLCC), 28-lead
	LI713	= Plastic Leaded Chip Carrier (PLCC), 28-lead, Tape and Reel
	PI	= Plastic DIP, (600 mil Body), 28-lead
	KW	= Plastic Metric Quad Flatpack, (MQFP), 44-lead
	BU	= Plastic Metric Quad Flatpack, (MQFP), 64-lead

Examples:

a) TC7135CLI: 4-1/2 Digit A/D, BCD Output, PLCC package.

b) TC7135CPI: 4-1/2 Digit A/D, BCD Output, PDIP package.

c) TC7135CLI713: 4-1/2 Digit A/D, BCD Output, PLCC package, Tape and Reel.

d) TC7135CBU: 4-1/2 Digit A/D, BCD Output, MQFP package.

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