

# TC74ACT164P, TC74ACT164F

## 8-Bit Shift Register (S-IN, P-OUT)

The TC74ACT164 is an advanced high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

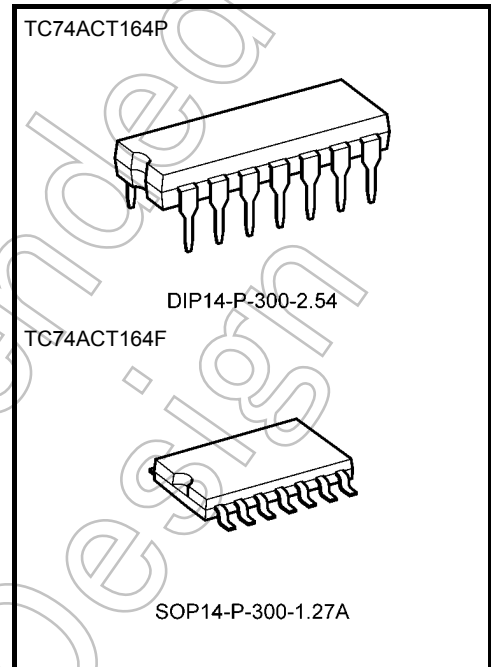
It consists of a serial-in, parallel-out 8-bit shift register with a CLOCK input and an overriding CLEAR input.

Two serial data inputs (A, B) are provided so that one may be used as a data enable.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

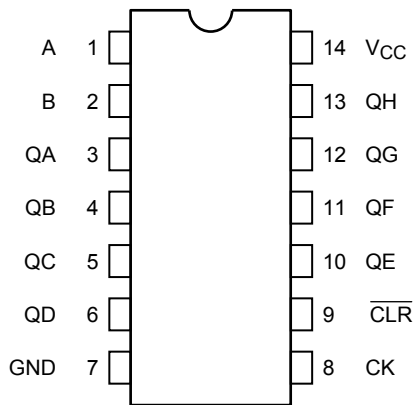
- High speed:  $f_{max} = 200 \text{ MHz (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 8 \mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs:  $V_{IL} = 0.8 \text{ V (max)}$   
 $V_{IH} = 2.0 \text{ V (max)}$
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$   
Capability of driving  $50 \Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F164



Weight	
DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)

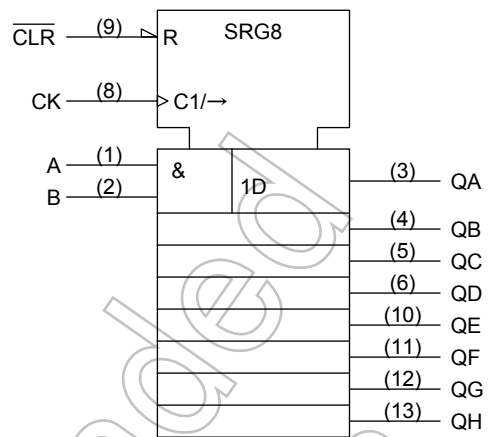
Start of commercial production  
1989-11

**Pin Assignment**



(top view)

**IEC Logic Symbol**



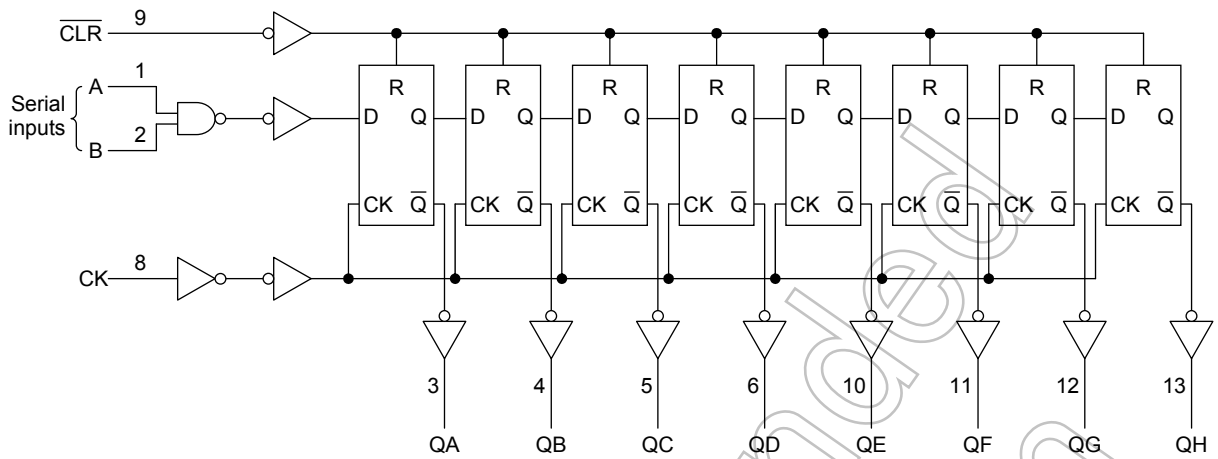
**Truth Table**

Inputs				Outputs			
CLR	CK	Serial IN		QA	QB	...	QH
		A	B				
L	X	X	X	L	L	...	L
H		X	X	No change			
H		L	X	L	QA <sub>n</sub>	...	QG <sub>n</sub>
H		X	L	L	QA <sub>n</sub>	...	QG <sub>n</sub>
H		H	H	H	QA <sub>n</sub>	...	QG <sub>n</sub>

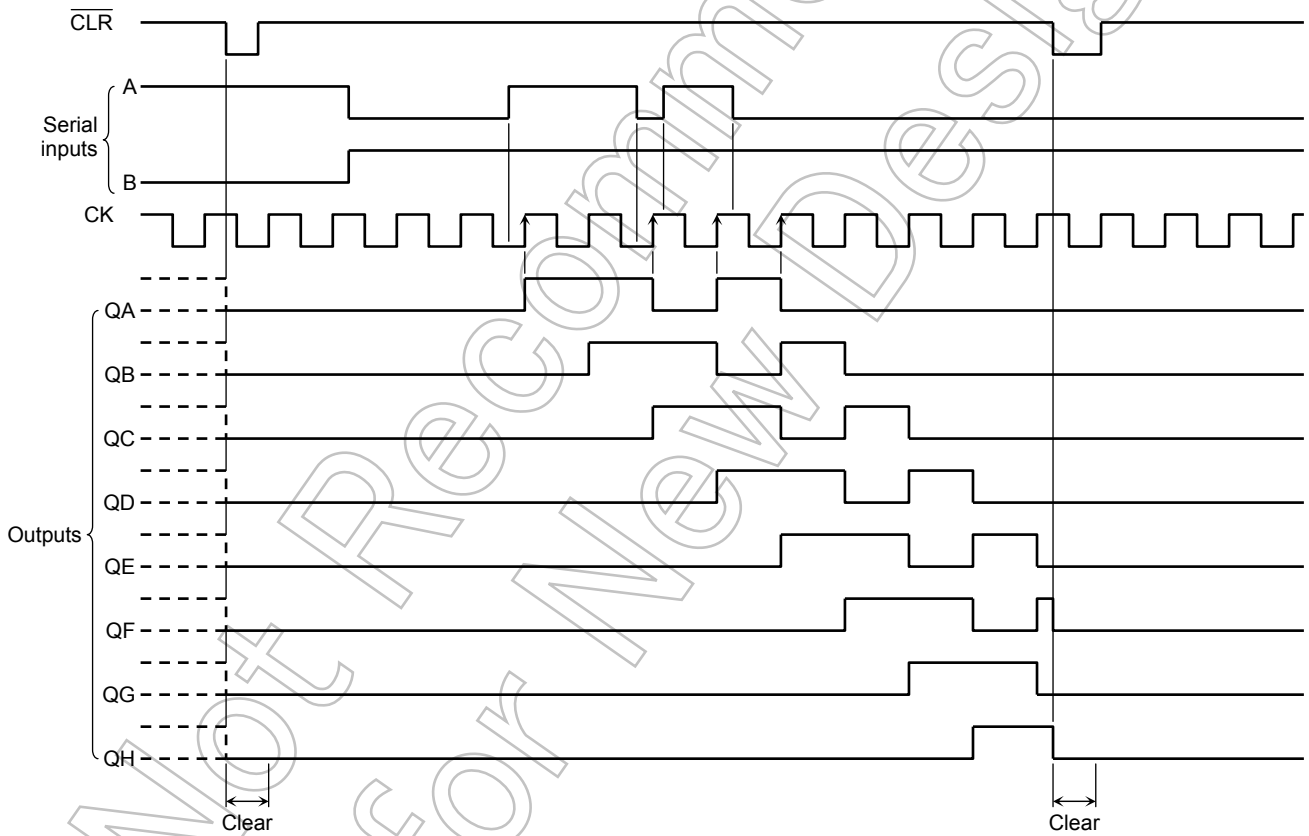
X : Don't care

QA<sub>n</sub>~QG<sub>n</sub>: The level of QA~QG, respectively, before the most recent positive edge of the clock.

**System Diagram**



**Timing Chart**



**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 50$	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 200$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}\text{C}$ . From  $T_a = 65$  to  $85^{\circ}\text{C}$  a derating factor of  $-10$  mW/ $^{\circ}\text{C}$  should be applied up to 300mW.

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}\text{C}$
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to 85°C		Unit
				Min	Typ.	Max	Min	Max	
High-level input voltage	V <sub>IH</sub>		4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V <sub>IL</sub>		4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -75 mA (Note)	4.5	4.4	4.5	—	4.4	—	V
			4.5	3.94	—	—	3.80	—	
			5.5	—	—	—	3.85	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 75 mA (Note)	4.5	—	0.0	0.1	—	0.1	V
			4.5	—	—	0.36	—	0.44	
			5.5	—	—	—	—	1.65	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	8.0	—	80.0	
		I <sub>C</sub>	PER Input: V <sub>IN</sub> = 3.4 V Other input: V <sub>CC</sub> or GND	5.5	—	—	1.35	—	1.5

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

### Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C		Limit	Unit
				Typ.	Limit	Limit	
Minimum pulse width (CK)	t <sub>W</sub> (L) t <sub>W</sub> (H)		5.0 ± 0.5	—	5.0	5.0	ns
Minimum pulse width (CLR)	t <sub>W</sub> (L)		5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time	t <sub>s</sub>		5.0 ± 0.5	—	3.0	3.0	
Minimum hold time	t <sub>h</sub>		5.0 ± 0.5	—	2.6	2.6	
Minimum removal time (CLR)	t <sub>rem</sub>		5.0 ± 0.5	—	2.0	2.0	

### AC Characteristics ( $C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$ , input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
Propagation delay time (CK-Q)	$t_{pLH}$ $t_{pHL}$		5.0 ± 0.5	—	6.6	11.0	1.0	12.5	ns
Propagation delay time (CLR-Q)	$t_{pHL}$		5.0 ± 0.5	—	6.9	11.0	1.0	12.5	
Maximum clock frequency	$f_{max}$		5.0 ± 0.5	80	150	—	80	—	MHz
Input capacitance	$C_{IN}$			—	5	10	—	10	pF
Power dissipation capacitance	$C_{PD}$ (Note)			—	101	—	—	—	

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

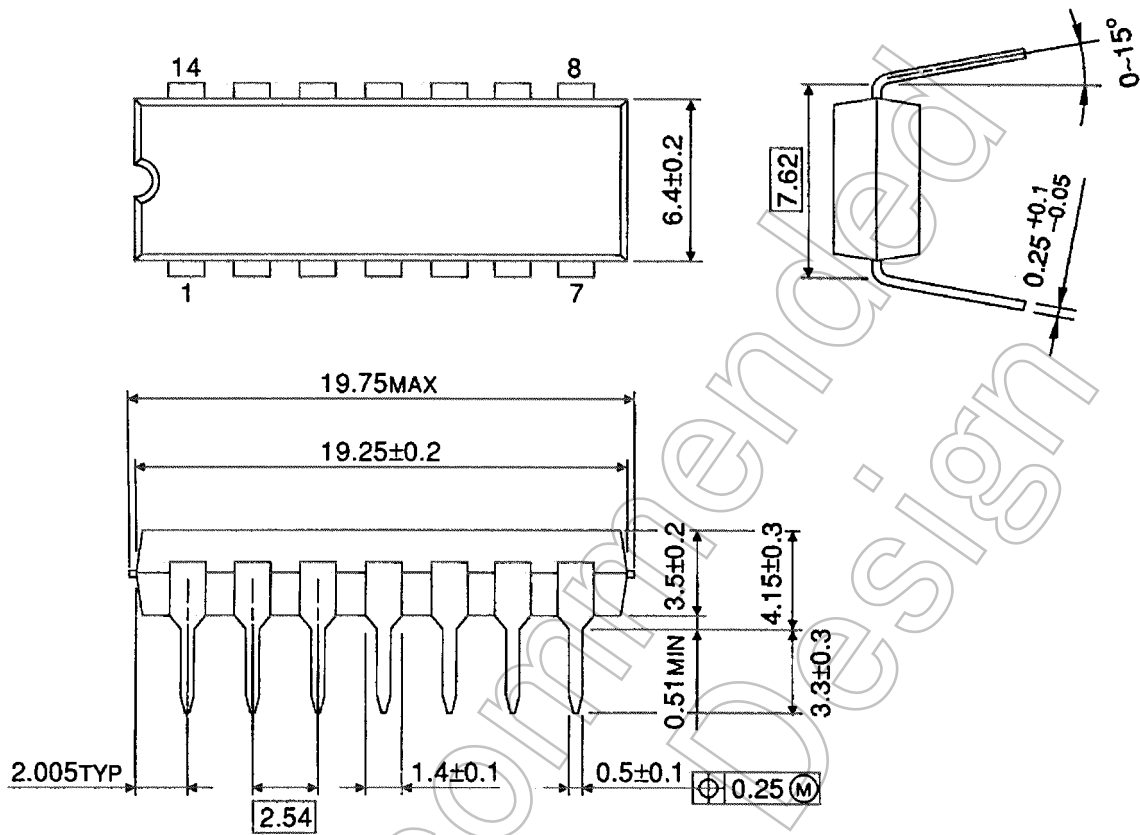
$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Not Recommended for New Design

**Package Dimensions**

DIP14-P-300-2.54

Unit : mm



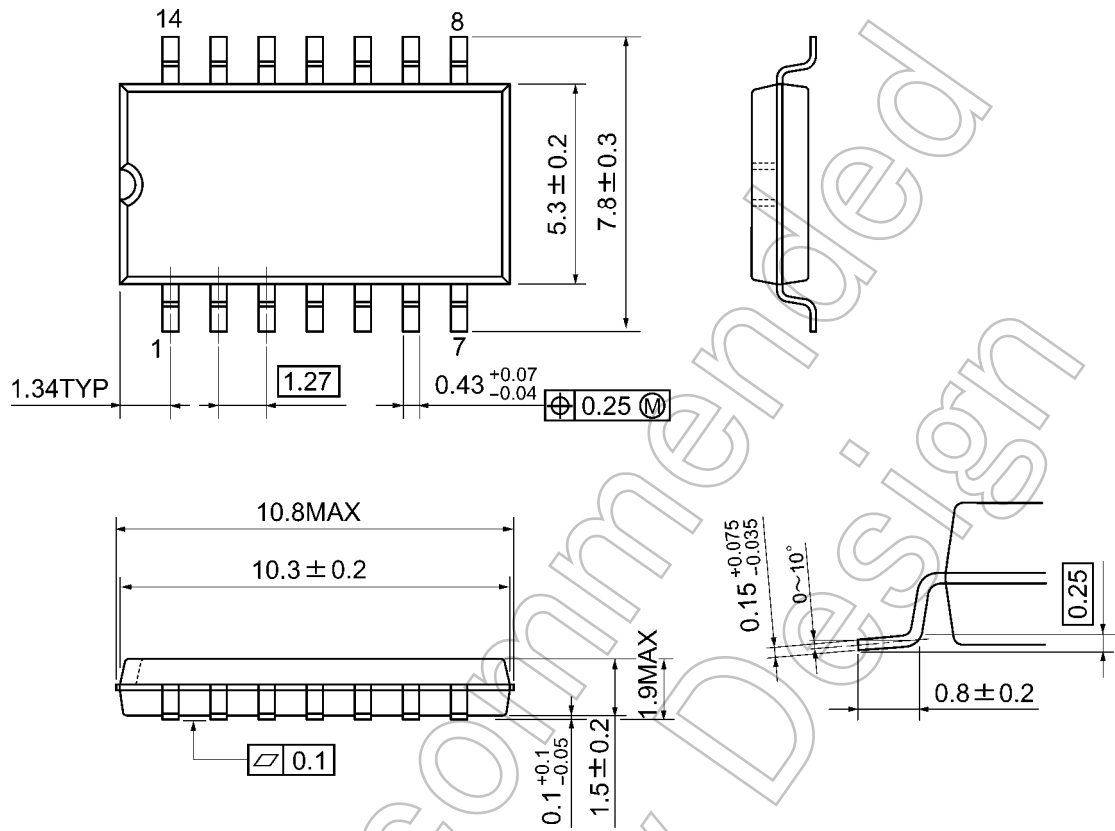
Weight: 0.96 g (typ.)

Not Recommended for New Design

**Package Dimensions**

SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

Not Recommended for New Design



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