TC826

Analog-to-Digital Converter with Bar Graph Display Output

Features

- Bipolar A/D Conversion
- 2.5% Resolution
- Direct LCD Display Drive
- 'Thermometer' BAR or DOT Display
- 40 Data Segments Plus Zero
- Over Range Plus Polarity Indication
- Precision On-Chip Reference: 35ppm/°C
- Differential Analog Input
- Low Input Leakage: 10pA
- Display Flashes on Over Range
- Display HOLD Mode
- Auto-Zero Cycle Eliminates Zero Adjust Potentiometer
- 9V Battery Operation
- Low Power Consumption: 1.1mW
- 20mV to 2.0V Full Scale Operation
- Non-Multiplexed LCD Drive for Maximum Viewing Angle

Device Selection Table

Part Number	Package	Temperature Range
TC826CBU	64-Pin PQFP	0°C to +70°C

General Description

In many applications, a graphical display is preferred over a digital display. Knowing a process or system operates, for example, within design limits is more valuable than a direct system variable read out. A bar or moving dot display supplies information precisely without requiring further interpretation by the viewer.

The TC826 is a complete analog-to-digital converter with direct liquid crystal (LCD) display drive. The 40 LCD data segments plus zero driver give a 2.5% resolution bar display. Full scale differential input voltage range extends from 20mV to 2V. The TC826 sensitivity is 500µV. A low drift 35ppm/°C internal reference, LCD backplane oscillator and driver, input polarity LCD driver, and over range LCD driver make designs simple and low cost. The CMOS design required only 125µA from a 9V battery. In +5V systems, a TC7660 DC to DC converter can supply the -5V supply. The differential analog input leakage is a low 10pA.

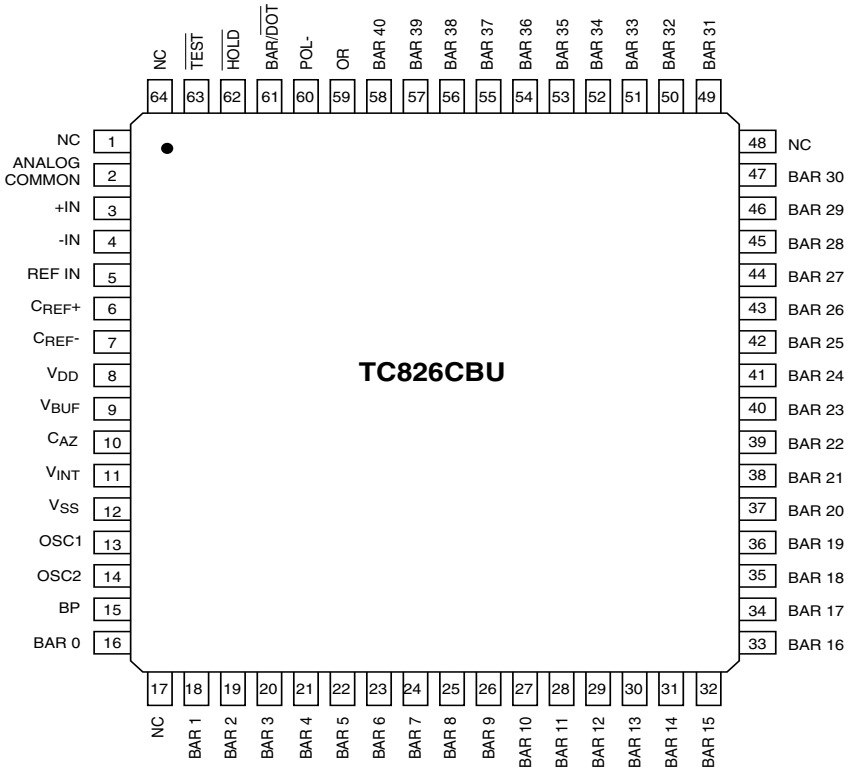
Two display formats are possible. The BAR mode display is like a 'thermometer' scale. The LCD segment driver that equals the input, plus all below it are on. The DOT mode activates only the segment equal to the input. In either mode, the polarity signal is active for negative input signals. An over range input signal causes the display to flash and activates the over range annunciator. A HOLD mode can be selected that freezes the display and prevents updating.

The dual slope integrating conversion method with auto-zero phase maximizes noise immunity and eliminates zero scale adjustment potentiometers. Zero scale drift is a low 5µV/°C. Conversion rate is typically 5 per second and is adjustable by a single external resistor.

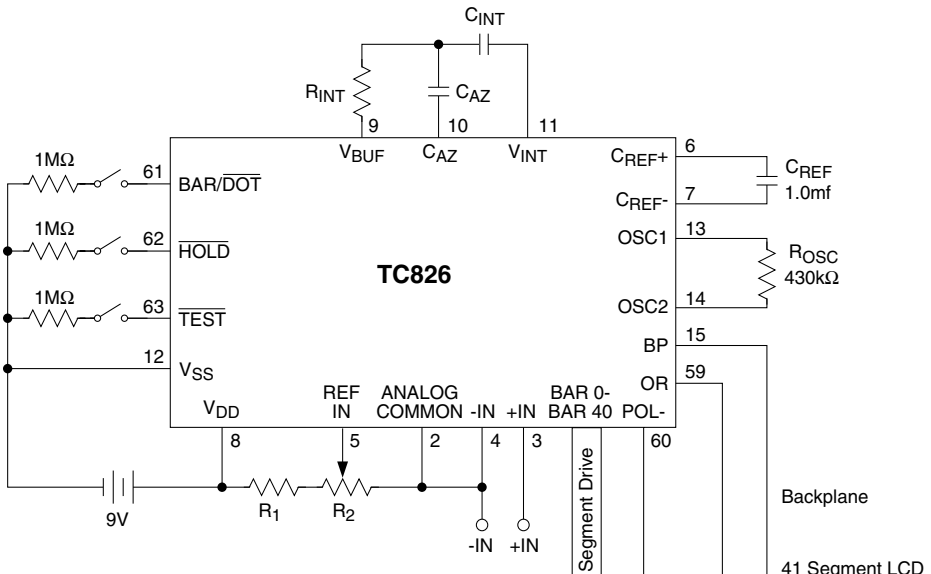
A compact, 0.5" square, flat package minimizes PC board area. The high pin count LSI package makes multiplexed LCD displays unnecessary. Low cost, direct drive LCD displays offer the widest viewing angle and are readily available. A standard display is available now for TC826 prototyping work.

Package Type

64-Pin PQFP



Typical Application



Component	2V Full Scale	200mV Full Scale	20mV Full Scale
R_{INT}	2MΩ	20kΩ	20kΩ
C_{INT}	0.033mf	0.033mf	0.033mf
C_{REF}	1mf	1mf	1mf
C_{AZ}	0.068mf	0.068mf	0.014mf

$R_1 + R_2 = 250k\Omega$

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V+ to V-) 15V

Analog Input Voltage (Either Input) **(Note 1)**... V+ to V-

Power Dissipation ($T_A \leq 70°C$)
64-Pin Plastic Flat Package 1.14W

Operating Temperature Range:
Commercial Package (C) ..... 0°C to +70°C

Storage Temperature Range ..... -65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC826 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_S = 9V; R_{OSC} = 430kΩ; T_A = 25°C; Full Scale = 20mV, unless otherwise stated.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
	Zero Input	-0	±0	+0	Display	V_{IN} = 0.0V
	Zero Reading Drift	—	0.2	1	µV/°C	V_{IN} = 0.0V 0°C ≤ T_A ≤ +70°C
NL	Linearity Error	-1	0.5	+1	Count	Max Deviation from Best Straight Line
R/O	Rollover Error	-1	0	+1	Count	$-V_{IN} = +V_{IN}$
EN	Noise	—	60	—	μV_{P-P}	V_{IN} = 0V
ILK	Input Leakage Current	—	10	20	pA	V_{IN} = 0V
CMRR	Common Mode Rejection Ratio	—	50	—	µV/V	VCM = ±1V V_{IN} = 0V
	Scale Factor Temperature Coefficient	—	1	—	ppm/°C	0 ≤ T_A ≤ 7 +0°C External Ref. Temperature Coefficient = 0ppm/°C
V_{CTC}	Analog Common Temperature Coefficient	—	35	100	ppm/°C	250kΩ between Common and V+, 0°C ≤ T_A ≤ +70°C
V_{COM}	Analog Common Voltage	2.7	2.9	3.35	V	250kΩ between Common and V_{DD}
VSD	LCD Segment Drive Voltage	4	5	6	V_{P-P}	
VBD	LCD Backplane Drive Voltage	4	5	6	V_{P-P}	
I_{DD}	Power Supply Current	—	125	175	µA	

Note 1: Input voltages may exceed the supply voltages when the input current is limited to 100µA.

2: Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.

3: Backplane drive is in phase with segment drive for 'off' segment and 180°C out of phase for 'on' segment. Frequency is 10 times conversion rate.

4: Logic input pins 58, 59, and 60 should be connected through 1MΩ series resistors to V_{SS} for logic 0.

2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number (64-Pin PQFP)	Symbol	Description
1	NC	Positive analog signal input.
2	ANALOG COMMON	Establishes the internal analog ground point. Analog common is set to 2.9V below the positive supply COMMON by an internal zener reference circuit. The voltage difference between V_{DD} and analog common can be used to supply the TC826 voltage reference input at REF IN (Pin 5).
3	+IN	Positive analog signal input.
4	-IN	Negative analog signal input.
5	REF IN	Reference voltage positive input. Measured relative to analog common. REF IN ≈ Full Scale/2.
6	C_{REF}+	Reference capacitor connection.
7	C_{REF}-	Reference capacitor connection.
8	V_{DD}	Positive supply terminal.
9	V_{BUF}	Buffer output. Integration resistor connection.
10	C_{AZ}	Negative comparator input. Auto-zero capacitor connection.
11	V_{INT}	Integrator output. Integration capacitor connection.
12	V_{SS}	Negative supply terminal.
13	OSC1	Oscillator resistor (R_{OSC}) connection.
14	OSC2	Oscillator resistor (R_{OSC}) connection.
15	BP	LCD Backplane driver.
16	BAR 0	LCD Segment driver: Bar 0.
17	NC	No connection.
18	BAR 1	LCD Segment driver: Bar 1.
19	BAR 2	LCD Segment driver: Bar 2.
20	BAR 3	LCD Segment driver: Bar 3.
21	BAR 4	LCD Segment driver: Bar 4.
22	BAR 5	LCD Segment driver: Bar 5.
23	BAR 6	LCD Segment driver: Bar 6.
24	BAR 7	LCD Segment driver: Bar 7.
25	BAR 8	LCD Segment driver: Bar 8.
26	BAR 9	LCD Segment driver: Bar 9.
27	BAR 10	LCD Segment driver: Bar 10.
28	BAR 11	LCD Segment driver: Bar 11.
29	BAR 12	LCD Segment driver: Bar 12.
30	BAR 13	LCD Segment driver: Bar 13.
31	BAR 14	LCD Segment driver: Bar 14.
32	BAR 15	LCD Segment driver: Bar 15.
33	BAR 16	LCD Segment driver: Bar 16.
34	BAR 17	LCD Segment driver: Bar 17.
35	BAR 18	LCD Segment driver: Bar 18.
36	BAR 19	LCD Segment driver: Bar 19.
37	BAR 20	LCD Segment driver: Bar 20.
38	BAR 21	LCD Segment driver: Bar 21.
39	BAR 22	LCD Segment driver: Bar 22.
40	BAR 23	LCD Segment driver: Bar 23.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (64-Pin PQFP)	Symbol	Description
41	BAR 24	LCD Segment driver: Bar 24.
42	BAR 25	LCD Segment driver: Bar 25.
43	BAR 26	LCD Segment driver: Bar 26.
44	BAR 27	LCD Segment driver: Bar 27.
45	BAR 28	LCD Segment driver: Bar 28.
46	BAR 29	LCD Segment driver: Bar 29.
47	BAR 30	LCD Segment driver: Bar 30.
48	NC	No connection.
49	BAR 31	LCD Segment driver: Bar 31.
50	BAR 32	LCD Segment driver: Bar 32.
51	BAR 33	LCD Segment driver: Bar 33.
52	BAR 34	LCD Segment driver: Bar 34.
53	BAR 35	LCD Segment driver: Bar 35.
54	BAR 36	LCD Segment driver: Bar 36.
55	BAR 37	LCD Segment driver: Bar 37.
56	BAR 38	LCD Segment driver: Bar 38.
57	BAR 39	LCD Segment driver: Bar 39.
58	BAR 40	LCD Segment driver: Bar 40.
59	OR	LCD segment driver that indicated input out-of-range condition.
60	POL-	LCD segment driver that indicates input signal is negative.
61	BAR/$\overline{\text{DOT}}$	Input logic signal that selects BAR or DOT display format. Normally in BAR mode. Connect to V_{SS} through 1MΩ resistor for DOT format.
62	$\overline{\text{HOLD}}$	Input logic signal that prevents display from changing. Pulled high internally to inactive state. Connect to V_{SS} through 1MΩ series resistor for HOLD mode operation.
63	$\overline{\text{TEST}}$	Input logic signal. Sets TC826 to BAR Display mode. BAR 0 to 40, plus OR flash on and off. The POL- LCD driver is on. Pulled high internally to inactive state. Connect to V_{SS} with 1MΩ series resistor to activate.
64	NC	No connection.

3.0 DETAILED DESCRIPTION

3.1 Dual Slope Conversion Principles

The TC826 is a dual slope, integrating analog-to-digital converter. The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (De-integration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}) (Figure 3-1).

In a simple dual slope converter, a complete conversion requires the integrator output to 'ramp-up' and 'ramp-down'.

A simple mathematical equation relates the input signal reference voltage and integration time:

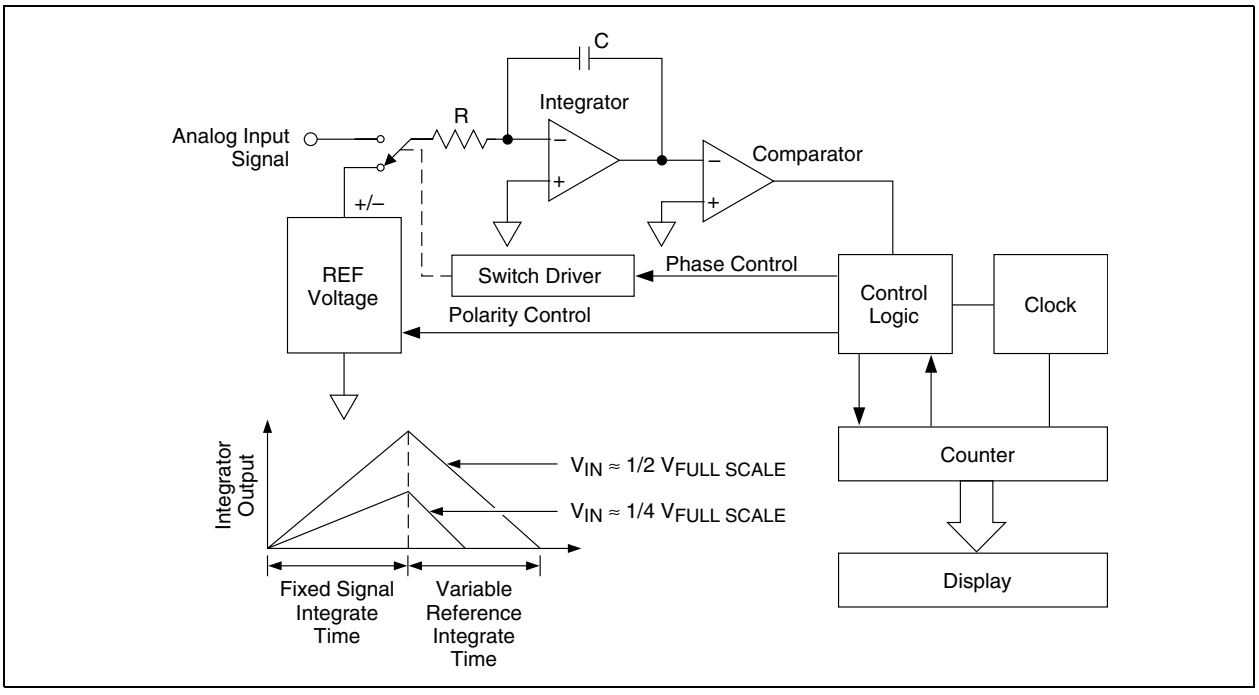
EQUATION 3-1:

$$\frac{1}{RC}\int_0^{t_{INT}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

Where:

V_R = Reference Voltage
V_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

FIGURE 3-1: BASIC DUAL SLOPE CONVERTER



For a constant V_{IN}:

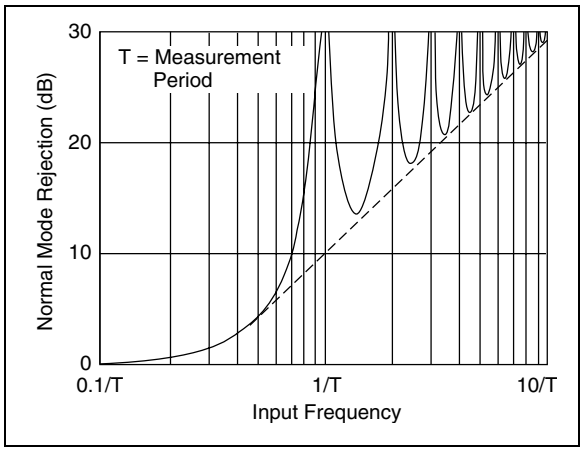
EQUATION 3-2:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated (Figure 3-2).

The TC826 converter improves the conventional dual slope conversion technique by incorporating an auto-zero phase. This phase eliminates zero scale offset errors and drift. A potentiometer is not required to obtain a zero output for zero input.

FIGURE 3-2: NORMAL MODE REJECTION OF DUAL SLOPE CONVERTER



4.0 THEORY OF OPERATION

4.1 Analog Section

In addition to the basic signal integrate and de-integrate cycles discussed above, the TC826 incorporates an auto-zero cycle.This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference cycle (Figure 4-1 and Figure 4-2).

4.1.1 AUTO-ZERO CYCLE

During the auto-zero cycle, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (internal analog ground) to establish a zero input condition. Additional analog gates close a feedback loop around the offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages.

The auto-zero cycle length is 19 counts minimum. Unused time in the de-integrate cycle is added to the auto-zero cycle.

4.1.2 SIGNAL INTEGRATION CYCLE

The auto-zero loop is opened and the internal differential inputs connect to +IN and -IN. The differential input signal is integrated for a fixed time period. The TC826 signal integration period is 20 clock periods or counts. The externally set clock frequency is divided by 32 before clocking the internal counters. The integration time period is:

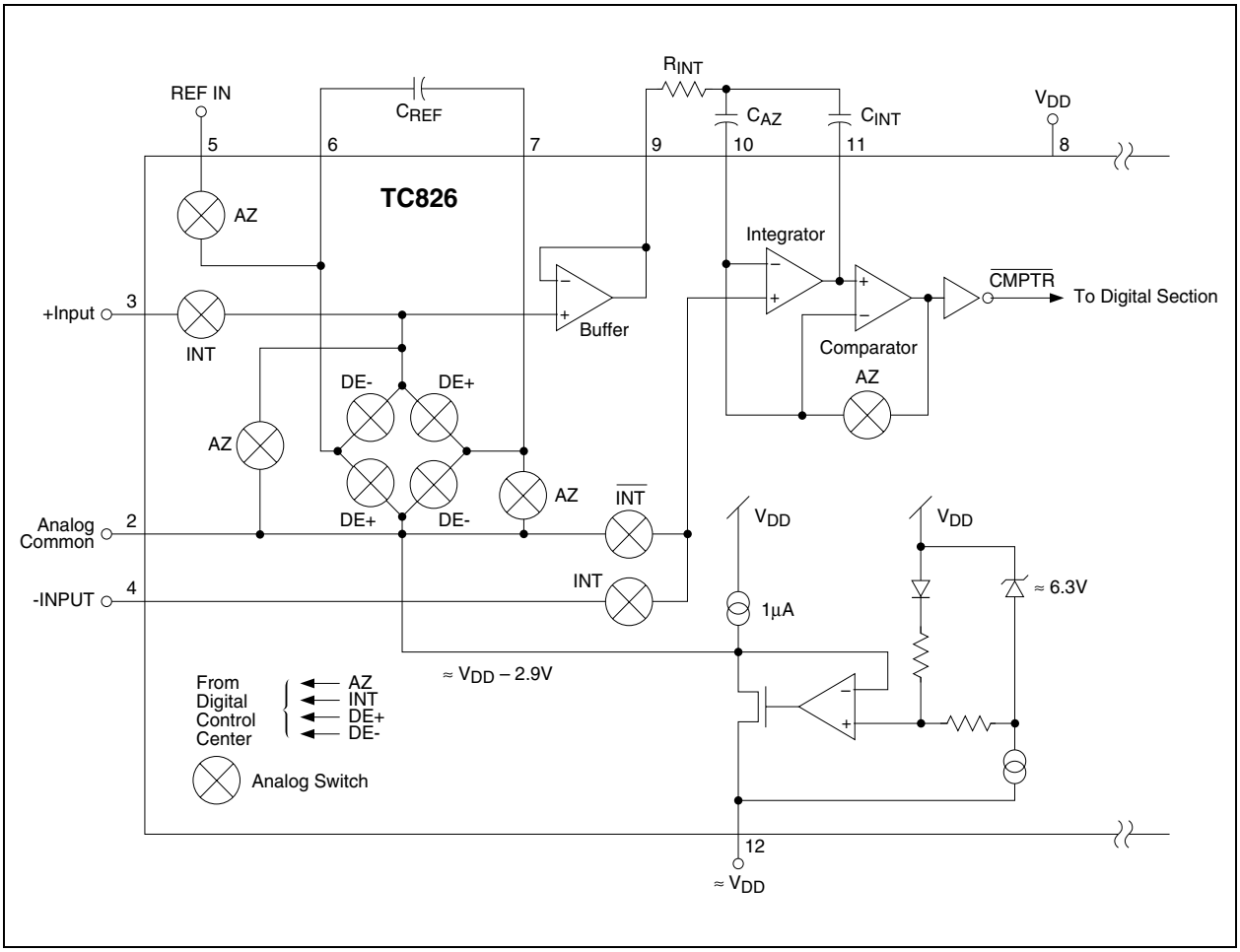
EQUATION 4-1:

Where:

$$T_{SI} = \frac{32}{F_{OSC}} \times 20$$

F_{OSC} = External Clock Frequency

FIGURE 4-1: TC826 ANALOG SECTION



The differential input voltage must be within the device Common mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, -IN should be tied to analog common. This is the usual connection for battery operated systems. Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication, in that signals less than 1LSB are correctly determined. This allows precision null detection limited only by device noise and system noise.

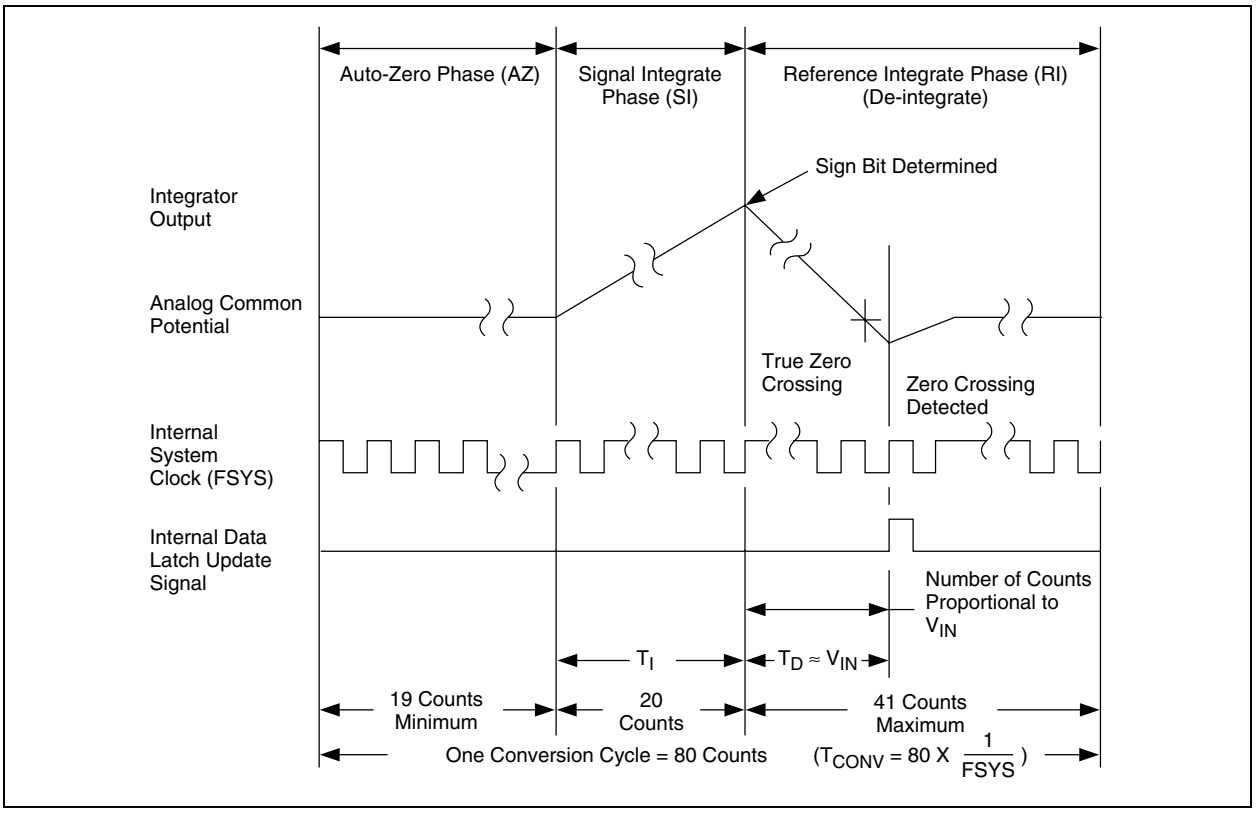
4.1.3 REFERENCE INTEGRATE CYCLE

The final phase is reference integrate or de-integrate. -IN is internally connected to analog common and +IN is connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 40 counts. The digital reading displayed is:

EQUATION 4-2:

$$20 = \frac{V_{IN}}{V_{REF}}$$

FIGURE 4-2: CONVERSION HAS THREE PHASES



4.2 System Timing

The oscillator frequency is divided by 32 prior to clocking the internal counters. The three-phase measurement cycle takes a total of 80 clock pulses. The 80 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 19 to 59 Counts
  For signals less than full scale, the auto-zero is assigned the unused reference integrate time period.
- Signal Integrate: 20 Counts
  This time period is fixed. The integration period is:

EQUATION 4-3:

$$T_{SI} = 20\left(\frac{32}{F_{OSC}}\right)$$

Where F_{OSC} is the externally set clock frequency.

- Reference Integrate: 0 to 41 Counts

4.3 Reference Voltage Selection

A full scale reading requires the input signal be twice the reference voltage. The reference potential is measured between REF IN (Pin 5) and ANALOG COMMON (Pin 2).

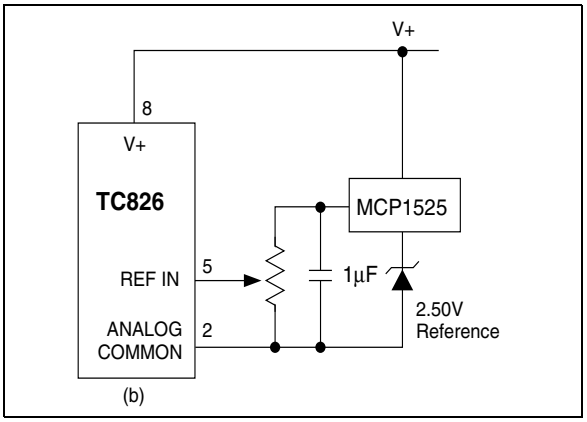
TABLE 4-1:

Required Full Scale Voltage	V_{REF}
20mV	10mV
2V	1V

The internal voltage reference potential available at analog common will normally be used to supply the converter's reference. This potential is stable whenever the supply potential is greater than approximately 7V. In applications where an externally generated reference voltage is desired, refer to Figure 4-3.

The reference voltage is adjusted with a near full scale input signal. Adjust for proper LCD display read out.

FIGURE 4-3: EXTERNAL REFERENCE



4.4 Components Value Selection

4.4.1 INTEGRATING RESISTOR (R_{INT})

The desired full scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 1µA drive current with minimal linearity error. R_{INT} is easily calculated for a 1µA full scale current:

EQUATION 4-4:

$$R_{INT} = \frac{\text{Full Scale Voltage(V)}}{1 \times 10 - 6} = \frac{V_{FS}}{1 \times 10 - 6}$$

Where V_{FS} = Full Scale Analog Input

4.4.2 INTEGRATING CAPACITOR (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4V of V_S+ or V_S- without saturating.

The integrating capacitor is easily calculated:

EQUATION 4-5:

$$C_{INT} = \frac{V_{FS}}{R_{INT}}\left(\frac{640}{F_{OSC} \times V_{INT}}\right)$$

Where: V_{INT} = Integrator Swing
F_{OSC} = Oscillator Frequency

The integrating capacitor should be selected for low dielectric absorption to prevent rollover errors. Polypropylene capacitors are suggested.

4.4.3 AUTO-ZERO CAPACITOR (C_{AZ})

C_{AZ} should be 2-3 times larger than the integration capacitor. A polypropylene capacitor is suggested. Typical values from 0.14µF to 0.068µF are satisfactory.

4.4.4 REFERENCE CAPACITOR (C_{REF})

A 1µF capacitor is suggested. Low leakage capacitors, such as polypropylene, are recommended.

Several capacitor/resistor combinations for common full scale input conditions are given in Table 4-2.

TABLE 4-2: SUGGESTED COMPONENT VALUES

Comp.	2V Full Scale $V_{REF} \approx 1V$	2mV Full Scale $V_{REF} \approx 100V$	20mV Full Scale $V_{REF} \approx 10V$
R_{INT}	2MΩ	200kΩ	20kΩ
C_{INT}	0.033µF	0.033µF	0.033µF
C_{REF}	1µF	1µF	1µF
C_{AZ}	0.068µF	0.068µF	1.14µF
R_{OSC}	430kΩ	430kΩ	430kΩ

Note: Approximately 5 conversions/second.

4.5 Differential Signal Inputs

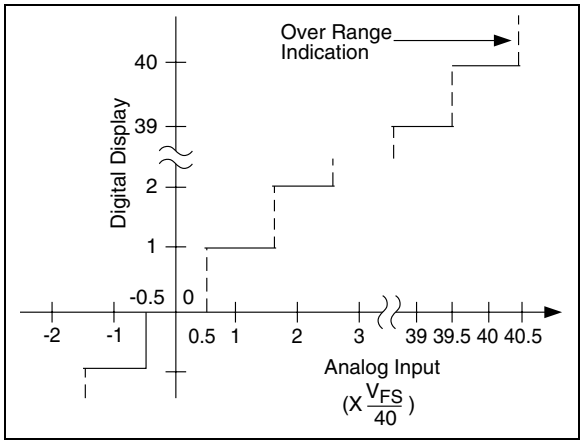
The TC826 is designed with true differential inputs and accepts input signals within the input stage Common mode voltage range (V_{CM}). The typical range is V+ -1 to V- +1V. Common mode voltages are removed from the system when the TC826 operates from a battery or floating power source (isolated from measured system) and -IN is connected to analog common (V_{COM}).

In systems where Common mode rejection ratio minimizes error. Common mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM}. For such applications, the integrator output swing can be reduced below the recommended 2V full scale swing. The integrator output will swing within 0.3V of V_{DD} or V_{SS} without increased linearity error.

4.6 Digital Section

The TC826 contains all the segment drivers necessary to drive a liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 256. A 430kΩ OSC gets the backplane frequency to approximately 55Hz, with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal, the segment is 'OFF'. An out-of-phase segment drive signal causes the segment to be 'ON' or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment drive, -POL, is 'ON' for negative analog inputs. If +IN and -IN are reversed, this indicator would reverse. The TC826 transfer function is shown in Figure 4-4.

FIGURE 4-4: TRANSFER FUNCTION



4.7 BAR/$\overline{\text{DOT}}$ Input (Pin 61)

The BAR/$\overline{\text{DOT}}$ input allows the user to select the display format. The TC826 powers up in the BAR mode. Select the DOT display format by connecting BAR/$\overline{\text{DOT}}$ to the negative supply (Pin 12) through a 1MΩ resistor.

4.8 $\overline{\text{HOLD}}$ Input (Pin 62)

The TC826 data output latches are not updated at the end of each conversion if $\overline{\text{HOLD}}$ is tied to the negative supply (Pin 12) through a 1MΩ resistor. The LCD display continuously displays the previous conversion results.

The $\overline{\text{HOLD}}$ pin is normally pulled high by an internal pull-up.

4.9 $\overline{\text{TEST}}$ Input (Pin 63)

The TC826 enters a Test mode with the $\overline{\text{TEST}}$ input connected to the negative supply (Pin 12). The connection must be made through a 1MΩ resistor. The $\overline{\text{TEST}}$ input is normally internally pulled high. A low input sets the output data latch to all ones. The BAR Display mode is set. The 41 LCD output segments (zero plus 40 data segments) and over range annunciator flash on and off at 1/4 the conversion rate. The polarity annunciator (POL-) segment will be on, but not flashing.

4.10 Over Range Display Operation (OR, Pin 59)

An out-of-range input signal will be indicated on the LCD display by the OR annunciator driver (Pin 59) becoming active.

In the BAR display format, the 41 bar segments and the over range annunciator, OR, will flash ON and OFF. The flash rate is on fourth the conversion rate (F_{OSC}/2560).

In the DOT Display mode, OR flashes and all other data segment drivers are off.

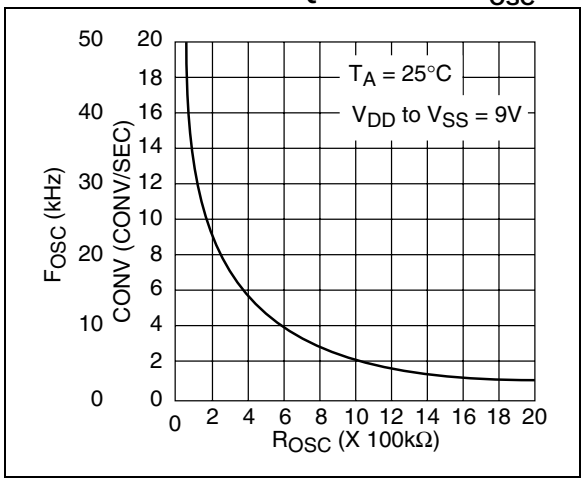
4.11 Polarity Indication (POL-, Pin 60)

The TC826 converts and displays data for positive and negative input signals. The POL LCD segment driver (Pin 60) is active for negative signals.

4.12 Oscillator Operation

The TC826 external oscillator frequency, F_{OSC}, is set by resistor R_{OSC} connected between pins 13 and 14. The oscillator frequency versus resistance curve is shown in Figure 4-5.

FIGURE 4-5: OSCILLATOR FREQUENCY VS. R_{OSC}

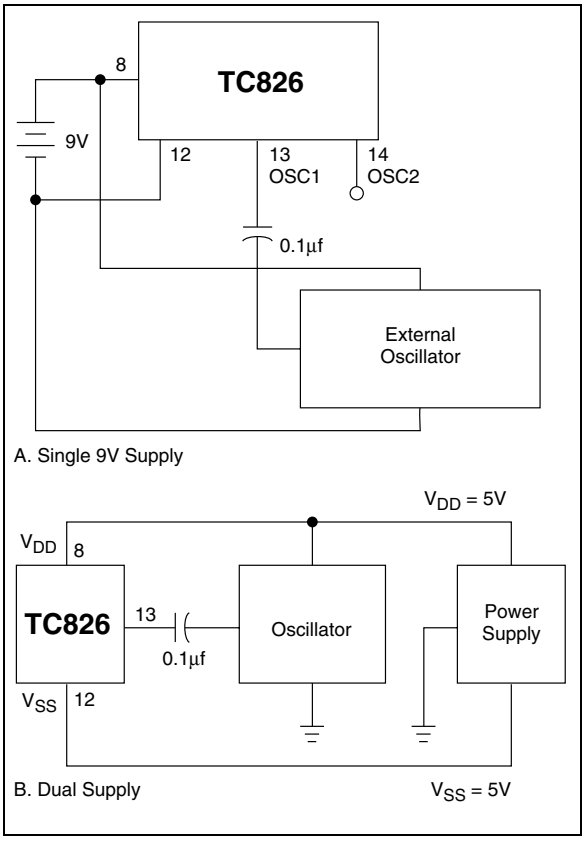


F_{OSC} is divided by 32 to provide an internal system clock, FYSY. Each conversion requires 80 internal clock cycles. The internal system clock is divided by 8 to provide the LCD backplane drive frequency. The display flash rate during an input out-of-range signal is set by dividing FSYS by 320.

The internal oscillator may be bypassed by driving OSC1 (Pin 13) with an external signal generator. OSC2 (Pin 14) should be left unconnected.

The oscillator should swing from V_{DD} to V_{SS} in single supply operation (Figure 4-6). In dual supply operation, the signal should swing from power supply ground to V_{DD}.

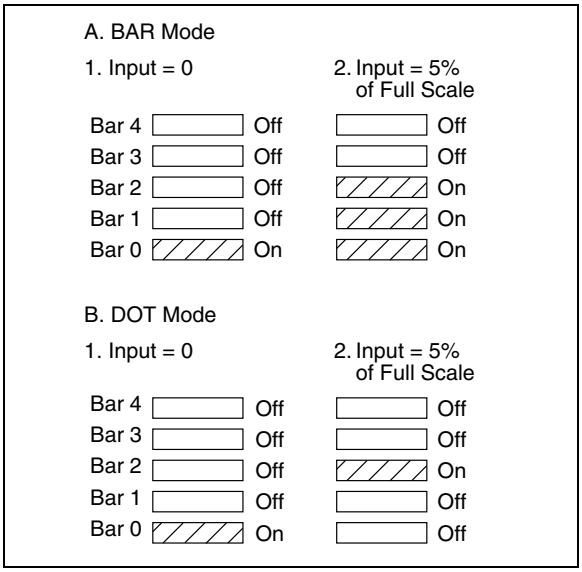
FIGURE 4-6: EXTERNAL OSCILLATOR CONNECTION



4.13 LCD Display Format

The input signal can be displayed in two formats (Figure 4-7). The BAR/DOT input (Pin 61) selects the format. The TC826 measurement cycle operates identically for either mode.

FIGURE 4-7: DISPLAY OPTION FORMATS



4.14 BAR Format

The TC826 powers up in the BAR mode. BAR/$\overline{DOT}$ is pulled high internally. This display format is similar to a thermometer display. All bars/LCD segments including zero, below the bar/LCD segment equaling the input signal level, are on. A half scale input signal, for example, would be displayed with BAR 0 to BAR 20 on.

4.15 $\overline{DOT}$ Format

By connecting BAR/$\overline{DOT}$ to V_{SS} through a 1MΩ resistor, the DOT mode is selected. Only the BAR LCD segment equaling the input signal is on. The zero segment is on for zero input.

This mode is useful for moving cursor or 'needle' applications.

4.16 LCD Displays

Most end products will use a custom LCD display for final production. Custom LCD displays are low cost and available from all manufacturers. The TC826 interfaces to non-multiplexed LCD displays. A backplane driver is included on-chip.

To speed initial evaluation and prototype work, a standard TC826 LCD display is available from Varitronix.

Varitronix Ltd. LCDs
4/F Liven House
61-63 King Yip Street
Kwun Tong, Kowloon
Hong Kong
Tel: (852)2389-4317
Fax: (852)2343-9555

USA Office:
VL Electronics / Varitronix
3250 Wilshire Blvd., Suite 901
Los Angeles, CA 90010
Tel: (213) 738-8700
Fax: (213) 738-5340

- Part No.: VBG-413-DP

Other standard LCD displays suitable for development work are available in both linear and circular formats. One manufacturer is:

UCE Inc.
24 Fitch Street
Norwalk, CT 06855
Tel: 203/838-7509

- Part No. 5040: 50 segment circular display with 3-digit numeric scale.
- Part No. 5020: 50 segment linear display.

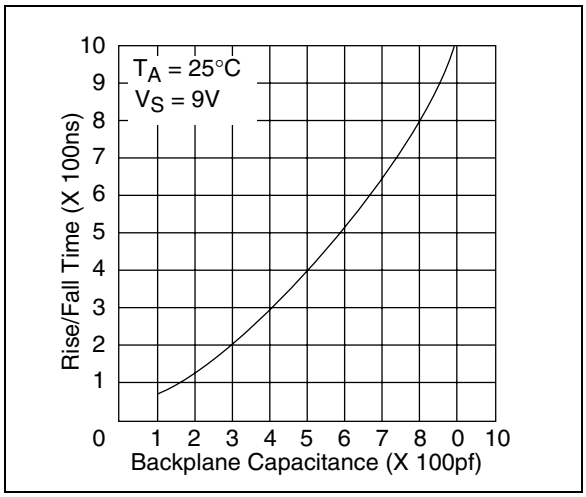
4.17 LCD Backplane Driver (BP, Pin 15)

Additional drive electronics are not required to interface the TC826 to an LCD display. The TC826 has an on-chip backplane generator and driver. The backplane frequency is:

$$FBP = F_{OSC}/256$$

Figure 4-8 gives typical backplane driver rise/fall time versus backplane capacitance.

FIGURE 4-8: BACKPLANE DRIVE RISE/FALL TIME VS. CAPACITANCE



4.18 Flat Package Socket

Sockets suitable for prototype work are available. A USA source is:

Nepenthe Distribution
2471 East Bayshore, Suite 520
Palo Alto, CA 94303
Tel: 415/856-9332
Telex: 910/373-2060

- 'BQ' Socket Part No.: IC51-064-042 BQ

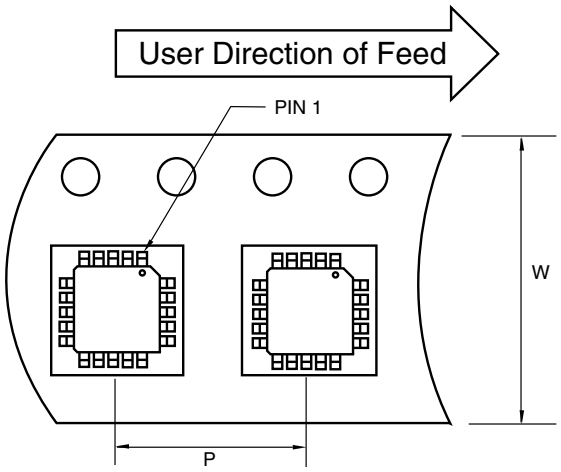
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package marking data not available at this time.

5.2 Taping Form

Component Taping Orientation for 64-Pin PQFP Devices



Standard Reel Component Orientation
for TR Suffix Device

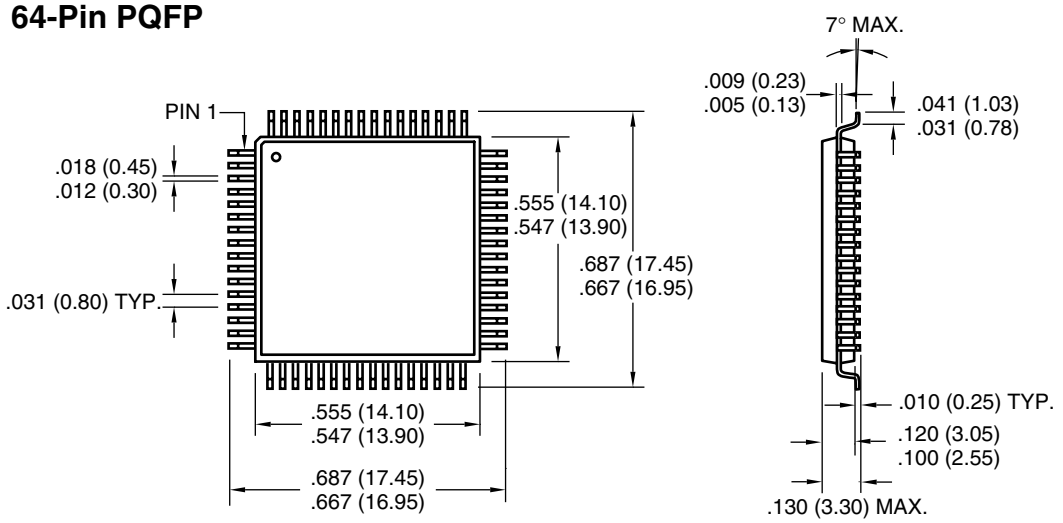
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
64-Pin PQFP	32 mm	24 mm	250	13 in

Note: Drawing does not represent total number of pins.

5.3 Package Dimensions

64-Pin PQFP



Dimensions: mm (inches)

NOTES:

SALES AND SUPPORT

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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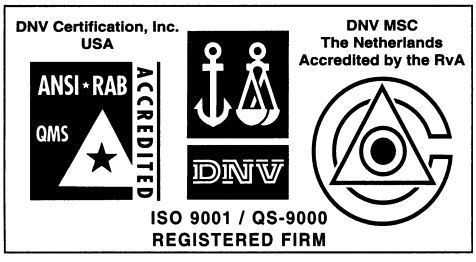

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