Supertex inc.



Dual N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV _{DSS} /	R _{DS(ON)}	V _{GS(th)}	I _{D(ON)}	Order Number/Package
BV _{DGS}	(max)	(max) (min)	(min)	SO-8
240V	6.0Ω	2.0V	1.0A	TD9944TG

Features

- Dual N-channel devices
- □ Low threshold 2.0V max.
- High input impedance
- □ Low input capacitance 125pF max.
- Fast switching speeds
- Low on resistance
- □ Free from secondary breakdown
- Low input and output leakage

Applications

- □ Logic level interfaces ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These dual low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's wellproven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

D, S 1 8 7 2 D, G, 6 З S2 D_2 4 5 G_{2} D, SO-8 top view Note: See Package Outline section for dimensions.

12/13/01

Supertex Inc. does not recommend the use of its products in life support applications and will not knowingly sell its products for use in such applications unless it receives an adequate "products liability indemnification insurance agreement." Supertex does not assume responsibility for use of devices described and limits its liability to the replacement of devices determined to be defective due to workmanship. No responsibility is assumed for possible omissions or inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications, refer to the Supertex website: http://www.supertex.com. For complete liability information on all Supertex products, refer to the most current databook or to the Legal/Disclaimer page on the Supertex website.

Pin Configuration

Electrical Characteristics (each device, @ 25°C unless otherwise specified)

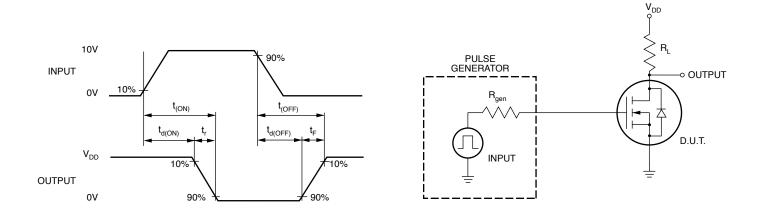
Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
BV_{DSS}	Drain-to-Source Breakdown Voltage	240			V	$V_{GS} = 0V, I_D = 2mA$	
V _{GS(th)}	Gate Threshold Voltage	0.6		2.0	V	$V_{GS} = V_{DS}, I_{D} = 1mA$	
$\Delta V_{GS(th)}$	Change in $V_{\text{GS}(\text{th})}$ with Temperature			-5.0	mV/°C	$V_{GS} = V_{DS}, I_{D} = 1mA$	
I _{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I _{DSS}	Zero Gate Voltage Drain Current			10	μΑ	V_{GS} = 0V, V_{DS} = Max Rating	
				1.0	mA	$V_{GS} = 0V, V_{DS} = 0.8$ Max Rating $T_A = 125^{\circ}C$	
I _{D(ON)}	ON-State Drain Current	0.5	1.9		A	$V_{GS} = 4.5V, V_{DS} = 25V$	
		1.0	2.8			$V_{GS} = 10V, V_{DS} = 25V$	
R _{DS(ON)}	Static Drain-to-Source		4.0	6.0	Ω	$V_{GS} = 4.5V, I_{D} = 250mA$	
	ON-State Resistance		4.0	6.0		$V_{GS} = 10V, I_{D} = 0.5A$	
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.4	%/°C	$V_{GS} = 10V, I_{D} = 0.5A$	
G _{FS}	Forward Transconductance	300	600		mΩ	$V_{DS} = 25V, I_{D} = 0.5A$	
C _{ISS}	Input Capacitance		65	125		$V_{GS} = 0V, V_{DS} = 25V$ f = 1 MHz	
C _{OSS}	Common Source Output Capacitance		35	70	pF		
C _{RSS}	Reverse Transfer Capacitance		10	25			
t _{d(ON)}	Turn-ON Delay Time			10			
t _r	Rise Time			10	ns	$V_{DD} = 25V,$ $I_D = 1.0A,$ $R_{GEN} = 25\Omega$	
t _{d(OFF)}	Turn-OFF Delay Time			20	115		
t _f	Fall Time			20			
V_{SD}	Diode Forward Voltage Drop			1.8	V	$V_{GS} = 0V, I_{SD} = 1.0A$	
t _{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = 1.0A$	

Notes:

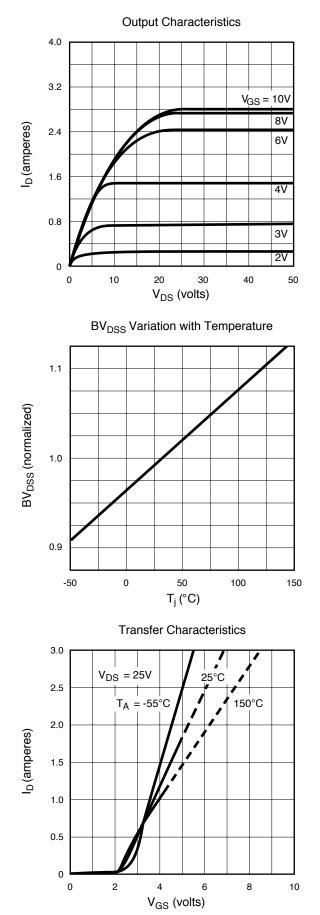
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

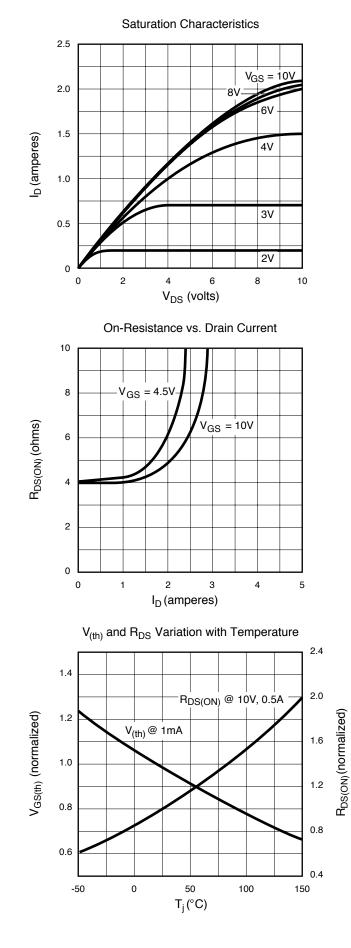
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Typical Performance Curves

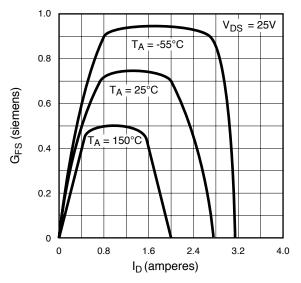


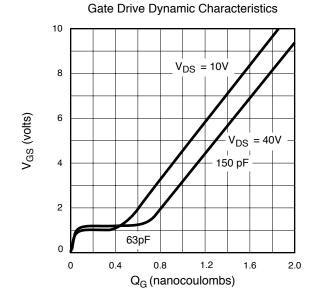


Typical Performance Curves

Capacitance vs. Drain-to-Source Voltage 200 f = 1MHz 150 C (picofarads) 100 CISS 50 Coss C_{RSS} 0 0 10 20 30 40 V_{DS} (volts)

Transconductance vs. Drain Current





12/13/010



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