



**Dual N-Channel Enhancement-Mode Vertical DMOS FETs**

**Ordering Information**

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	V <sub>GS(th)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number/Package
				SO-8
240V	6.0Ω	2.0V	1.0A	TD9944TG

**Features**

- Dual N-channel devices
- Low threshold — 2.0V max.
- High input impedance
- Low input capacitance — 125pF max.
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage

**Low Threshold DMOS Technology**

These dual low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

**Applications**

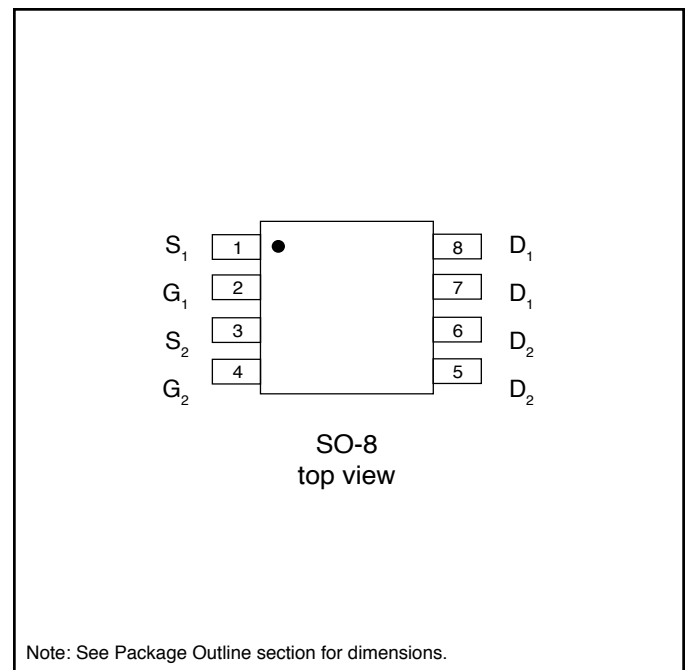
- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

**Absolute Maximum Ratings**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\* Distance of 1.6 mm from case for 10 seconds.

**Pin Configuration**



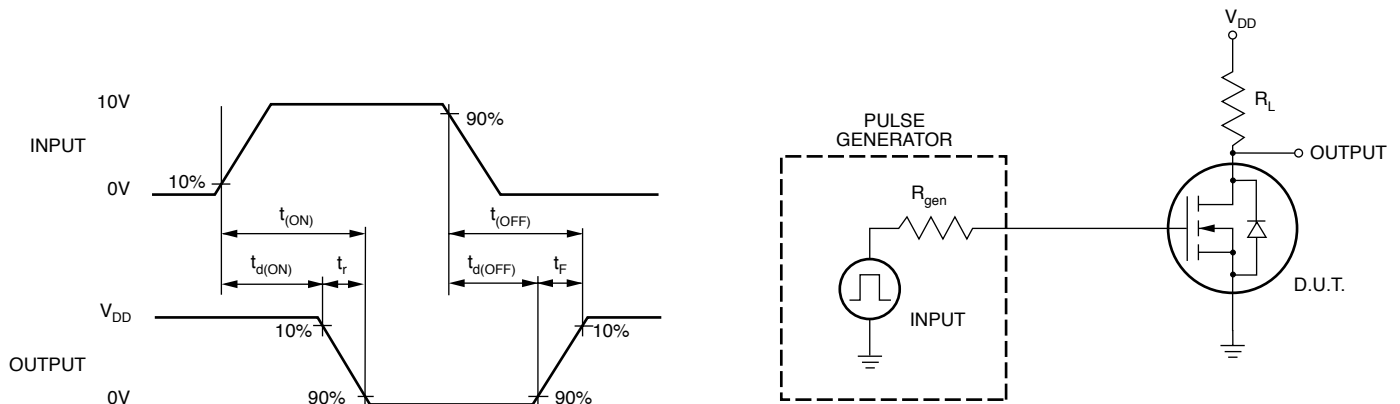
## Electrical Characteristics (each device, @ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	240			V	$V_{GS} = 0V, I_D = 2mA$
$V_{GS(th)}$	Gate Threshold Voltage	0.6		2.0	V	$V_{GS} = V_{DS}, I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.0	mV/°C	$V_{GS} = V_{DS}, I_D = 1mA$
$I_{GSS}$	Gate Body Leakage			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate Voltage Drain Current			10	$\mu A$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				1.0	mA	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ C$
$I_{D(ON)}$	ON-State Drain Current	0.5	1.9		A	$V_{GS} = 4.5V, V_{DS} = 25V$
		1.0	2.8			$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		4.0	6.0	$\Omega$	$V_{GS} = 4.5V, I_D = 250mA$
			4.0	6.0		$V_{GS} = 10V, I_D = 0.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.4	%/°C	$V_{GS} = 10V, I_D = 0.5A$
$G_{FS}$	Forward Transconductance	300	600		mS	$V_{DS} = 25V, I_D = 0.5A$
$C_{ISS}$	Input Capacitance		65	125	pF	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance		35	70		
$C_{RSS}$	Reverse Transfer Capacitance		10	25		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = 25V,$ $I_D = 1.0A,$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			10		
$t_{d(OFF)}$	Turn-OFF Delay Time			20		
$t_f$	Fall Time			20		
$V_{SD}$	Diode Forward Voltage Drop			1.8	V	$V_{GS} = 0V, I_{SD} = 1.0A$
$t_{rr}$	Reverse Recovery Time		300		ns	$V_{GS} = 0V, I_{SD} = 1.0A$

### Notes:

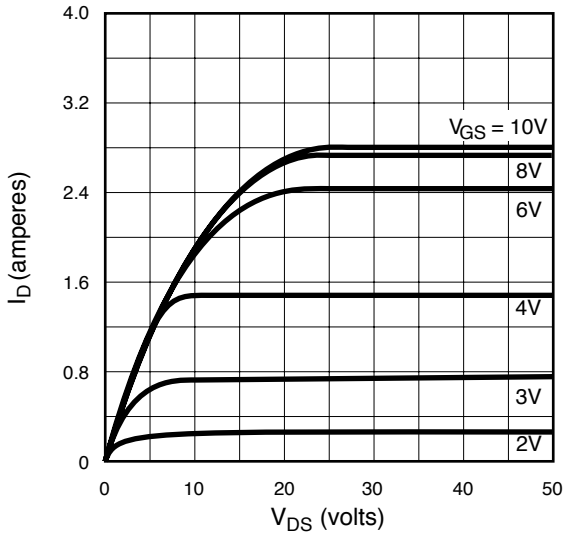
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 $\mu$ s pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

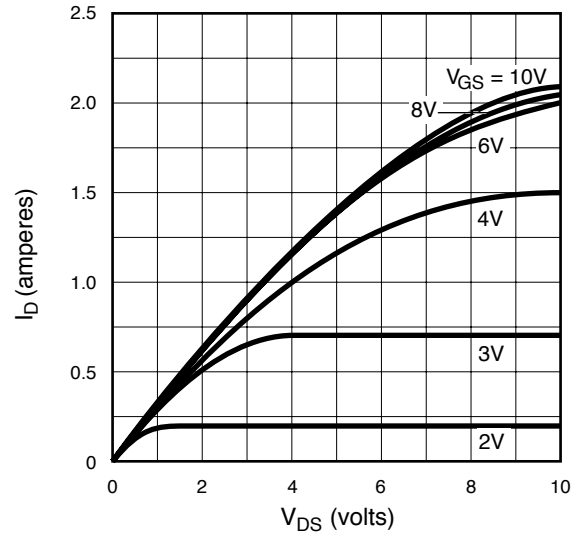


# Typical Performance Curves

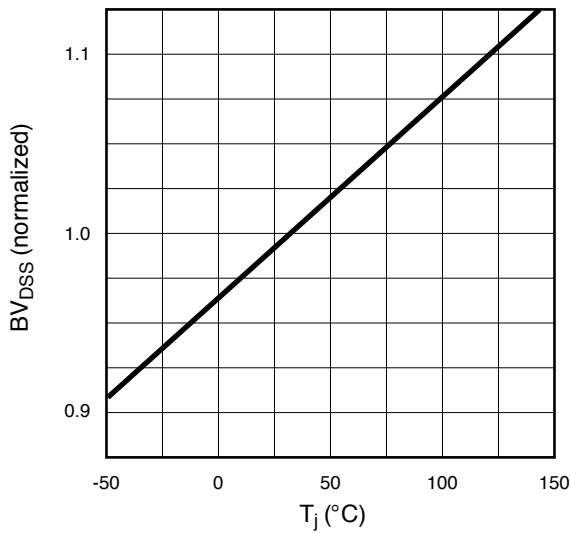
Output Characteristics



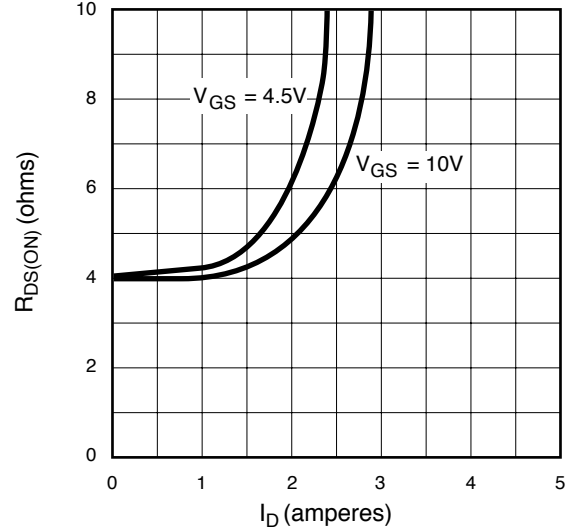
Saturation Characteristics



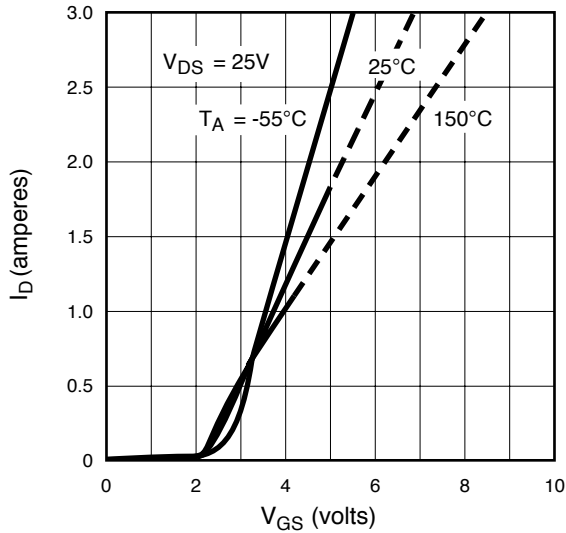
$BV_{DSS}$  Variation with Temperature



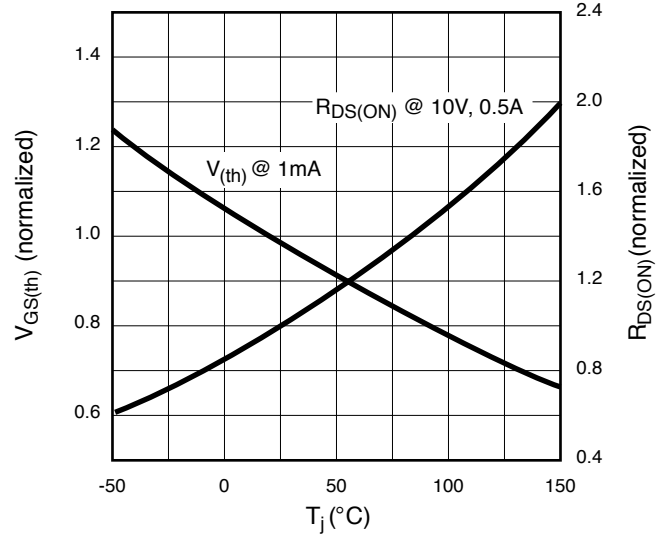
On-Resistance vs. Drain Current



Transfer Characteristics

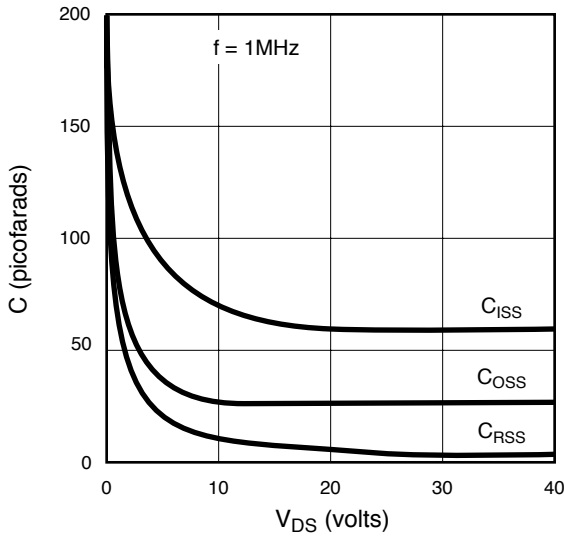


$V_{GS(th)}$  and  $R_{DS}$  Variation with Temperature

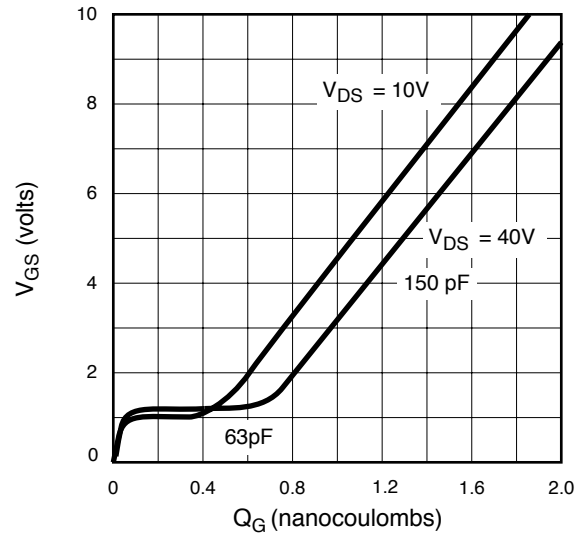


# Typical Performance Curves

Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



Transconductance vs. Drain Current

