DATA SHEET

TDA1306T
Noise shaping filter DAC

Product specification
Supersedes data of September 1994
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

Noise shaping filter DAC TDA1306T

FEATURES

General

- Double-speed mode
- Digital volume control
- Soft mute function
- 12 dB attenuation
- Low power dissipation
- Digital de-emphasis
- TDA1305T pin compatible.

Easy application

- Voltage output
- Only 1st-order analog post-filtering required
- Operational amplifiers and digital filter integrated
- Selectable system clock (f_{sys}) $256f_s$ or $384f_s$
- I^2S-bus ($f_{sys} = 256f_s$) or 16, 18 or 20 bits LSB fixed serial input format ($f_{sys} = 384f_s$)
- Single rail supply.

High performance

- Superior signal-to-noise ratio
- Wide dynamic range
- No zero crossing distortion
- Inherently monotonic
- Continuous calibration digital-to-analog conversion combined with noise shaping technique.

GENERAL DESCRIPTION

The TDA1306T is a dual CMOS digital-to-analog converter with up-sampling filter and noise shaper. The combination of oversampling up to $4f_s$, noise shaping and continuous calibration conversion ensures that only simple 1st-order analog post-filtering is required.

The TDA1306T supports the I^2S-bus data input mode ($f_{sys} = 256f_s$) with word lengths of up to 20 bits and the LSB fixed serial data input format ($f_{sys} = 384f_s$) with word lengths of 16, 18 or 20 bits. Two cascaded IIR filters increase the sampling rate 4 times.

The DACs are of the continuous calibration type and incorporate a special data coding. This ensures a high signal-to-noise ratio, wide dynamic range and immunity to process variation and component ageing.

Two on-board operational amplifiers convert the digital-to-analog current to an output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1306T	SO24	plastic small outline package; 24 leads; body width 7.5 mm.	SOT137–1

QUICK REFERENCE DATA

All power supply pins V_{DD} and V_{SS} must be connected to the same external supply unit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	5	8	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	3	5	mA
I_{DDO}	operational amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	2	4	mA
Analog signals						
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V; R_L > 5 kΩ	0.935	1.1	1.265	V
R_L	output load resistance		5	–	–	kΩ
DAC performance						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; f_i = 1 kHz;	–	–70	–	dB
			–	0.032	–	%
		at –60 dB signal level; f_i = 1 kHz;	–	–42	–32	dB
			–	0.8	2.5	%
S/N	signal-to-noise ratio	no signal; A-weighted	–	–108	–96	dB
BR	input bit rate at data input	f_s = 44.1 kHz; normal speed	–	–	2.822	Mbits/s
		f_s = 44.1 kHz; double speed	–	–	5.645	Mbits/s
f_{sys}	system clock frequency (pin 12)		6.4	–	18.432	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

BLOCK DIAGRAM

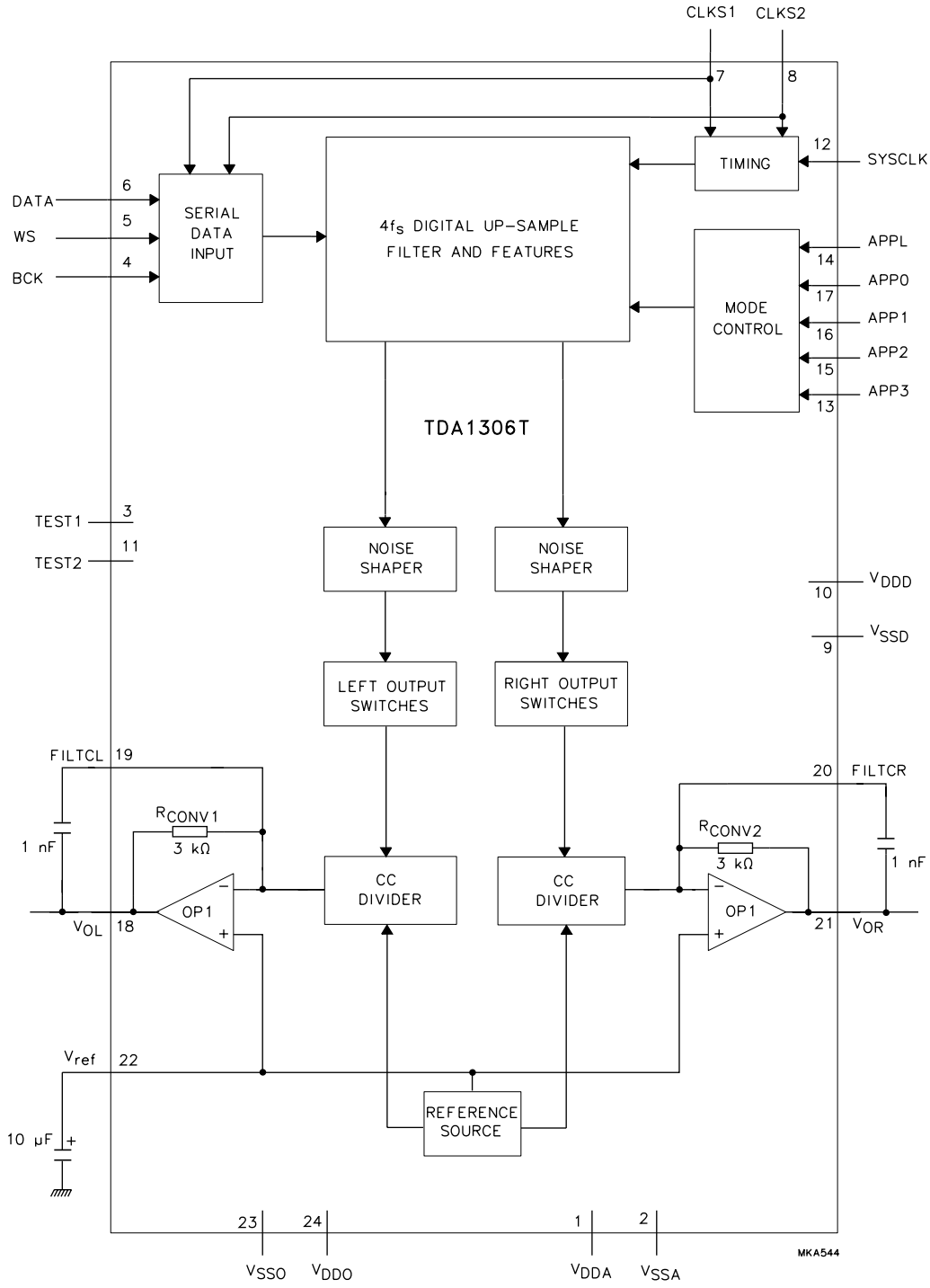


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	analog supply voltage (+5 V)
V_{SSA}	2	analog ground
TEST1	3	test input 1; pin should be connected to ground
BCK	4	bit clock input
WS	5	word select input
DATA	6	data input
CLKS1	7	clock and format selection 1 input
CLKS2	8	clock and format selection 2 input
V_{SSD}	9	digital ground
V_{DDD}	10	digital supply voltage (+5 V)
TEST2	11	test input 2; pin should be connected to ground
SYSCLK	12	system clock input $256f_s$ or $384f_s$
APP3	13	application mode 3 input
APPL	14	application mode selection input
APP2	15	application mode 2 input
APP1	16	application mode 1 input
APP0	17	application mode 0 input
V_{OL}	18	left channel output
FILTCL	19	capacitor for left channel 1st order filter function; should be connected between pins 19 and 18
FILTCR	20	capacitor for right channel 1st order filter function; should be connected between pins 20 and 21
V_{OR}	21	right channel output
V_{ref}	22	internal reference voltage for output channels; $0.5V_{DDO}$ (typ.)
V_{SSO}	23	operational amplifier ground
V_{DDO}	24	operational amplifier supply voltage

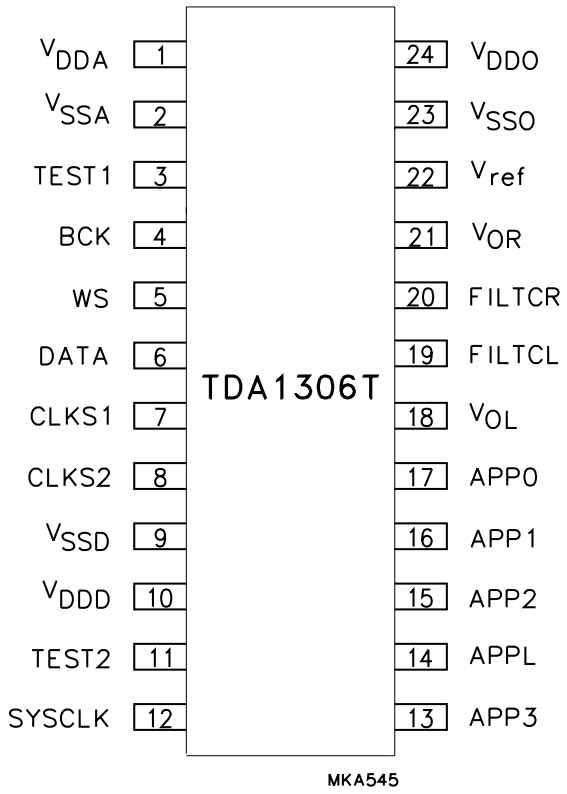


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1306T CMOS DAC incorporates an up-sampling filter, a noise shaper, continuous calibrated current sources and operational amplifiers.

System clock and data input format

The TDA1306T accommodates slave mode only. Consequently, in all applications, the system devices must provide the system clock. The system frequency is selectable at pins CLKS1 and CLKS2 (see Table 1).

The TDA1306T supports the following data input modes:

- I^2S-bus with data word length of up to 20 bits ($f_{sys} = 256f_s$)
- LSB fixed serial format with data word length of 16, 18 or 20 bits ($f_{sys} = 384f_s$). As this format idles on the MSB it is necessary to know how many bits are being transmitted.

The input formats are illustrated in Fig.9. Left and right data channel words are time multiplexed.

Table 1 Data input format and system clock

CLKS1	CLKS2	DATA INPUT FORMAT	SYSTEM CLOCK	
			NORMAL SPEED	DOUBLE SPEED
0	0	I^2S-bus	$256f_s$	$128f_s$
0	1	LSB fixed 16 bits	$384f_s$	$192f_s$
1	0	LSB fixed 18 bits	$384f_s$	$192f_s$
1	1	LSB fixed 20 bits	$384f_s$	$192f_s$

Device operation

When the APPL pin is held HIGH and APP3 is held LOW, pins APP0, APP1 and APP2 form a microcontroller interface. When the APPL pin is held LOW, pins APP0, APP1, APP2 and APP3 form a pseudo-static application (TDA1305T pin compatible).

PSEUDO-STATIC APPLICATION MODE (APPL = LOGIC 0)

In this mode, the device operation is controlled by pseudo-static application pins where:

APP0 = attenuation mode control

APP1 = double-speed mode control

APP2 = mute mode control

APP3 = de-emphasis mode control.

In the pseudo-static application mode the TDA1306T is pin compatible with the TDA1305T slave mode.
The correspondence between TDA1306T pin number, TDA1306T pin name, TDA1305T pin mnemonic and a description of the effects is given in Table 2.

Table 2 Pseudo-static application mode

PIN MNEMONIC	PIN NUMBER	TDA1305T FUNCTION	VALUE	DESCRIPTION
APP0	17	ATSB	0	12 dB attenuation (from full scale) activated (only if MUSB = logic 1)
			1	full scale (only if MUSB = logic 1)
APP1	16	DSMB	0	double-speed mode
			1	normal-speed mode
APP2	15	MUSB	0	samples decrease to mute level
			1	level according to ATSB
APP3	13	DEEM1	0	de-emphasis OFF (44.1 kHz)
			1	de-emphasis ON (44.1 kHz)

MICROCONTROLLER APPLICATION MODE (APPL = LOGIC 1 AND APP3 = LOGIC 0)

In this mode, the device operation is controlled by a set of flags in an 8-bit mode control register. The 8-bit mode control register is written by a microcontroller interface where:

APPL = logic 1

APP0 = Data

APP1 = Clock

APP2 = RAB

APP3 = logic 0.

The correspondence between serial-to-parallel conversion, mode control flags and a summary of the effect of the control flags is given in Table 3. Figures 3 and 4 illustrate the mode set timing.

MICROCONTROLLER WRITE OPERATION SEQUENCE

The microcontroller write operation follows the following sequence:

- APP2 is held LOW by the microcontroller
- Microcontroller data is clocked into the internal shift register on the LOW-to-HIGH transition on pin APP1
- Data D7 to D0 is latched into the appropriate control register on the LOW-to-HIGH transition of pin APP2 (APP1 = HIGH)
- If more data is clocked into the TDA1306T before the LOW-to-HIGH transition on pin APP2 then only the last 8 bits are used
- If less data is clocked into the TDA1306T unpredictable operation will result
- If the LOW-to-HIGH transition of pin APP2 occurs when APP1 = LOW, the command will be disregarded.

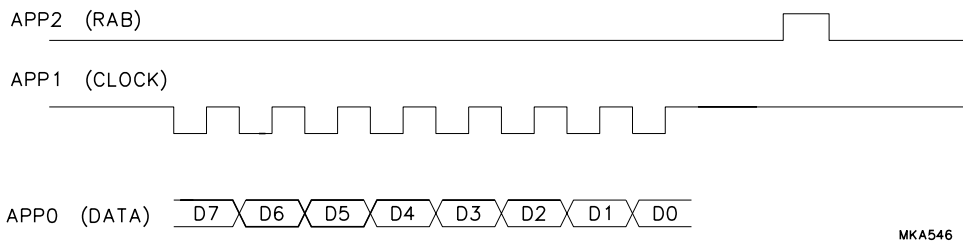


Fig.3 Microcontroller timing.

MICROCONTROLLER WRITE OPERATION SEQUENCE (REPEAT MODE)

The same command can be repeated several times (e.g. for fade function) by applying APP2 pulses as shown in Fig.4. It should be noted that APP1 must stay HIGH between APP2 pulses. A minimum pause of 22 μs is necessary between any two step-up or step-down commands.

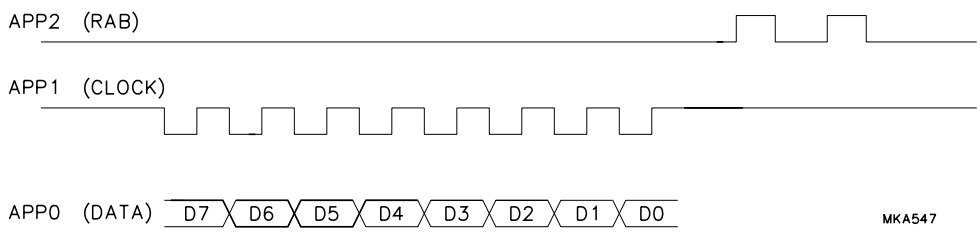


Fig.4 Microcontroller timing (repeat mode).

Table 3 Microcontroller mode control register

BIT POSITION	FUNCTION	DESCRIPTION	ACTIVE LEVEL
D7	ATSB	12 dB attenuation (from full scale)	LOW
D6	DSMB	double speed	LOW
D5	MUSB	mute	LOW
D4	DEEM	de-emphasis	HIGH
D3	FS	full scale	HIGH
D2	INCR	increment	HIGH
D1	DECR	decrement	HIGH
D0	not applicable	reserved	not applicable

Volume control

A digital level control is incorporated in the TDA1306T which performs the function of soft mute and attenuation (pseudo-static application mode) or soft mute, attenuation, fade, increment and decrement (microcontroller application mode). The volume control of both channels can be varied in small step changes determined by the value of the internal fade counter where:

Audio level = counter × maximum level/120.

Where the counter is a 7-bit binary number between 0 and 120. The time taken for mute to vary from 120 to 0 is $1/120f_s$. For example, when f_s = 44.1 kHz, the time taken is approximately 3 ms.

VOLUME CONTROL (PSEUDO-STATIC APPLICATION MODE)

In the pseudo-static application mode (APPL = logic 0) the digital audio output level is controlled by APP0 (attenuation) and APP2 (mute) so only the final volume levels full scale, 12 dB (attenuate) and mute (–infinity dB) can be selected. The mute function has priority over the attenuation function. Accordingly, if MUSB is LOW, the state of ATSB has no effect. An example of volume control in this application mode is illustrated in Fig.5.

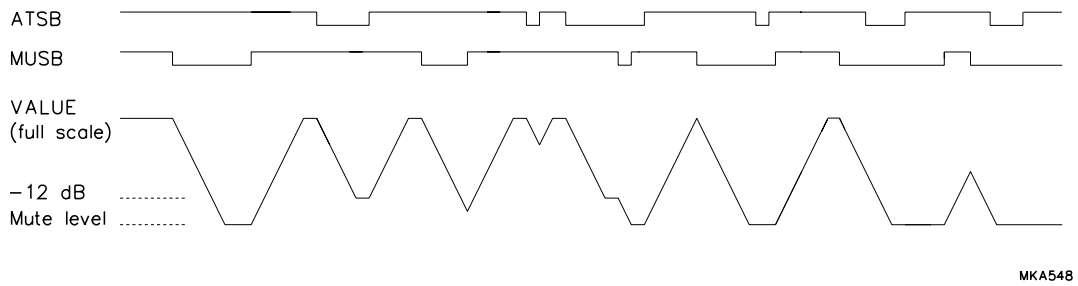


Fig.5 Volume control (pseudo-static application mode).

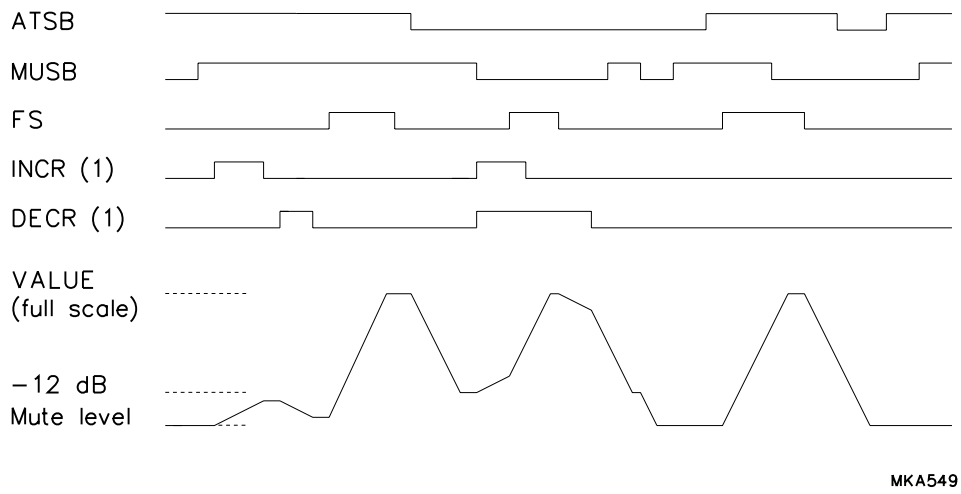
VOLUME CONTROL (MICROCONTROLLER APPLICATION MODE)

In the microcontroller application mode (APPL = logic 1, APP3 = logic 0) the audio output level is controlled by volume control bits ATSB, MUSB, FS, INCR and DECR.

Mute is activated by sending the MUSB command to the mode control register via the microcontroller interface. The audio output level will be reduced to zero in a maximum of 120 steps (depending on the current position of the fade counter) and taking a maximum of 3 ms. Mute, attenuation and full scale are synchronized to prevent operation in the middle of a word.

- The counter is preset to 120 by the full scale command
- The counter is preset to 30 by the attenuate command when its value is more then 30. If the value of the counter is less than 30 dB the ATSB command has no effect.
- The counter is preset to logic 0 by the mute command MUSB
- Attenuation (–12 dB) is activated by sending the ATSB command to the fade control register (D7)
- Attenuation and mute are cancelled by sending the full-scale command to the fade control register (Register D3).

To control the fade counter in a continuous way, the INCREMENT and DECREMENT commands are available (fade control Registers D1 and D2). They will increment and decrement the counter by 1 for each register write operation. When issuing more than 1 step-up or step-down command in sequence, the write repeat mode may be used (see microcontroller application mode). An example of volume control in this application mode is illustrated in Fig.6.



(1) INCR and DECR in repeat mode.

Fig.6 Volume control (microcontroller application mode).

There are two recommended application situations within the microcontroller mode:

- The customer wants to use the microcontroller interface without the volume setting facility. In this event the operation is as follows:
  - Mute ON; by sending the MUSB command
  - Mute OFF; by sending the FS command
  - Attenuation ON; by sending the ATSB command
  - Attenuation OFF; by sending the FS command.

  It is possible to switch from 'Attenuation ON' to 'Mute ON' but not vice-versa.
- Incorporating the volume control feature operates as follows:
  - Mute ON; by sending the MUSB command the microcontroller has to store the previous volume setting
  - Mute OFF; by sending succeeding INCR commands until the previous volume is reached
  - Attenuation ON; by sending succeeding DECR commands until a relative downstep of −12 dB is reached.
    The microcontroller has to store the previous volume
  - Attenuation OFF; by sending the succeeding INCR commands until the previous volume is reached
  - Volume UP; by sending succeeding INCR commands
  - Volume DOWN; by sending succeeding DECR commands.

De-emphasis

A digital de-emphasis is implemented in the TDA1306T. By selecting the DEEM bit at register D4 (microcontroller application mode) or activating the APP3 pin (pseudo-static application mode), de-emphasis can be applied by means of an IIR filter. De-emphasis is synchronized to prevent operation in the middle of a word.

Double-speed mode

The double-speed mode is controlled by the DSMB bit at register D6 (microcontroller application mode) or by activating the APP1 pin (pseudo-static application mode). When the control bit is active LOW the device operates in the double-speed mode.

Oversampling filter and noise shaper

The digital filter is a four times oversampling filter.
It consists of two sections which each increase the sample rate by 2. The noise-shaper operates on $4f_s$ and reduces the in-band noise density.

DAC and operational amplifiers

In this noise shaping filter DAC a special data code and bidirectional current sources are used in order to achieve true low-noise performance. The special data code guarantees that only small values of current flow to the output during small signal passages while larger positive or negative values are generated using the bidirectional current sources. The noise shaping filter-DAC uses the continuous calibration conversion technique.

The operational amplifiers and the internal conversion resistors R_{CONV1} and R_{CONV2} convert the DAC current to an output voltage available at V_{OL} and V_{OR}. Connecting an external capacitor between FILTCL and V_{OL}, FILTCR and V_{OR} respectively provides the required 1st-order post filtering.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	7.0	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 2	–2000	+2000	V
		note 3	–200	+200	V

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 mH series inductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	69	K/W

QUALITY SPECIFICATION

In accordance with *“UZW-BO/FQ-0601”.*

DC CHARACTERISTICS

V_{DDD} = V_{DDA} = V_{DDO} = 5 V; T_{amb} = 25 °C; all voltages referenced to ground (pins 2, 9 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage (pin 10)	note 1	4.5	5.0	5.5	V
V_{DDA}	analog supply voltage (pin 1)	note 1	4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage (pin 24)	note 1	4.5	5.0	5.5	V
I_{DDD}	digital supply current	f_{sys} = 11.28 MHz	–	5	8	mA
I_{DDA}	analog supply current	at digital silence	–	3	6	mA
I_{DDO}	operational amplifier supply current	no operational amplifier load resistor	–	2	4	mA
P_{tot}	total power dissipation	f_{sys} = 11.28 MHz; digital silence; no operational amplifier load resistor	–	50	90	mW
V_{IH}	HIGH level digital input voltage (pins 3 to 8 and 11 to 17)		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
V_{IL}	LOW level digital input voltage (pins 3 to 8 and 11 to 17)		–0.5	–	$+0.3V_{DDD}$	V
R_{pd}	internal pull-down resistor to V_{SSD} (pins 3 and 11)		17	–	134	kΩ
$\|I_{LI}\|$	input leakage current		–	–	10	μA
C_i	input capacitance		–	–	10	pF
V_{ref}	reference voltage (pin 22)	with respect to V_{SSO}	$0.45V_{DDO}$	$0.5V_{DDO}$	$0.55V_{DDO}$	V
R_{CONV}	current-to-voltage conversion resistor		2.4	3.0	3.6	kΩ
$V_{FS(rms)}$	full-scale output voltage (RMS value)	R_L > 5 kΩ; note 2	0.935	1.1	1.265	V
R_L	output load resistance		5	–	–	kΩ

Notes

1. All power supply pins (V_{DD} and V_{SS}) must be connected to the same external power supply unit.
2. R_L is the AC resistance of the external circuitry connected to the audio outputs of the application circuit.

AC CHARACTERISTICS (ANALOG)

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 2, 9 and 23); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DACs						
SVRR	supply voltage ripple rejection V_{DDA} and V_{DDO}	f_{ripple} = 1 kHz; V_{ripple} = 100 mV (p-p); C22 = 10 μF	–	40	–	dB
ΔG_v	unbalance between the 2 DAC voltage outputs (pins 18 and 21)	maximum volume	–	–	0.5	dB
α_{ct}	crosstalk between the 2 DAC voltage outputs (pins 18 and 21)	one output digital silence the other maximum volume	–	–110	–85	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; f_i = 1 kHz	–	–70	–	dB
			–	0.032	–	%
		at –60 dB signal level; f_i = 1 kHz	–	–42	–32	dB
			–	0.8	2.5	%
S/N	signal-to-noise ratio	no signal; A-weighted	–	–108	–96	dB
Operational amplifiers						
G_v	open-loop voltage gain		–	85	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 3 kHz; V_{ripple} = 100 mV (p-p); A-weighted	–	90	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	$R_L > 5$ kΩ; f_i = 1 kHz; V_o = 2.8 V (p-p)	–	–100	–	dB
f_{UG}	unity gain frequency	open loop	–	4.5	–	MHz
$\|Z_o\|$	AC output impedance	$R_L > 5$ kΩ	–	1.5	150	Ω

AC CHARACTERISTICS (DIGITAL)

V_{DDD} = V_{DDA} = V_{DDO} 4.5 to 5.5 V; all voltages referenced to ground (pins 2, 9 and 23); T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{WX}	clock cycle time	f_{sys} = 384f_s; normal speed	54.2	59.1	104	ns
		f_{sys} = 192f_s; double speed	54.2	59.1	104	ns
		f_{sys} = 256f_s; normal speed	81.3	88.6	156	ns
		f_{sys} = 128f_s; double speed	81.3	88.6	156	ns
t_{CWL}	f_{sys} LOW level pulse width		22	–	–	ns
t_{CWH}	f_{sys} HIGH level pulse width		22	–	–	ns
Serial input data timing (see Fig.8)						
f_s	word select input audio sample frequency	normal speed	25	44.1	48	kHz
		double speed	50	88.2	96	kHz
f_{BCK}	clock input frequency (data input rate)	f_{sys} = 384f_s; normal speed; note 1	–	–	64f_s	kHz
		f_{sys} = 192f_s; double speed; note 1	–	–	64f_s	kHz
		f_{sys} = 256f_s; normal speed	–	–	64f_s	kHz
		f_{sys} = 128f_s; double speed; note 2	–	–	48f_s	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
t_H	bit clock HIGH time		55	–	–	ns
t_L	bit clock LOW time		55	–	–	ns
t_{su}	data set-up time		20	–	–	ns
t_h	data hold time		10	–	–	ns
t_{suWS}	word select set-up time		20	–	–	ns
t_{hWS}	word select hold time		10	–	–	ns
Microcontroller interface timing (see Fig.9)						
t_L	input LOW time		2	–	–	µs
t_H	Input HIGH time		2	–	–	µs
t_{suDC}	set-up time DATA to CLOCK		1	–	–	µs
t_{hCD}	hold time CLOCK to DATA		1	–	–	µs
t_{suCR}	set-up time CLOCK to RAB		1	–	–	µs

Notes

1. A clock frequency of up to 96f_s is possible in the event of a rising edge of BCK occurring during SYSCLK = LOW.
2. A clock frequency of up to 64f_s is possible in the event of a rising edge of BCK occurring during SYSCLK = LOW.

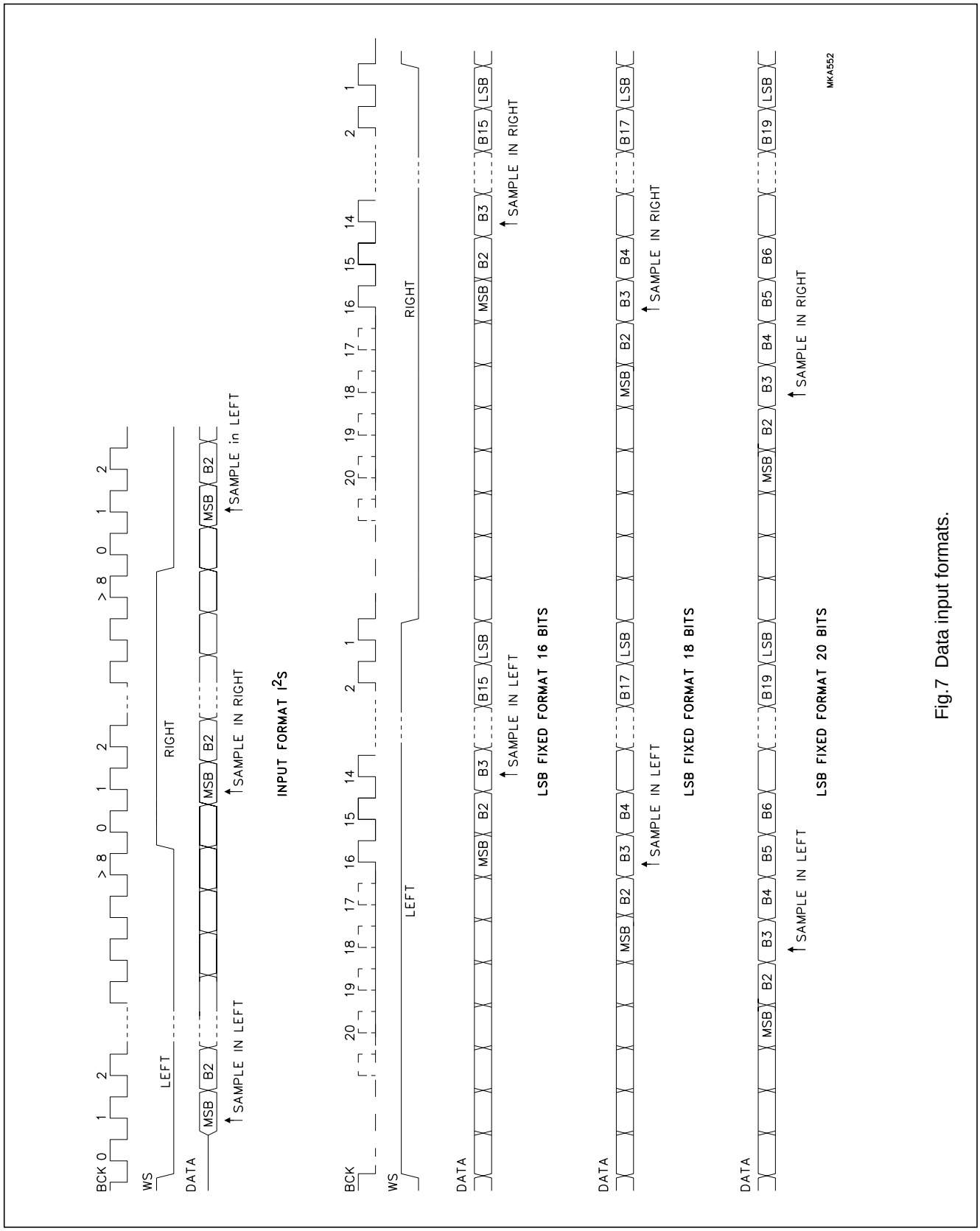


Fig.7 Data input formats.

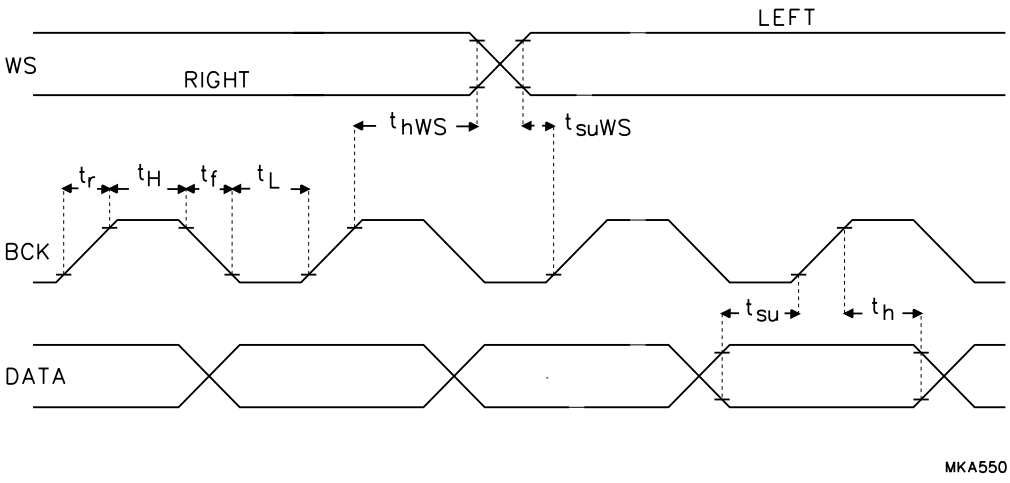


Fig.8 Timing of input signals.

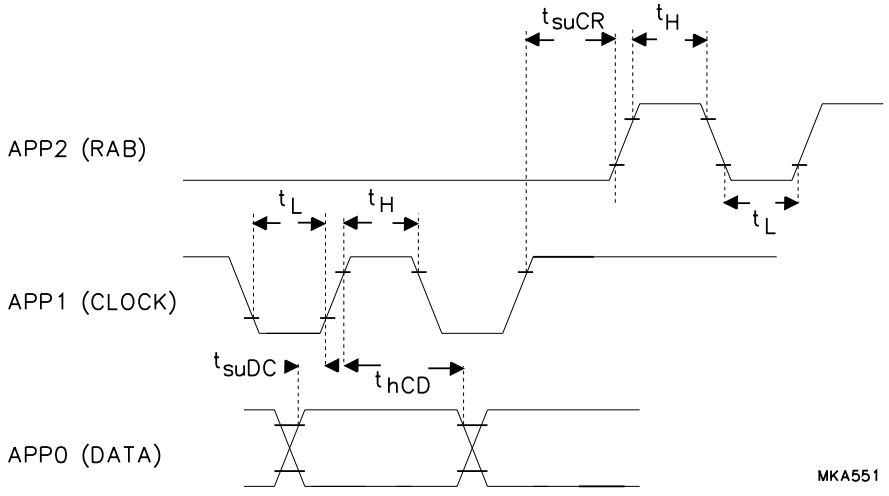


Fig.9 Microcontroller timing.

TEST AND APPLICATION INFORMATION

Filter characteristics

Table 4 Digital filter specification (f_s = 44.1 kHz)

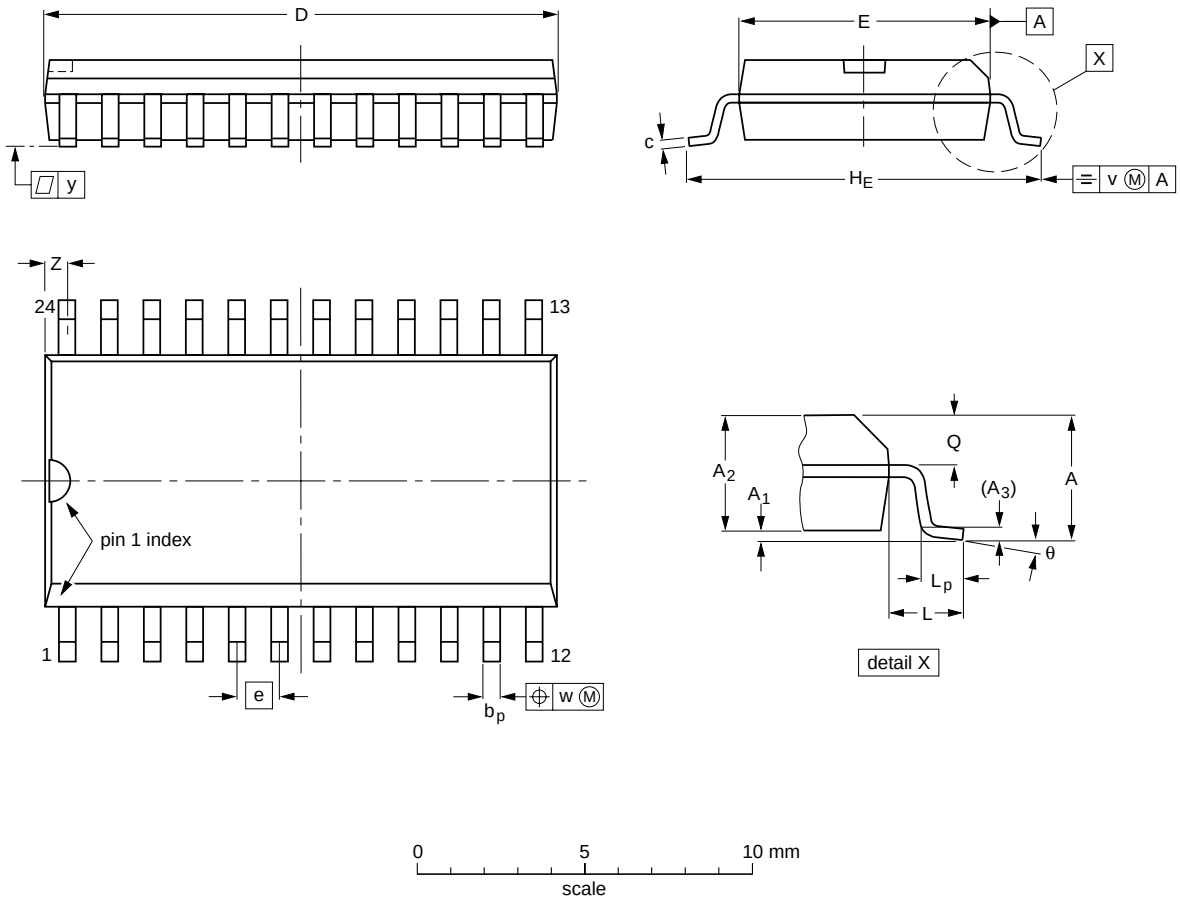
BAND	ATTENUATION
0 to 19 kHz	< 0.001 dB
19 to 20 kHz	< 0.03 dB
24 kHz	> 25 dB
25 to 35 kHz	> 40 dB
35 to 64 kHz	> 50 dB
64 to 68 kHz	> 31 dB
68 kHz	> 35 dB
69 to 88 kHz	> 40 dB

Table 5 Digital filter phase distortion (f_s = 44.1 kHz)

BAND	PHASE DISTORTION
0 to 16 kHz	< ±1°

PACKAGE OUTLINE

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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