DATA SHEET

TDA1564
High efficiency 2 × 25 W/4 Ω stereo car radio power amplifier

Preliminary specification
Supersedes data of 2003 Sep 17

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Philips
Semiconductors

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High efficiency 2 × 25 W/4 Ω stereo car radio power amplifier

TDA1564

FEATURES

- Low dissipation due to switching from Single-Ended (SE) to Bridge-Tied Load (BTL) mode
- Differential inputs with high Common Mode Rejection Ratio (CMRR)
- Mute/standby/operating (mode select pin)
- Load dump protection circuit
- Short-circuit safe to ground, to supply voltage and across load
- Loudspeaker protection circuit
- Offset detection for each channel
- Device switches to single-ended operation at excessive junction temperatures
- Thermal protection at high junction temperature (170°C)
- Clip detection at THD = 2.5 %
- Diagnostic information (clip/protection/prewarning/offset).

GENERAL DESCRIPTION

The TDA1564 is a monolithic power amplifier in a 17-lead single-in-line (SIL) plastic power package. It contains two identical 25 W amplifiers. The dissipation is minimized by switching from SE to BTL mode, only when a higher output voltage swing is needed. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	DC biased	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
$\lvert Z_i \rvert$	input impedance		90	120	150	kΩ
P_o	output power	R_L = 4 Ω; EIAJ	–	38	–	W
		R_L = 4 Ω; THD = 10 %	23	25	–	W
		R_L = 4 Ω; THD = 2.5 %	18	20	–	W
G_v	voltage gain	P_o = 1 W	25	26	27	dB
CMRR	common mode rejection ratio	f = 1 kHz; R_S = 0 Ω	–	80	–	dB
SVRR	supply voltage ripple rejection	f = 1 kHz; R_S = 0 Ω	45	65	–	dB
$\lvert \Delta V_O \rvert$	DC output offset voltage		–	–	100	mV
α_{cs}	channel separation	R_S = 0 Ω; P_o = 15 W	40	70	–	dB
$\lvert \Delta G_v \rvert$	channel unbalance		–	–	1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1564TH	HSOP20	plastic, heatsink small outline package; 20 leads; low stand-off height	SOT418-3
TDA1564J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

BLOCK DIAGRAM

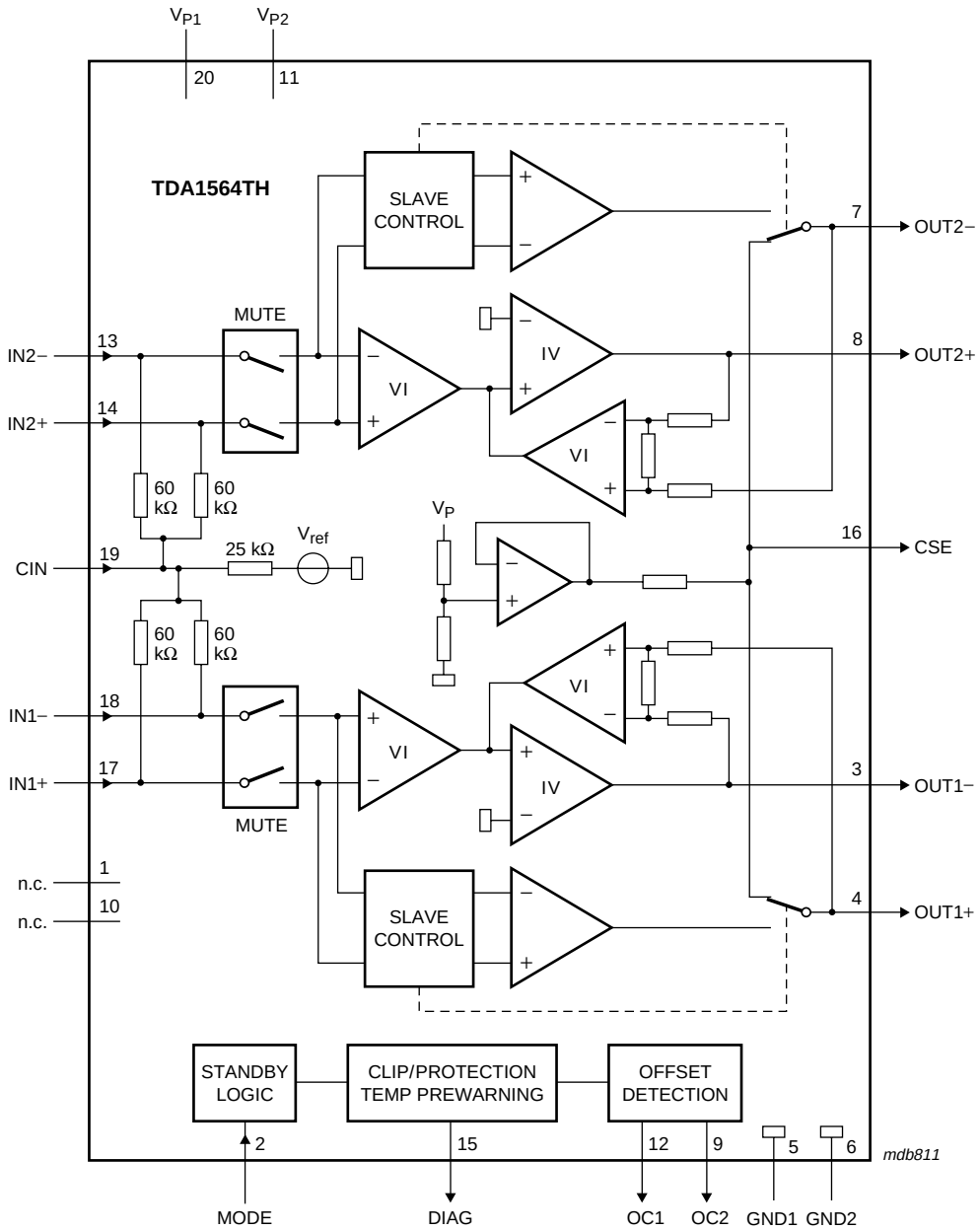


Fig.1 Block diagram (TDA1564TH).

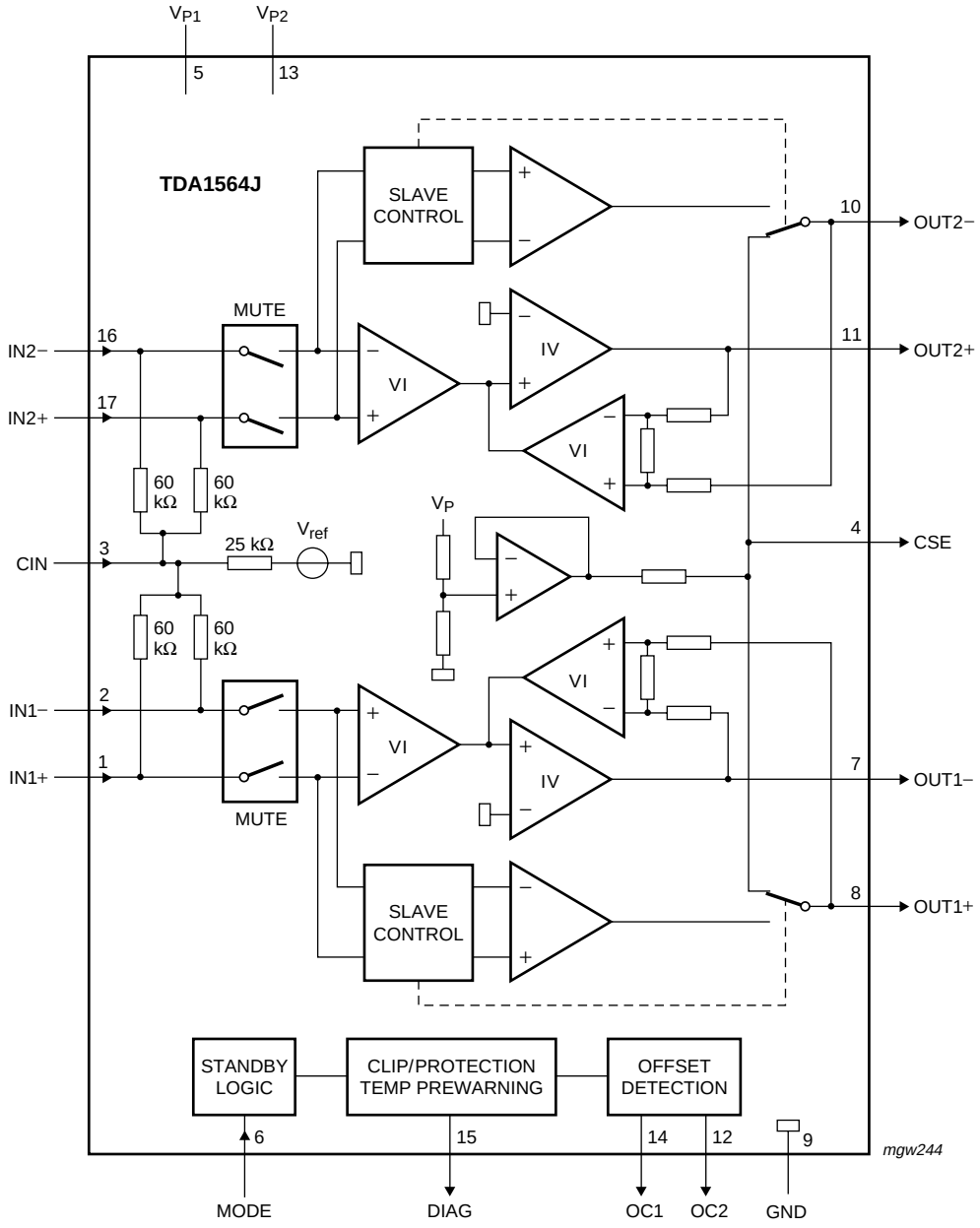


Fig.2 Block diagram (TDA1564J).

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA1564TH	TDA1564J	
n.c.	1	–	not connected
MODE	2	6	mute/standby/operating
OUT1–	3	7	inverting output 1
OUT1+	4	8	non-inverting output 1
GND1	5	–	ground 1
GND	–	9	ground
GND2	6	–	ground 2
OUT2–	7	10	inverting output 2
OUT2+	8	11	non-inverting output 2
OC2	9	12	offset capacitor 2
n.c.	10	–	not connected
V_{P2}	11	13	supply voltage 2
OC1	12	14	offset capacitor 1
IN2–	13	16	inverting input 2
IN2+	14	17	non-inverting input 2
DIAG	15	15	diagnostic
CSE	16	4	electrolytic capacitor for single-ended (SE) mode
IN1+	17	1	non-inverting input 1
IN1–	18	2	inverting input 1
CIN	19	3	common input
V_{P1}	20	5	supply voltage 1

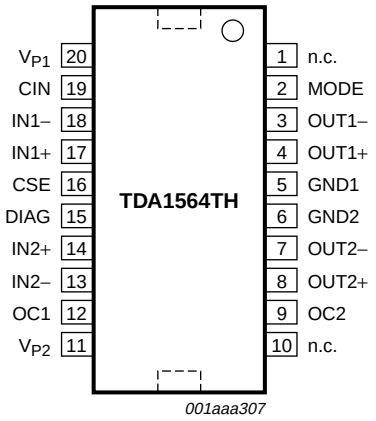


Fig.3 Pin configuration (TDA1564TH).

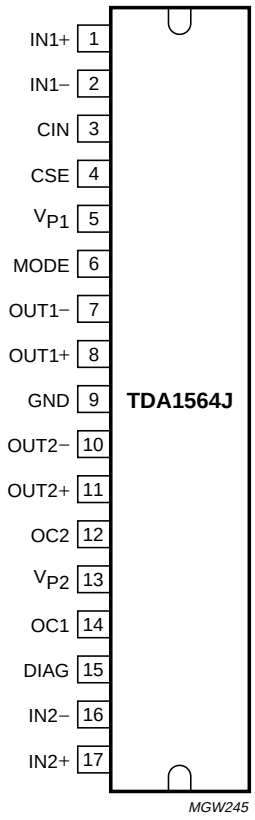


Fig.4 Pin configuration (TDA1564J).

FUNCTIONAL DESCRIPTION

The TDA1564 contains two identical amplifiers with differential inputs. At low output power [up to output amplitudes of 3 V (RMS) at V_P = 14.4 V], the device operates as a normal SE amplifier. When a larger output voltage swing is needed, the circuit switches internally to BTL operation.

With a sine wave input signal, the dissipation of a conventional BTL amplifier (up to 2 W output power) is more than twice the dissipation of the TDA1564 (see Fig.12).

In normal use, when the amplifier is driven with music-like signals, the high (BTL) output power is only needed for a small percentage of time. Assuming that a music signal has a normal (Gaussian) amplitude distribution, the dissipation of a conventional BTL amplifier with the same output power is approximately 70 % higher (see Figs 13 and 14.

The heatsink has to be designed for use with music signals. With such a heatsink, the thermal protection will disable the BTL mode when the junction temperature exceeds 150 °C. In this case, the output power is limited to 5 W per amplifier.

The gain of each amplifier is internally fixed at 26 dB. The device can be switched to the following modes via the MODE pin:

- Standby with low standby current (< 50 μA)
- Mute condition, DC adjusted
- On, operation.

The device is fully protected against a short-circuit of the output pins to ground and to the supply voltage. It is also protected against a short-circuit of the loudspeaker and against high junction temperatures. In the event of a permanent short-circuit condition to ground or the supply voltage, the output stage will be switched off, causing low dissipation. With a permanent short-circuit of the

loudspeaker, the output stage will be repeatedly switched on and off. The duty cycle in the 'on' condition is low enough to prevent excessive dissipation.

The device also has two independent DC offset detection circuits that can detect DC output voltages across the speakers. With a DC offset greater than 2 V, a warning is given on the diagnostic pin. There will be no internal shutdown with DC offsets.

When the supply voltage drops below 6 V (e.g. engine start), the circuit mutes immediately, avoiding clicks from the electronic circuit preceding the power amplifier.

The voltage of the SE electrolytic capacitor (pin 4) is kept at $0.5V_P$ by means of a voltage buffer (see Fig.2). The value of this capacitor has an important influence on the output power in SE mode, especially at low signal frequencies. A high value is recommended to minimize dissipation at low frequencies.

The diagnostic output is an open-collector output and requires a pull-up resistor. It gives the following outputs:

- Clip detection at THD = 2.5 %
- Short-circuit protection:
  - When a short-circuit occurs (for at least 10 ms) at the outputs to ground or the supply voltage, the output stages are switched off to prevent excessive dissipation; the outputs are switched on again approximately 500 ms after the short-circuit is removed, during this short-circuit condition the protection pin is LOW
  - When a short-circuit occurs across the load (for at least 10 ms), the output stages are switched off for approximately 500 ms; after this time, a check is made to see whether the short-circuit is still present
  - The power dissipation in any short-circuit condition is very low.
- During start-up/shutdown, when the product is internally muted
- Temperature prewarning:
  - A prewarning (junction temperature > 145 °C) indicates that the temperature protection will become active. The prewarning can be used to reduce the input signal and thus reduce the power dissipation.
- Offset detection:
  - One of the channels has a DC output voltage greater than 2 V.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	18	V
		non-operating	–	30	V
		load dump; t_r > 2.5 ms	–	45	V
$V_{P(sc)}$	short-circuit safe voltage		–	18	V
V_{rp}	reverse polarity voltage		–	6	V
I_{ORM}	repetitive peak output current		–	4	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	150	°C
T_{amb}	ambient temperature		–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	note 1	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

Note

1. The value of $R_{th(c-h)}$ depends on the application (see Fig.5).

Heatsink design

There are two parameters that determine the size of the heatsink. The first is the rating for the virtual junction temperature and the second is the ambient temperature at which the amplifier must still deliver its full power in the BTL mode.

With a conventional BTL amplifier, the maximum power dissipation with a music-like signal (at each amplifier) will be approximately two times 6.5 W. At a virtual junction temperature of 150 °C and a maximum ambient temperature of 65 °C, $R_{th(vj-c)}$ = 1.3 K/W and $R_{th(c-h)}$ = 0.2 K/W, the thermal resistance of the heatsink should be: $\frac{150-65}{2\times 6.5} - 1.3 - 0.2 = 5$ K/W

Compared to a conventional BTL amplifier, the TDA1564 has a higher efficiency. The thermal resistance of the heatsink should be:

$1.7\left(\frac{145-65}{2\times 6.5}\right) - 1.3 - 0.2 = 9$ K/W

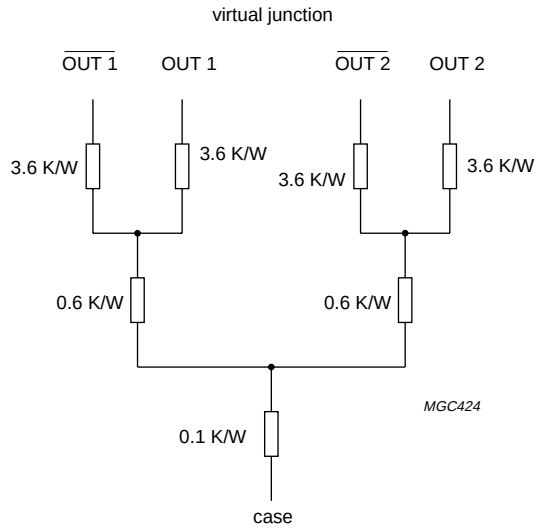


Fig.5 Thermal equivalent resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage	note 1; Fig.17	6.0	14.4	18.0	V
$I_{q(tot)}$	total quiescent current	$R_L = \infty$; Fig.16	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
V_{CSE}	average electrolytic capacitor voltage at pin 4		–	7.1	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage	on state	–	–	100	mV
		mute state	–	–	100	mV
Mode select switch; see Fig.6						
V_{MODE}	voltage at mode select pin	standby condition	0	–	1	V
		mute condition	2	–	3	V
		on condition	4	5	V_P	V
$I_{MODE(sw)}$	switch current through pin 6	V_{MODE} = 5 V	–	25	40	μA
Diagnostic						
V_{DIAG}	output voltage at the diagnostic output pin	I_{DIAG} = 2 mA; during any fault condition or clip detect	–	–	0.5	V
I_{DIAG}	current through the diagnostic pin	during any fault condition or clip detect	2	–	–	mA
$V_{O(DC)}$	DC output voltage detection levels		1.4	2	2.5	V
Protection						
T_{pre}	prewarning temperature		–	145	–	°C
$T_{dis(BTL)}$	BTL disable temperature	note 2	–	150	–	°C

Notes

1. The circuit is DC biased at V_P = 6 to 18 V and AC operating at V_P = 8 to 18 V.
2. If the junction temperature exceeds 150 °C, the output power is limited to 5 W per channel.

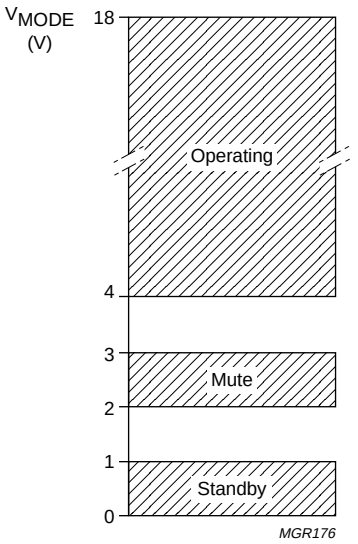


Fig.6 Switching levels of the mode select pin.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; C_{CSE} = 1000 μF; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5 %; Fig.18	15	19	–	W
		THD = 10 %; Fig.18	23	25	–	W
		EIAJ	–	38	–	W
		V_P = 13.2 V; THD = 0.5 %	–	16	–	W
		V_P = 13.2 V; THD = 10 %	–	20	–	W
THD	total harmonic distortion	P_o = 1 W; note 1; Fig.19	–	0.1	–	%
P	power dissipation		see Figs 12 and 13			W
B_p	power bandwidth	THD = 1 %; P_o = –1 dB with respect to 15 W	–	20 to 15000	–	Hz
$f_{ro(l)}$	low frequency roll-off	–1 dB; note 2	–	25	–	Hz
$f_{ro(h)}$	high frequency roll-off	–1 dB	130	–	–	kHz
G_v	closed-loop voltage gain	P_o = 1 W; Fig.21	25	26	27	dB
SVRR	supply voltage ripple rejection	R_S = 0 Ω; V_{ripple} = 2 V (p-p); Fig.22				
		on/mute	45	65	–	dB
		standby; f = 100 Hz to 10 kHz	45	–	–	dB
CMRR	common mode rejection ratio	R_S = 0 Ω	70	90	–	dB
$\lvert Z_i \rvert$	input impedance		90	120	150	kΩ
$\lvert \Delta Z_i \rvert$	mismatch in input impedance		–	1	–	%
V_{SE-BTL}	SE to BTL switch voltage level	note 3	–	3	–	V
$\lvert V_{out} \rvert$	output voltage mute (RMS value)	V_i = 1 V (RMS)	–	100	150	μV
$V_{n(o)}$	noise output voltage	on; R_S = 0 Ω; note 4	–	100	150	μV
		on; R_S = 10 kΩ; note 4	–	105	–	μV
		mute; note 5	–	100	150	μV
α_{cs}	channel separation	R_S = 0 Ω; P_o = 15 W; Fig.23	40	70	–	dB
$\lvert \Delta G_v \rvert$	channel unbalance		–	–	1	dB

Notes

1. The distortion is measured with a bandwidth of 10 Hz to 30 kHz.
2. Frequency response externally fixed (input capacitors determine the low frequency roll-off).
3. The SE to BTL switch voltage level depends on the value of V_P.
4. Noise output voltage measured with a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage is independent of R_S.

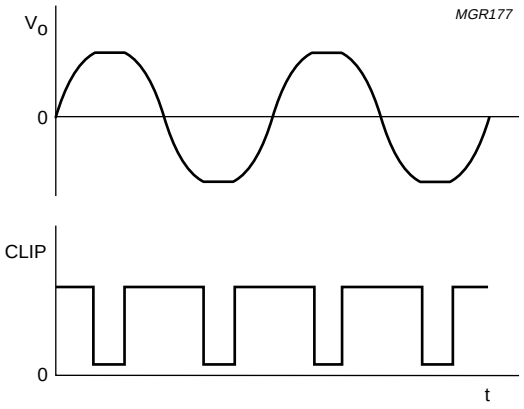


Fig.7 Clip detection waveforms.

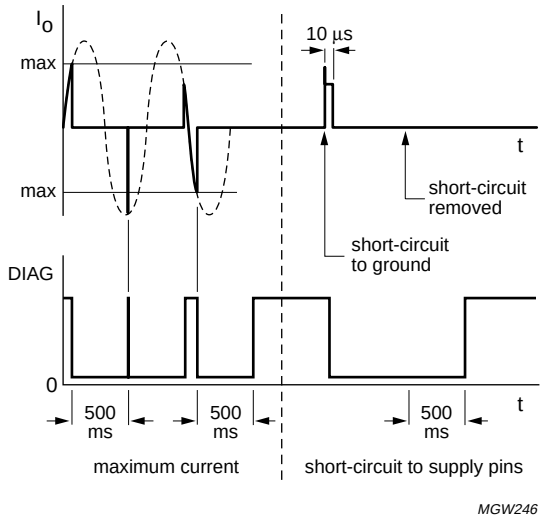
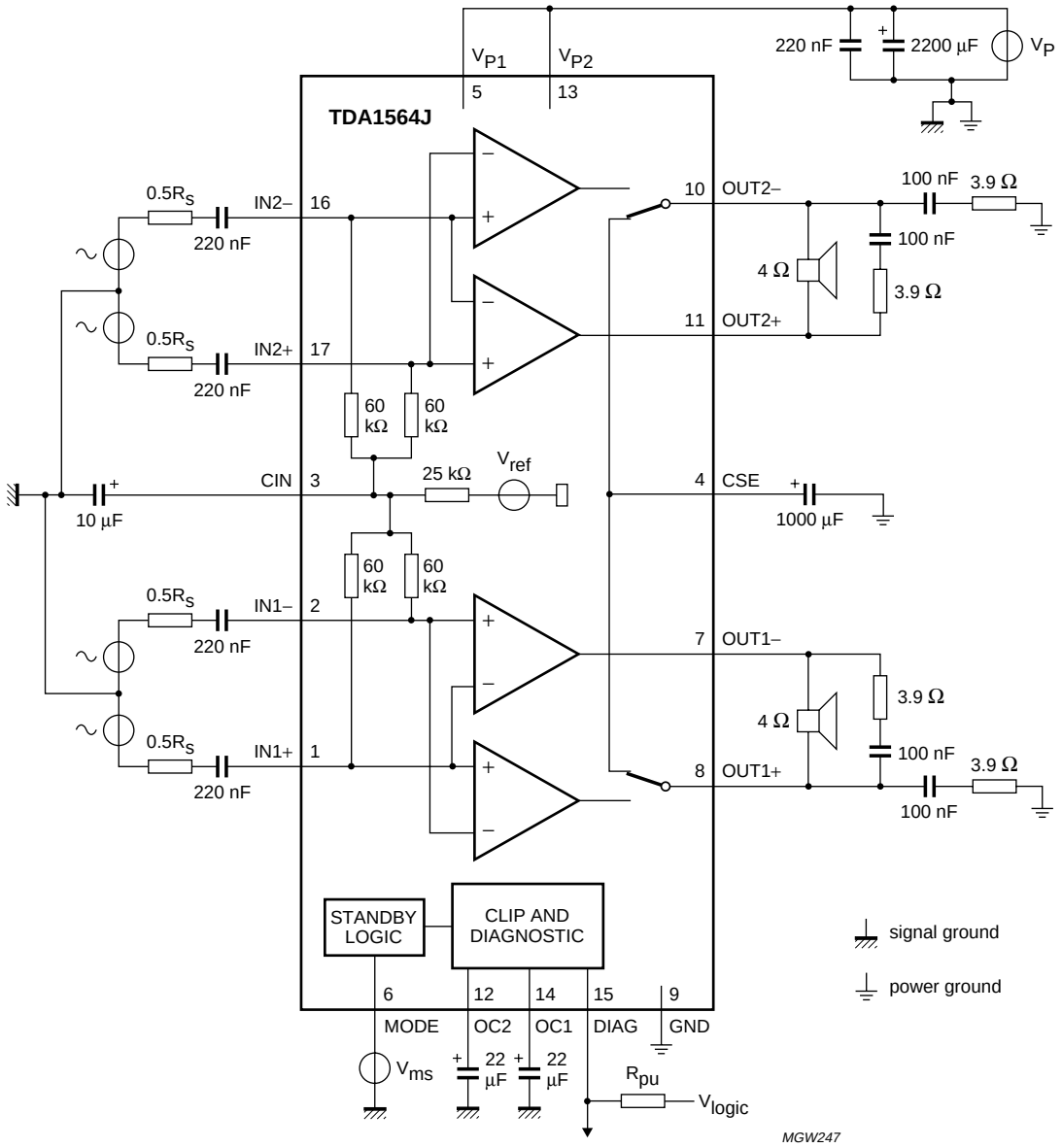


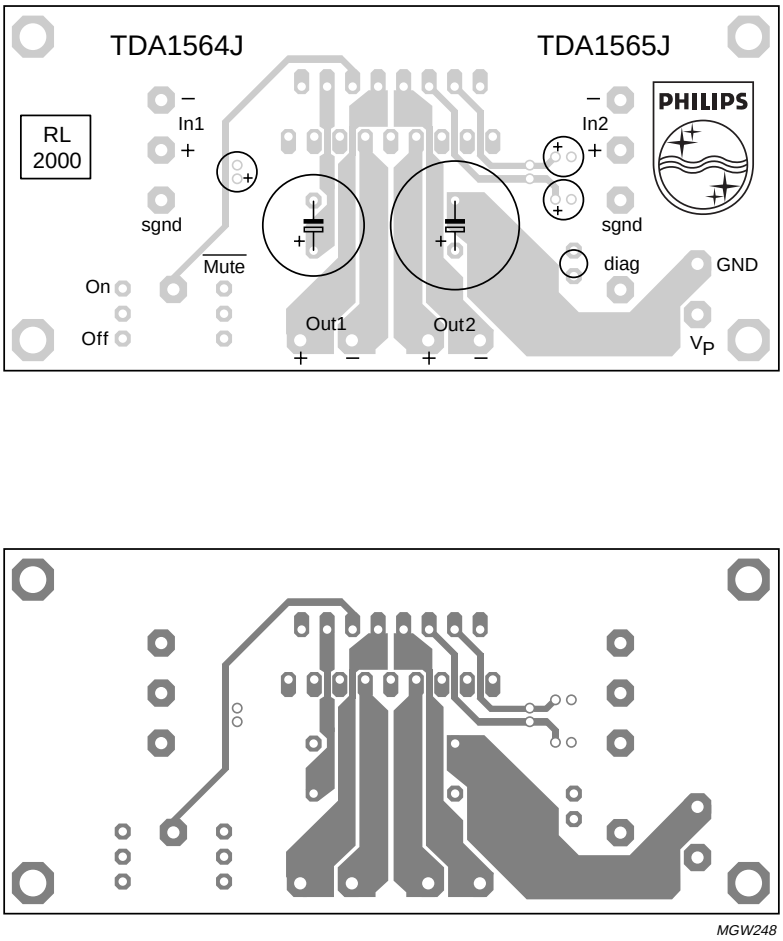
Fig.8 Protection waveforms.

TEST AND APPLICATION INFORMATION



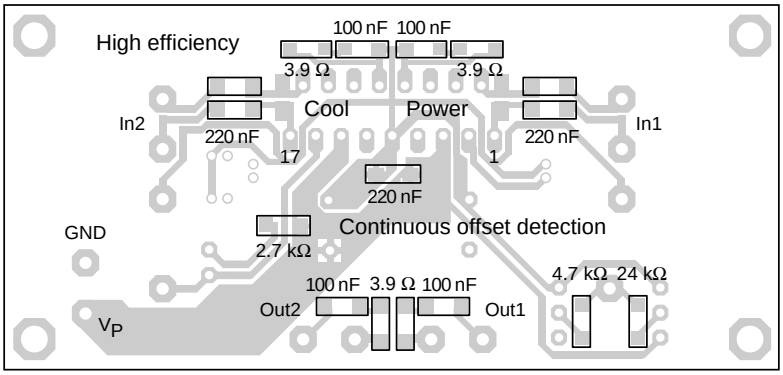
Connect Boucherot filter to pin 8 or pin 10 with the shortest possible connection.

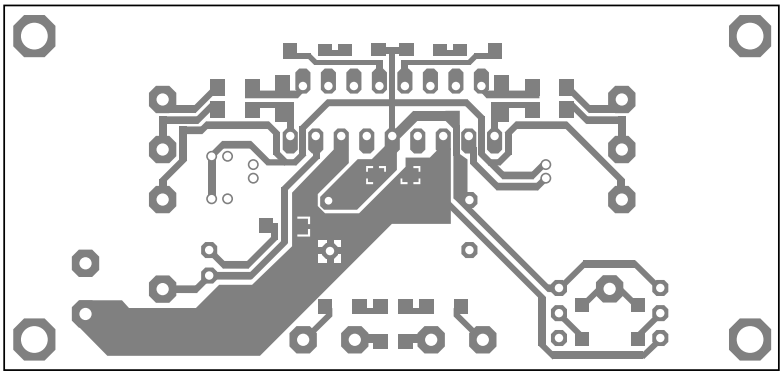
Fig.9 Application diagram (TDA1564J).



Dimensions in mm.

Fig.10 PCB layout (component side) for the application of Fig.9.

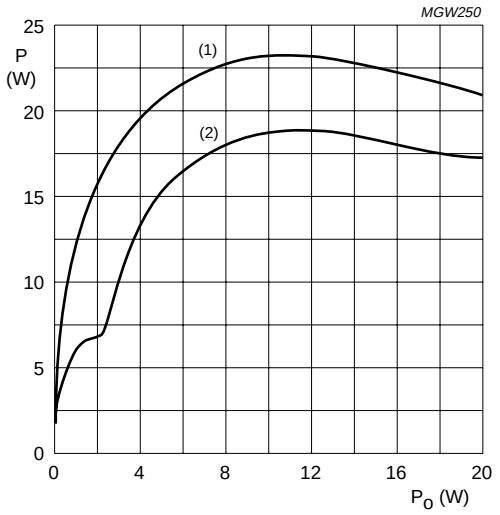




MGW249

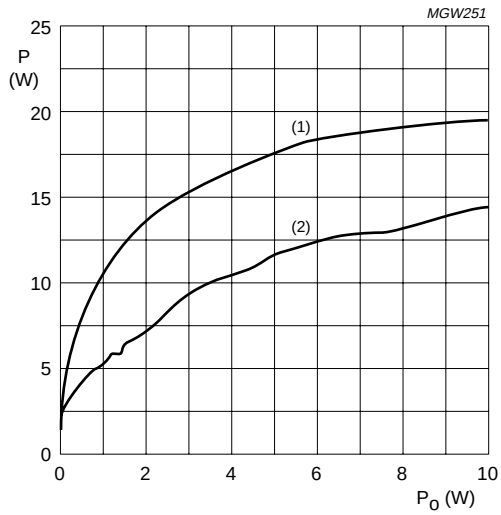
Dimensions in mm.

Fig.11 PCB layout (soldering side) for the application of Fig.9.



Input signal 1 kHz, sinusoidal; V_P = 14.4 V.
(1) For a conventional BTL amplifier.
(2) For TDA1564.

Fig.12 Power dissipation as a function of output power; sine wave driven.



(1) For a conventional BTL amplifier.
(2) For TDA1564.

Fig.13 Power dissipation as a function of output power; pink noise through IEC-60268 filter.

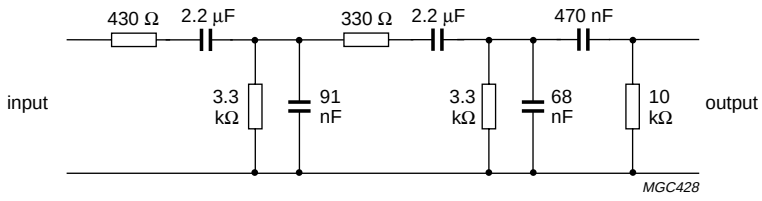


Fig.14 IEC-60268 filter.

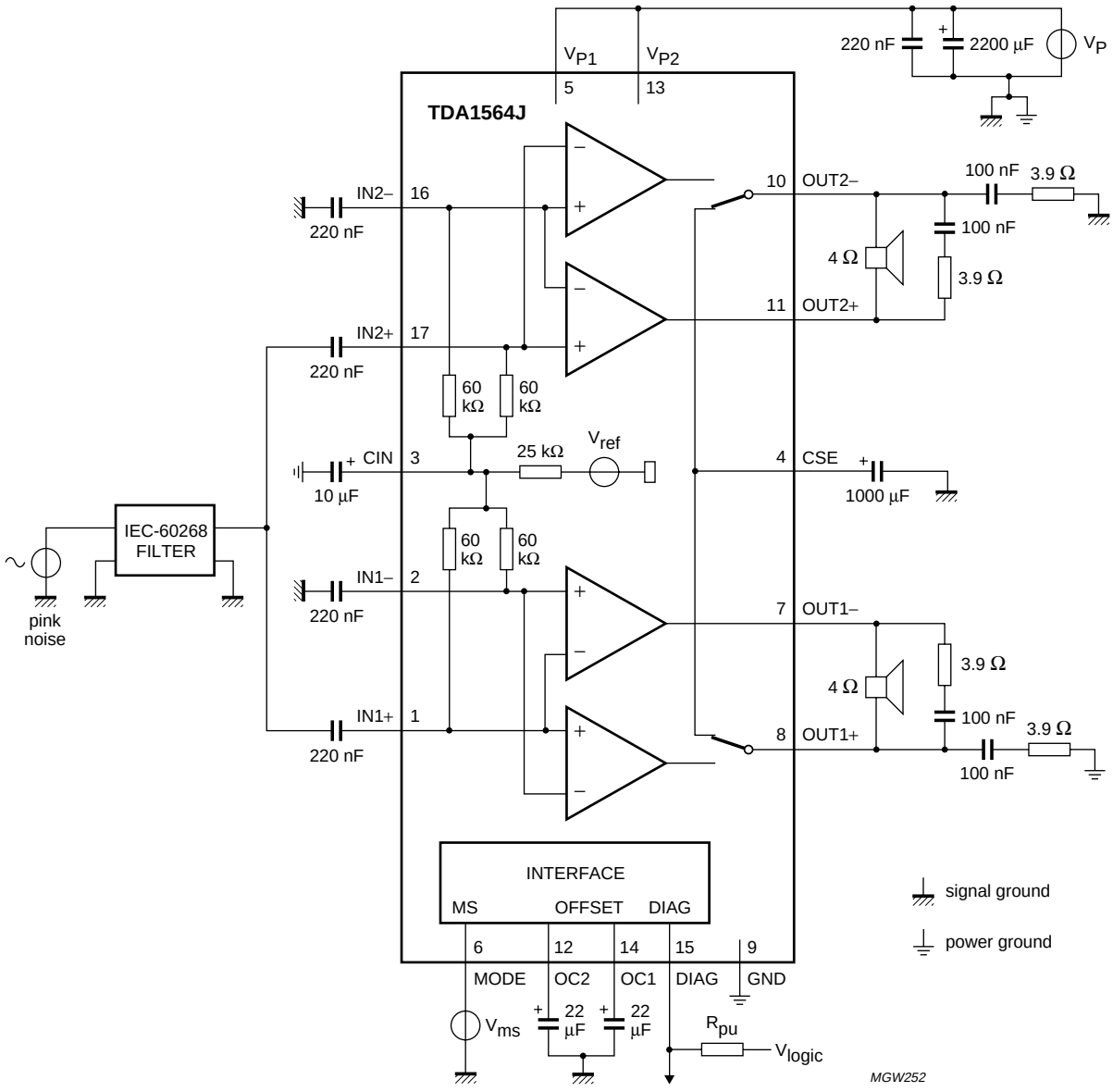
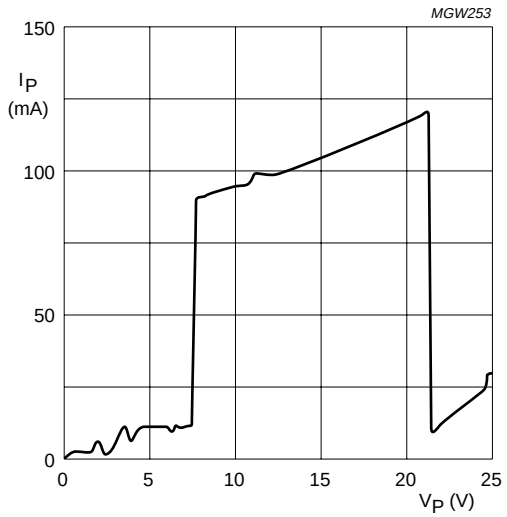
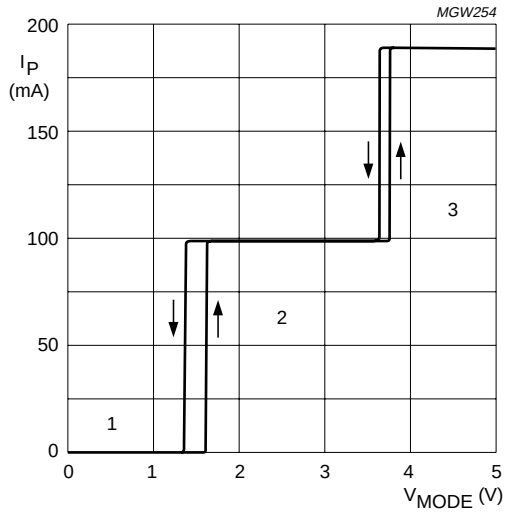


Fig.15 Test and application diagram for dissipation measurements with a music-like signal (pink noise).



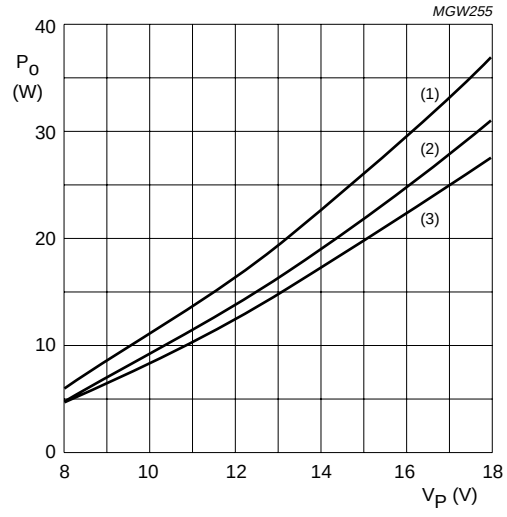
V_{MODE} = 5 V; R_l = ∞.

Fig.16 Quiescent current as a function of supply voltage.



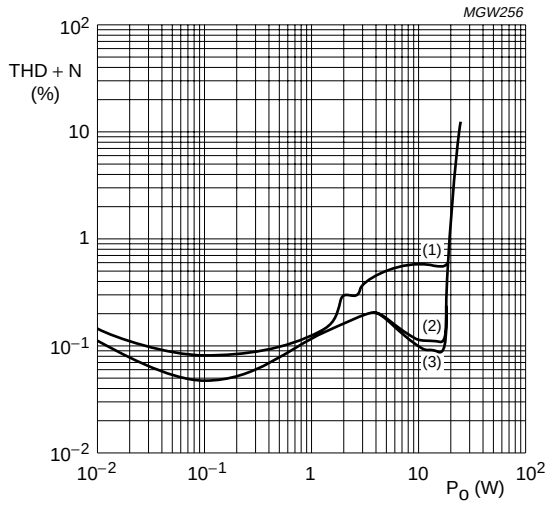
V_P = 14.4 V
(1) Standby.
(2) Mute.
(3) Operating.

Fig.17 Supply current as a function of V_{MODE}.



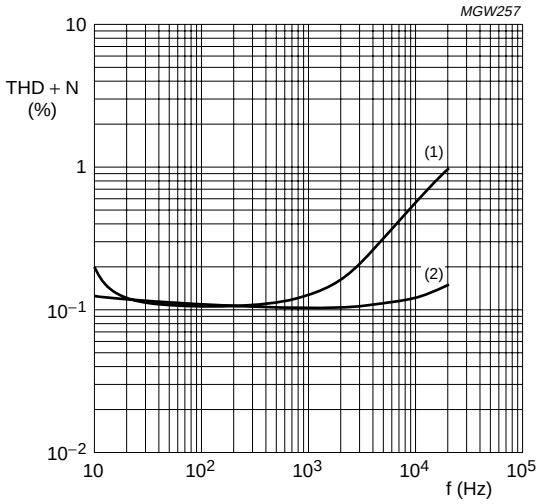
(1) TDH + N = 10 %.
(2) TDH + N = 2.5 %.
(3) TDH + N = 0.5 %.

Fig.18 Output power as a function of supply voltage.



(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 kHz.

Fig.19 THD + noise as a function of output power.



(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.20 THD + noise as a function of frequency.

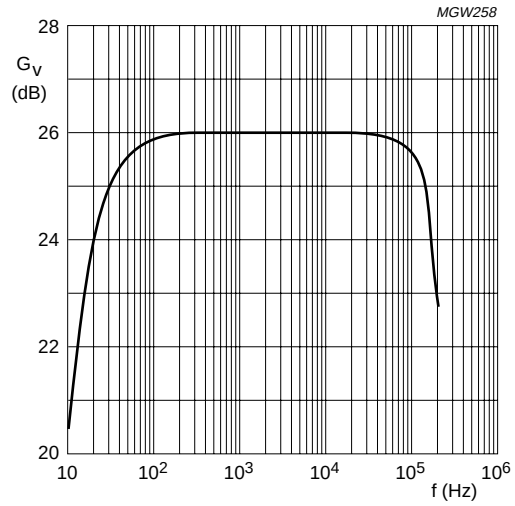
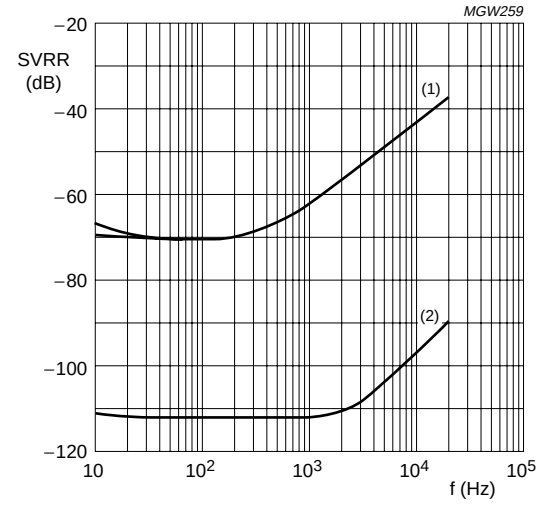
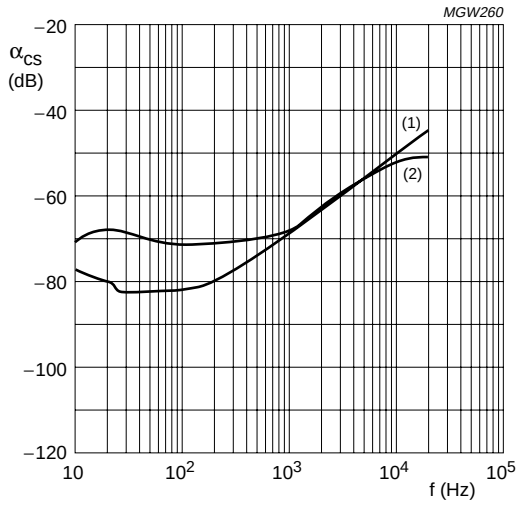


Fig.21 Voltage gain as a function of frequency.



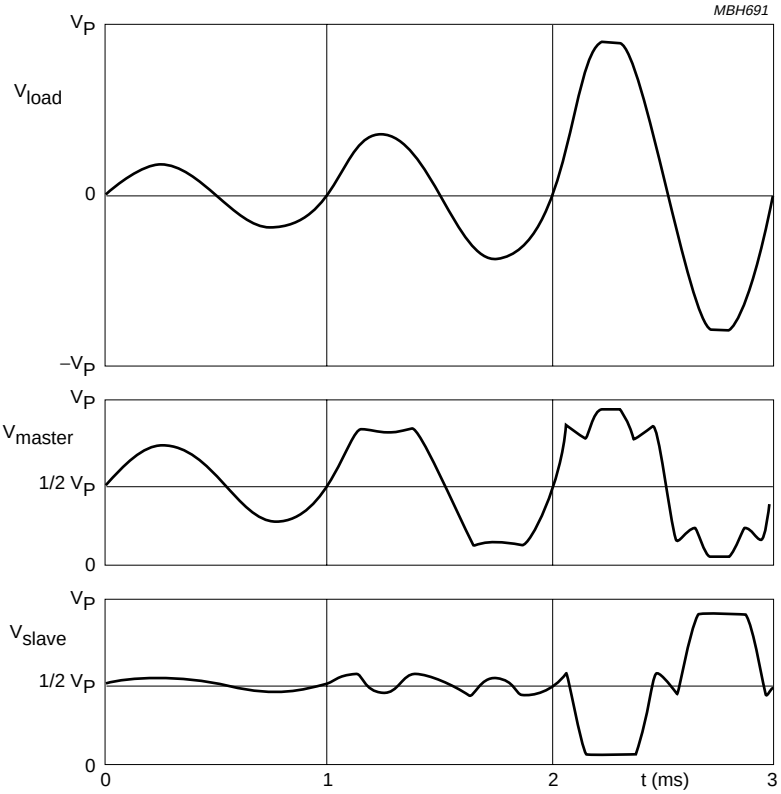
(1) On/Mute.
(2) Standby.

Fig.22 SVRR as a function of frequency.



(1) P_{o2} = 10 W.
(2) P_{o2} = 1 W.

Fig.23 Channel separation as a function of frequency.



See Fig.9
$V_{load} = V_7 - V_8$ or $V_{11} - V_{10}$.
$V_{master} = V_7$ or V_{11}.
$V_{slave} = V_8$ or V_{10}.

Fig.24 Output waveforms.

APPLICATION NOTES

Advantages of high efficiency

1. Power conversion improvement (power supply): Usually, the fact that the reduction of dissipation is directly related to supply current reduction, is neglected. One advantage is less voltage drop in the whole supply chain. Another advantage is less stress for the coil in the supply line. Even the adapter or supply circuit remains cooler than before due to the reduced heat dissipation in the whole chain because more supply current will be converted into output power.
2. Power dissipation reduction: This is the best known advantage of high efficiency amplifiers.
3. Heatsink size reduction: The heatsink size of a conventional amplifier may be reduced with approximately 50 % at V_p = 14.4 V when the TDA1564 will be used. In that case, the maximum heatsink temperature will remain the same.
4. Heatsink temperature reduction: The power dissipation and the thermal resistance of the heatsink determine the heatsink temperature rise.

When the same heatsink size is used from a conventional amplifier, the maximum heatsink temperature decreases and also the maximum junction temperature, which extends the life of this semiconductor device. The maximum dissipation with music-like input signals decreases by 40 %.

It is clear that the use of the TDA1564 saves a significant amount of energy. The maximum supply current decreases by approximately 32 %, that reduces the dissipation in the amplifier as well as in the whole supply chain. The TDA1564 allows a heatsink size reduction of approximately 50 % or the heatsink temperature decreases by 40 % when the heatsink size hasn't been changed.

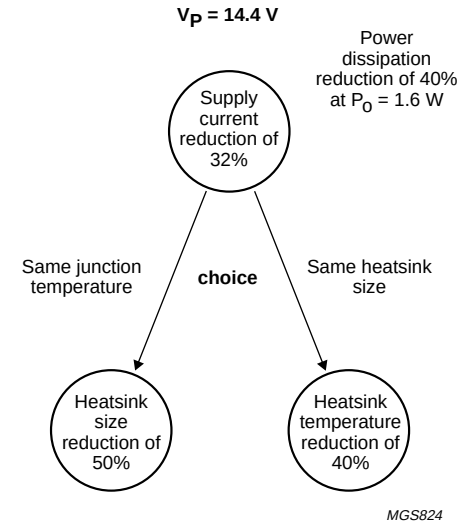
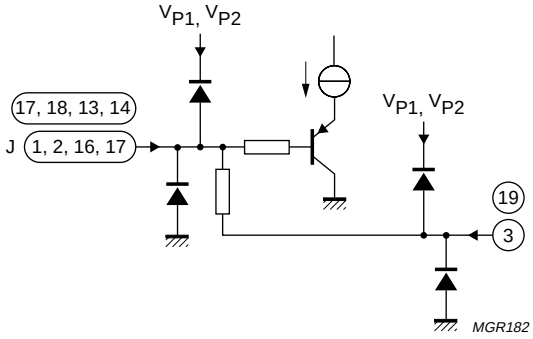
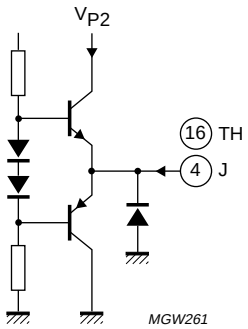
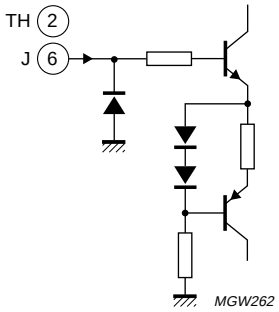


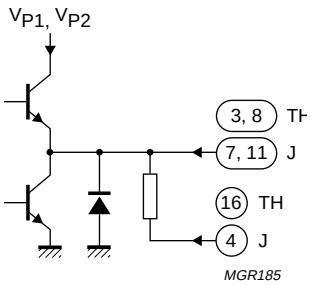
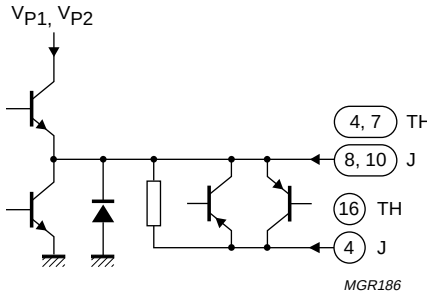
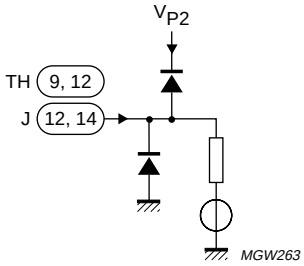
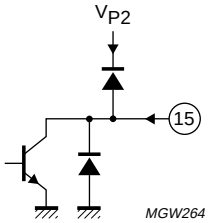
Fig.25 Heatsink design.

Advantage of the concept used by TDA1564

The TDA1564 is highly efficient under all conditions, because it uses a single-ended capacitor to create a non-dissipating half supply voltage. Other concepts rely on the fact that both input signals are the same in amplitude and phase. With the concept of a SE capacitor it means that it doesn't matter what kind of signal processing is done on the input signals. For example, amplitude difference, phase shift or delays between both input signals, or other DSP processing, have no impact on the efficiency.

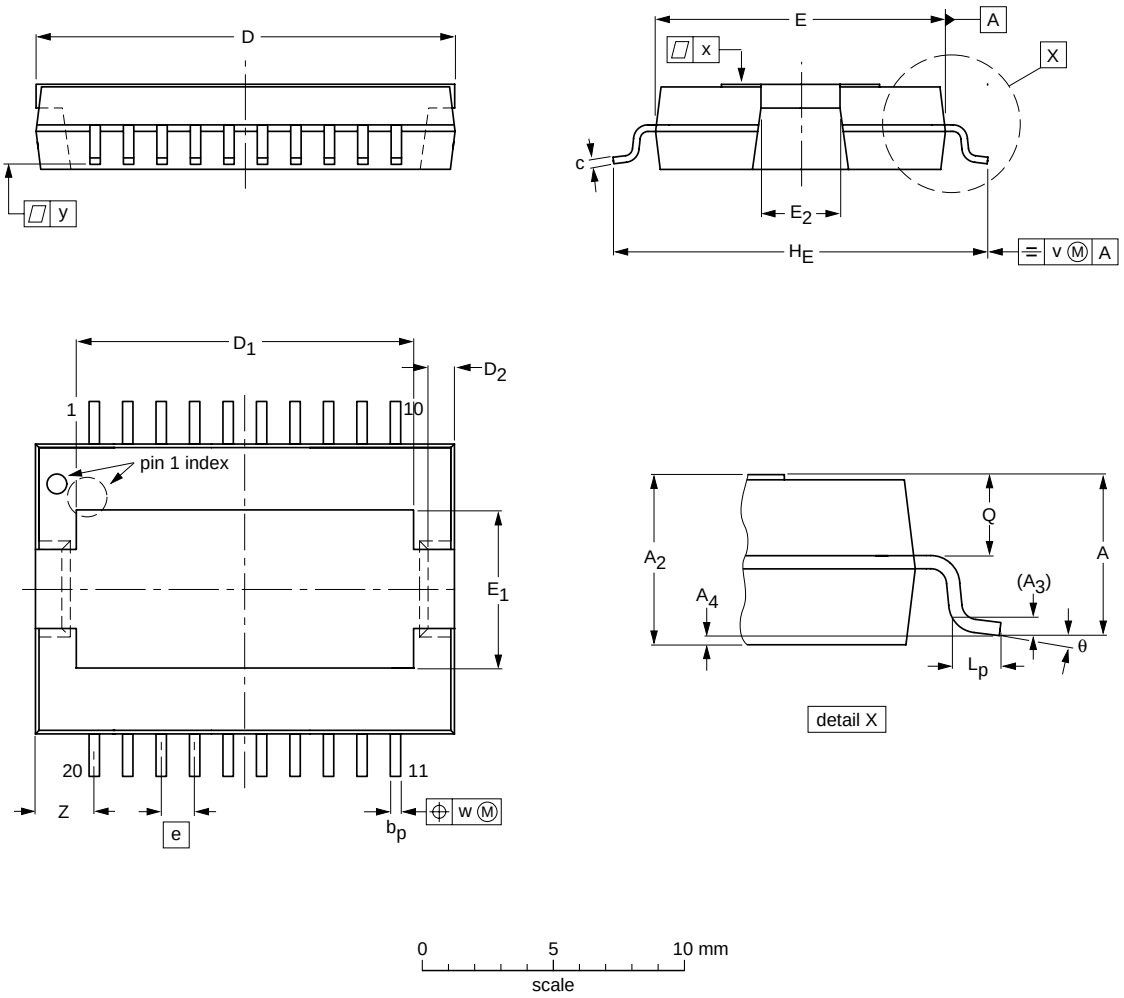
INTERNAL PIN CONFIGURATIONS

PIN		NAME	EQUIVALENT CIRCUIT
TDA1564TH	TDA1564J		
17, 18, 13, 14 and 19	1, 2, 16, 17 and 3	IN1+, IN1–, IN2–, IN2+ and CIN	
16	4	CSE	
2	6	MODE	

PIN		NAME	EQUIVALENT CIRCUIT
TDA1564TH	TDA1564J		
3, 8	7, 11	OUT1–, OUT2+	
4, 7	8, 10	OUT1+, OUT2–	
9, 12	12, 14	OC1, OC2	
15	15	DIAG	

PACKAGE OUTLINES

HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height **SOT418-3**



DIMENSIONS (mm are the original dimensions)

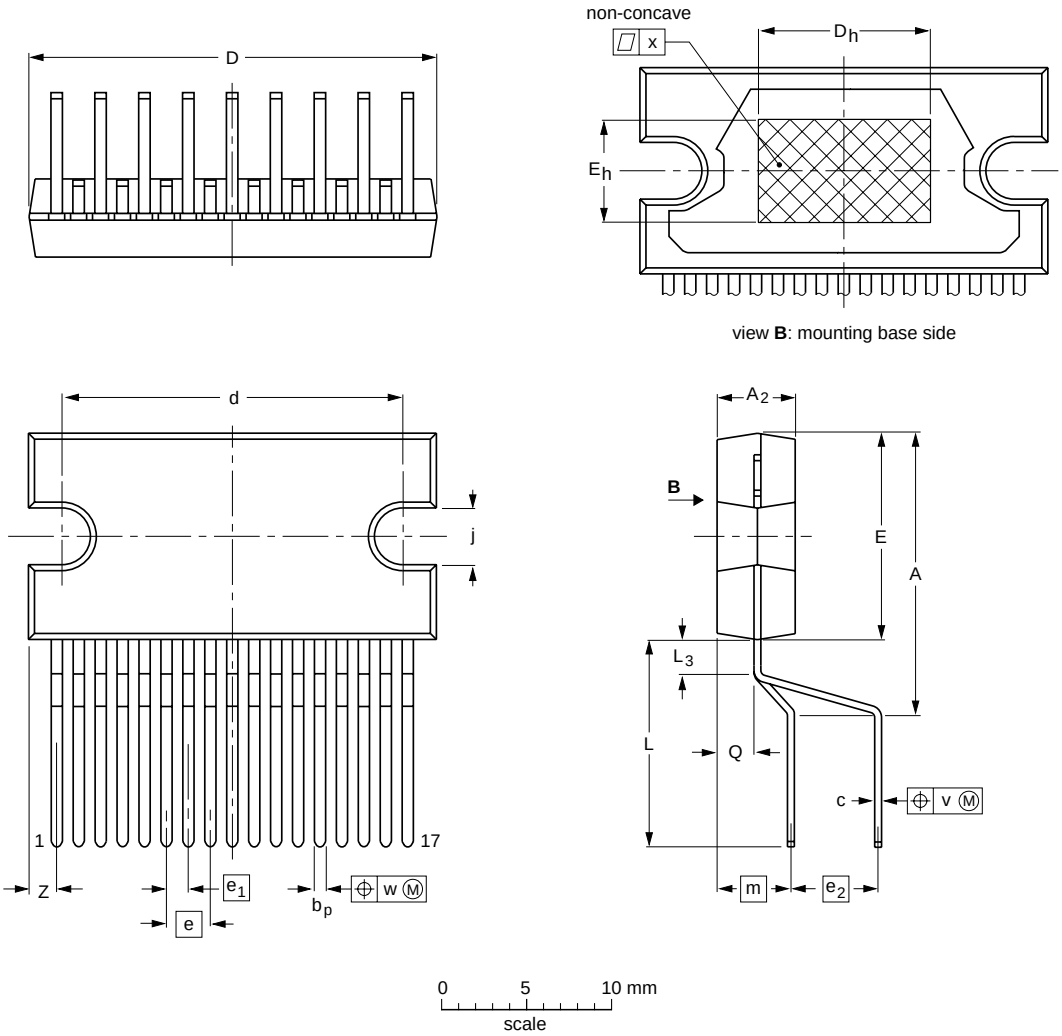
UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 –0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT418-3						~~02-02-12~~ 03-07-23

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT243-1						~~99-12-17~~ 03-03-12

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA, HTSSON..T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be

applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE(1)	SOLDERING METHOD		
		WAVE	REFLOW(2)	DIPPING
Through-hole mount	CPGA, HCPGA	suitable	–	suitable
	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable(3)	–	–
Through-hole-surface mount	PMFP(4)	not suitable	not suitable	–
Surface mount	BGA, HTSSON..T(5), LBGA, LFBGA, SQFP, SSOP-T(5), TFBGA, USON, VFBGA	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable(6)	suitable	–
	PLCC(7), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(7)(8)	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended(9)	suitable	–
	CWQCCN..L(11), PMFP(10), WQCCN32L(11)	not suitable	not suitable	–

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
4. Hot bar soldering or manual soldering is suitable for PMFP packages.
5. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
6. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
7. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

8. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
9. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
10. Hot bar or manual soldering is suitable for PMFP packages.
11. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

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Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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