

AM/FM tuner for car radio and Hi-Fi applications

Not For New Design

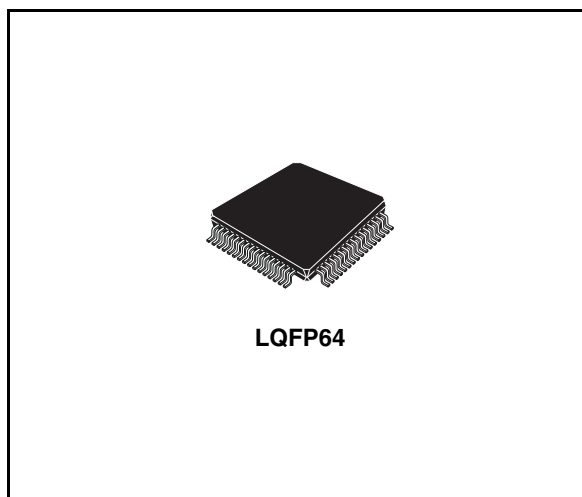
Features

- High performance front-end IC for AM/FM receivers
- Fully integrated high-speed PLL for optimized RDS applications
- FM MPX/AM audio output, 450 kHz AM IF output for stereo AM applications
- AM double conversion architecture
- AM/FM station detector and digital IF-counter
- Single frequency reference for both AM and FM
- Full electrical adjustment
- I²C bus programmable

Description

The TDA7421N is a high-performance tuner circuit which integrates AM and FM sections, PLL frequency synthesizer and IF counter on a single chip.

Use of BiCMOS technology allows the implementation of tuning functions with a minimum of external components. Value spread of external components can be fully compensated by means of on-chip electrical adjustment controlled by external microprocessor.



The FM quality detection circuit, in conjunction with the digital IF counter, enables the stop-station function in “seek” mode and MPX mute during reception. The combination of programmable level detector and IF counter allows reliable AM stop-station performance.

The Automatic Gain Control (AGC) operates on different signal bandwidths in order to optimize sensitivity and dynamic range.

I²C-bus controls functions such as AGC, amplifier gains, PLL and counter settings.

Table 1. Device summary

Order code	Package	Packing
TDA7421N	LQFP64	Tray
E-TDA7421N ⁽¹⁾	LQFP64	Tray

1. In ECOPACK® package see [Section 8: Package information on page 45](#).

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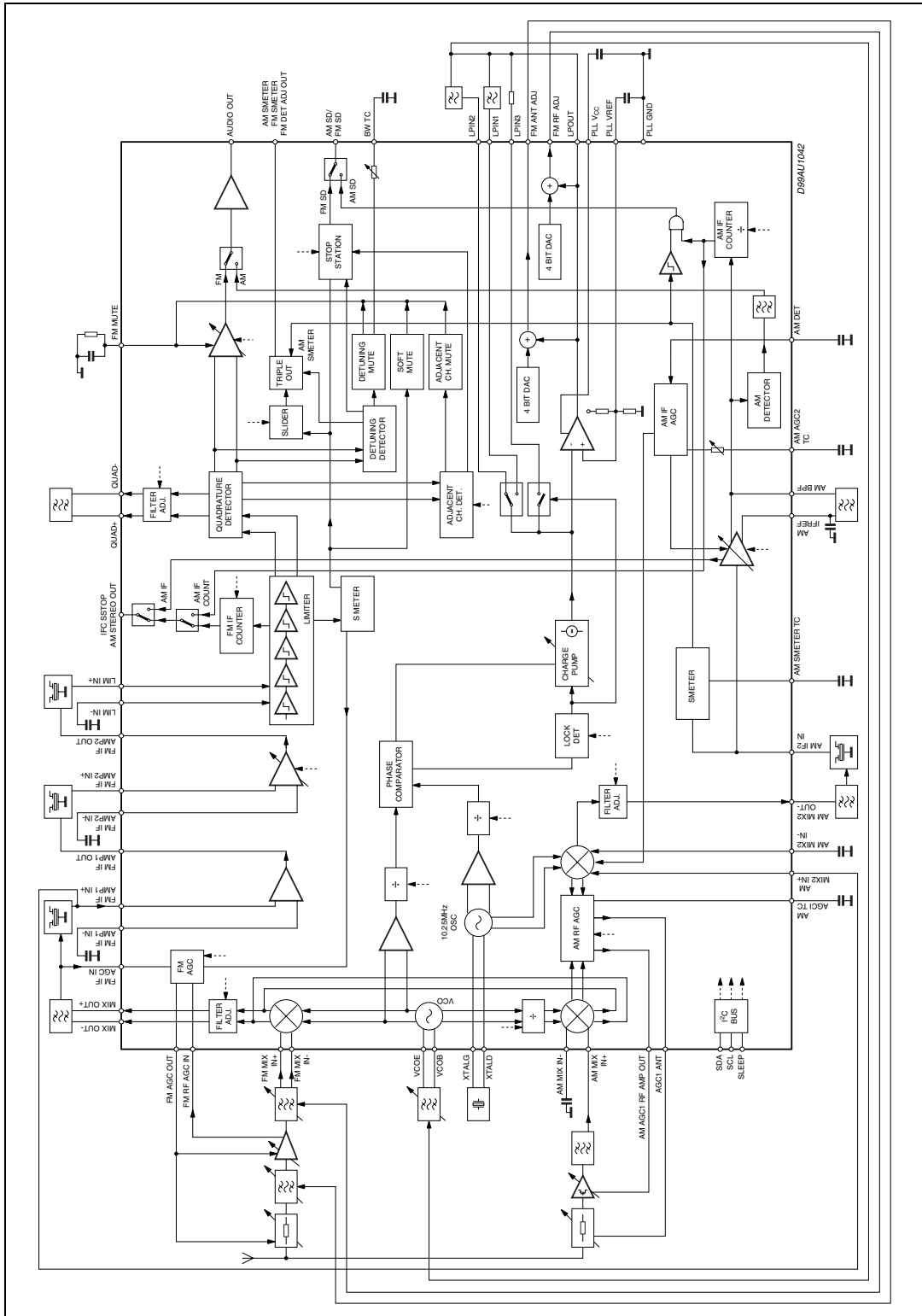
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1 Block diagram

Figure 1. Block diagram



2 Pin description

Figure 2. Pin connection (top view)

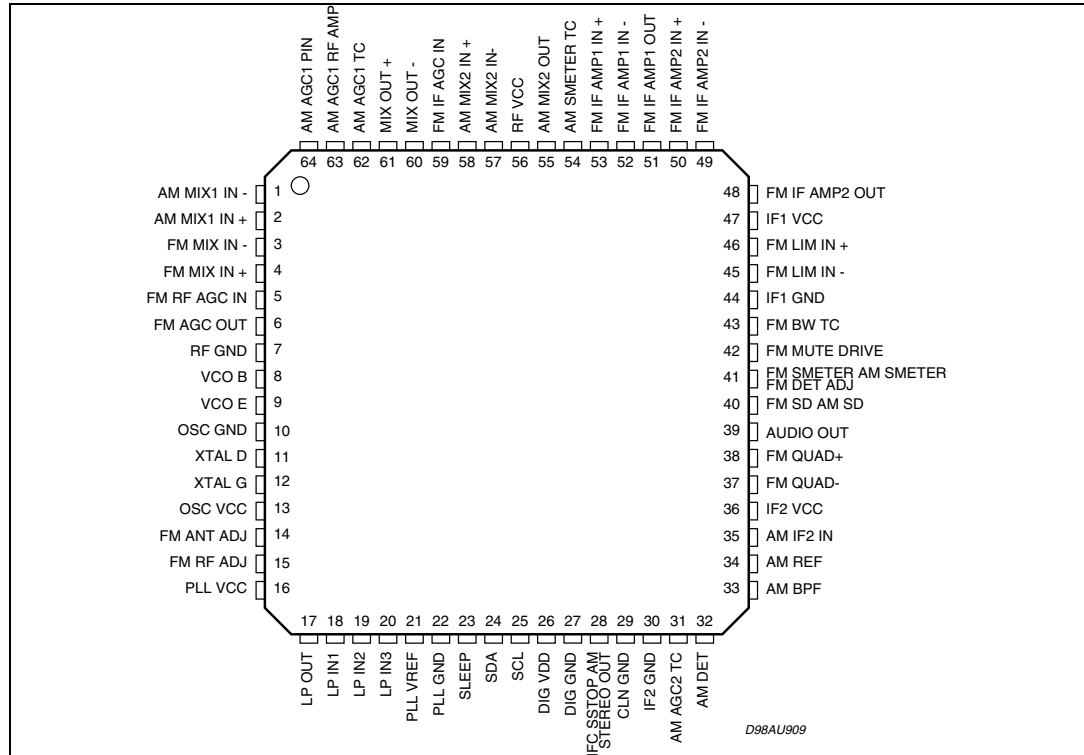


Table 2. Pin description

Pin #	Pin name	Function
1	AM MIX1 IN -	AM 1 st mixer negative input (differential -)
2	AM MIX1 IN +	AM 1 st mixer positive input (differential +)
3	FM MIX1 IN -	FM mixer negative input (differential -)
4	FM MIX1 IN +	FM mixer positive input (differential +)
5	FM RF AGC IN	RF AGC input
6	FM AGC OUT	FM AGC output voltage
7	RF GND	RF ground
8	VCO B	Local oscillator input to the transistor base
9	VCO E	Local oscillator input to the transistor emitter
10	OSC GND	Oscillator ground
11	XTAL D	Crystal oscillator MOS amplifier output
12	XTAL G	Crystal oscillator MOS amplifier input
13	OSC VCC	Oscillator positive supply
14	FM ANT ADJ	Tuning varicap voltage for antenna FM filter

Table 2. Pin description (continued)

Pin #	Pin name	Function
15	FM RF ADJ	Tuning varicap voltage for RF FM filter
16	PLL VCC	PLL positive supply
17	LP OUT	Op Amp output to PLL loop filters
18	LP IN1	FM loop filter connection to op-amp inverting input
19	LP IN2	AM loop filter connection to op-amp inverting input
20	LP IN3	FM-HS loop filter connection to op-amp inverting input
21	PLL VREF	Voltage reference to Op Amp noninverting input
22	PLL GND	PLL ground
23	SLEEP	I ² C bus disconnect signal
24	SDA	I ² C bus data
25	SCL	I ² C bus clock
26	DIG VDD	Digital positive supply
27	DIG GND	Digital ground
28 (*)	IFC SSTOP AM STEREO OUT	IF-Counter stop signal or AM IF2 amplifier output
29	CLN GND	“Clean” ground
30	IF2 GND	IF2 ground
31	AM AGC2 TC	AM 2 nd AGC time constant
32	AM DET	AM detector capacitor
33	AM BPF	AM IF filter
34	AM REF	Reference voltage of AM IF amplifier
35	AM IF2 in	AM IF2 amplifier input
36	IF2 VCC	IF2 positive supply
37	FM QUAD -	FM quadrature detector tank (differential -)
38	FM QUAD +	FM quadrature detector tank (differential +)
39	AUDIO OUT	FM MPX/AM Audio output
40 ⁽¹⁾	FM SD AM SD	FM station detector output or AM station detector output
41 ⁽¹⁾	FM SMETER AM SMETER FM DET ADJ	FM S-meter output or AM S-meter output or FM detector adjustment output
42	FM MUTE DRIVE	FM mute time constant
43	FM BW TC	FM detuning detector time constant
44	IF1 GND	IF1 ground
45	FM LIM IN -	FM limiter negative input (differential -)

Table 2. Pin description (continued)

Pin #	Pin name	Function
46	FM LIM IN +	FM limiter negative input (differential +)
47	IF1 VCC	IF1 positive supply
48	FM IF AMP2 OUT	FM 2 nd IF amplifier output
49	FM IF AMP2 IN -	FM 2 nd IF amplifier negative input (differential -)
50	FM IF AMP2 IN +	FM 2 nd IF amplifier positive input (differential +)
51	FM IF AMP1 OUT	FM 1 st IF amplifier output
52	FM IF AMP IN -	FM 1 st IF amplifier negative input (differential -)
53	FM IF AMP IN +	FM 1 st IF amplifier positive input (differential +)
54	AM S-METER TC	AM S-meter time constant
55	AM MIX2 OUT	AM 2 nd mixer output
56	RF VCC	RF positive supply
57	AM MIX2 IN -	AM 2 nd mixer negative input (differential -)
58	AM MIX2 IN +	AM 2 nd mixer positive input (differential +)
59	FM IF AGC IN	FM IF AGC input
60	MIX OUT -	FM/AM 1 st mixer negative output (differential -)
61	MIX OUT +	FM/AM 1 st mixer positive output (differential +)
62	AM AGC1 TC	AM 1 st AGC time constant
63	AM AGC1 RF AMP	AM 1 st AGC voltage output (to RF amplifier)
64	AM AGC1 PIN	AM 1 st AGC current output (to antenna attenuation diodes)

1. Pin function is user defined by software.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T _{amb}	Operating temperature range	-40 to 85	°C
T _{stg}	Storage Temperature Range	-55 to 150	°C
V _{CC}	Analog Supply Voltages (PLL, RF, IF1, IF2, OSC)	10.2	V
V _{DD}	Digital Supply Voltage	5.5	V

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. Value	Unit
R _{th j-amb, fa}	Thermal resistance junction to ambient, free air	68	°C/W
R _{th j-amb, sol}	Thermal Resistance Junction to ambient, soldered	55	°C/W

3.3 FM section global performances

Table 5. FM section global performances

Refer to evaluation circuit– Input 98.1 MHz, 40 kHz dev., 1 kHz mod., 60 dBmV antenna level, mono.– MPX Output, de-emphasis 50 ms, BPF 200 Hz-15 kHz

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
FM I _{CC}	Total supply current including mixer			90		mA
S+N/N	Signal to noise ratio			66		dB
THD	Total harmonic distortion			0.3		%
V _{O AF}	Audio output level	75 kHz Deviation		400		mV _{RMS}
US ₁	Usable sensitivity (40dB)	antenna level at which S+N/N = 40 dB		0		dB _μ V
US ₂	Usable sensitivity (26dB)	antenna level at which S+N/N = 26 dB		-6		dB _μ V
AGC _{SP}	AGC starting point			55		dB _μ V

3.4 AM section global performances

Table 6. AM section global performances

Refer to evaluation circuit.

Input: $f_c = 999$ kHz, $f_{mod} = 400$ Hz, $m = 30$ %, 74 dB μV_{emf} antenna level unless otherwise specified.

Audio output + RC BPF (BPF 20 Hz - 20 kHz)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ΔI_{CC}	Total supply current including mixers			80		mA
$V_{IN\ MIN}$	Maximum sensitivity	$\Delta V_{AF} = -20$ dB		13		dB μV (emf)
$V_{IN\ US}$	Usable sensitivity	$S+N/N = 20$ dB		27		dB μV (emf)
ΔV_{is}	AGC range	$\Delta V_{AF} = -10$ dB		50		dB
S+N/N	Signal to noise ratio	$V_{INRF} = 74$ dBu		54		dB
α_{IMAG}	Image rejection	$f_{im} = 22.399$ MHz, antenna level @ $V_{AF} = -10$ dB				dB
α_{TW}	Tweet, $\Delta(S+N/N)$	$f_1 = 900$ kHz; $f_2 = 1350$ kHz		1.2		dB
THD	Total harmonic distortion			0.3		%
		$m = 80$ %		1		%
		$V_{INRF} = 120$ dB μV_{emf}		0.3		%
V_{AF}	Audio output level			107		mV _{RM S}
V_{AMST}	AM IF2 output level			105		dB μV

3.5 Electrical characteristics

Table 7. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DC parameters ($T_{amb} = 25$ °C; $V_{CC} = 8$ V, $V_{dd} = 5$ V, no RF input unless otherwise specified)						
PLL V_{CC}	PLL supply voltage		7.5		10	V
PLL I_{CC}	PLL supply current	AM mode		1.6		mA
		FM mode		3.0		mA
DIG V_{dd}	Digital supply voltage		4.75		5.25	V
DIG I_{dd}	Digital supply current	AM mode		4.6		mA
		FM mode		4.0		mA
RF V_{CC}	RF supply voltage		7.5		10	V
RF I_{CC}	RF supply current	AM mode		27.0		mA
		FM mode		13.0		mA

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IF1 V _{CC}	IF1 supply voltage		7.5		10	V
IF1 I _{CC}	IF1 supply current	AM mode		4.0		mA
		FM mode		22.0		mA
IF2 V _{CC}	IF2 supply voltage		7.5		10	V
IF2 I _{CC}	IF2 supply current	AM mode		10.0		mA
		FM mode		28.0		mA
OSC V _{CC}	Oscillator supply voltage		7.5		10	V
OSC I _{CC}	Oscillator supply current	AM mode		17.0		mA
		FM mode		81.0		mA
Voltage controlled oscillator (VCO)						
Ref: FM test circuit, measure V _{osc} with high impedance FET probe						
f _{VCOmin}	Minimum VCO frequency	V _{tun} = 0 Europe/USA Japan		80.9 55	98.2 65.4	MHz
f _{VCOmax}	Maximum VCO frequency	V _{tun} = V _{CC} Europe/USA Japan	123.2 79.2	128 90		MHz
V _{OSC}	Oscillator Amplitude	f _{OSC} = 108.8MHz, Europe/USA f _{OSC} = 72.3MHz Japan		110		dBμV
C/N	Carrier to Noise	1 kHz offset		85		dBc/Hz
Reference Oscillator						
Ref: AM test circuit, measure V _{XTAL} with high impedance FET probe						
f _{XTAL}	Reference frequency			10.25		MHz
V _{XTAL}	Oscillator amplitude			108		dBμV
FM front-end electrical adjustments						
Ref: FM test circuit, measure V _{ANTADJ} and V _{RFADJ} referred to V _{PLLOUT}						
ANTADJ MAX OFF	Maximum FM antenna filter adjustment voltage offset	V _{PLLOUT} = 2.5 V, ANA3-0 set to 1111	21	25	27	%
ANTADJ STEP OFF	FM antenna filter adjustment voltage offset step	V _{PLLOUT} = 2.5 V, ANA3-0 set to 1001	2.8	3.6	4.4	%
RFADJ MAX OFF	Maximum FM RF filter adjustment voltage offset	V _{PLLOUT} = 2.5 V, RFA3-0 set to 1111	21	25	27	%
RFADJ STEP OFF	FM RF filter adjustment voltage offset step	V _{PLLOUT} = 2.5 V, RFA3-0 set to 1001	2.8	3.6	4.4	%
FM mixer						
Ref: FM test circuit, measure input at V _{MIXFMIN} , output at V _{MIXOUT}						
R _{IN,MIX}	Single-ended input resistance (pin 3, pin4)			12		Ω
G _{MIX}	Conversion gain	f _{IN} = 98.1 MHz		21.8		dB
IP _{3MIX}	3rd order intermodulation distortion intercept point	f _d = 98.1 MHz; f _{u1} = 98.2 MHz; f _{u2} = 98.3 MHz;		108		dBμV

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
CP1 _{MIX}	1dB compression point	$f_{IN} = 98.1 \text{ MHz}$		90		dB μ V
CAdj1	Value of the minimum adjusting capacitance step	T1A3-0 set to 1000		0.38		pF
FM AGC						
Ref: FM test circuit, measure input at $V_{FMRFAGCIN}$ and $V_{FMIFAGCIN}$, output at $V_{FMAGCOUT}$						
$V_{RFAGCSTART}$	Open loop RF AGC starting point	$f_{RFAGCIN} = 98.1 \text{ MHz}$ Value of $V_{FMRFAGCIN}$ at which $V_{FMAGCOUT} = 4 \text{ V}$		80		dB μ V
$R_{IN,RFAGC}$	Input resistance			20		K Ω
$V_{IFAGCTART}$	Open loop IF AGC starting point	$f_{IFAGCIN} = 10.7 \text{ MHz}$ Value of $V_{FMIFAGCIN}$ at which $V_{FMAGCOUT} = 4 \text{ V}$ FAGC2-0 set to 111		77		dB μ V
$R_{IN,IFAGC}$	Input resistance			20		K Ω
$R_{OUT,FMAGC}$	Output resistance			10		K Ω
FM IF amplifier 1						
Ref: FM test circuit, measure input at $V_{FMAMP1IN}$, output at $V_{FMAMP1OUT}$						
$R_{IN,AMP1}$	Input resistance			330		Ω
$R_{OUT,AMP1}$	Output resistance			330		Ω
G_{AMP1}	Typical gain	$f_{IN} = 10.7 \text{ MHz}$		18.5		dB
IP3 _{AMP1}	3rd order intermodulation distortion intercept point	$f_d = 10.7 \text{ MHz}$; $f_{u1} = 10.8 \text{ MHz}$; $f_{u2} = 10.9 \text{ MHz}$; FBH3-0 set to 0100				dB μ V
CP1 _{AMP1}	1dB compression point	$f_{IN} = 10.7 \text{ MHz}$; FBH3-0 set to 0100				dB μ V
FM IF amplifier 2						
Ref: FM test circuit, measure input at $V_{FMAMP2IN}$, output at $V_{FMAMP2OUT}$						
$R_{IN,AMP2}$	Input resistance	$f = 10.7 \text{ MHz}$		330		Ω
$R_{OUT,AMP2}$	Output resistance	$f = 10.7 \text{ MHz}$		330		Ω
$G_{MIN,AMP2}$	Minimum gain	$f_{IN} = 10.7 \text{ MHz}$, FBL1-0 set to 01		6		dB
$G_{MAX,AMP2}$	Maximum gain	$f_{IN} = 10.7 \text{ MHz}$, FBL1-0 set to 00		10		dB
IP3 _{AMP2}	3rd order intermodulation distortion intercept point	$f_d = 10.7 \text{ MHz}$; $f_{u1} = 10.8 \text{ MHz}$; $f_{u2} = 10.9 \text{ MHz}$; FBL3-0 set to 0100				dB μ V
CP1 _{AMP2}	1dB compression point	$f_{IN} = 10.7 \text{ MHz}$; FBL3-0 set to 0100				dB μ V

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
FM limiter, field strength meter and demodulator						
Ref: FM test circuit, measure:						
– Input at $V_{FMLIMIN}$, $f_{IN} = 10.7$ MHz						
– FS meter output at $V_{FSMETER}$ (FMADJ set to 0, FSL4-0 set to 00000)						
– demodulator adjustment output at $V_{FSMETER}$ (FMADJ set to 1)						
$R_{IN,LIM}$	Limiter input resistance			330		Ω
G_{LIM}	Limiter gain			90		dB
LS	Limiting sensitivity			23		dB μ V
SM1	Smeter 1	$V_{FMLIMIN} = 40$ dB μ V		1.1		V
SM2	Smeter 2	$V_{FMLIMIN} = 60$ dB μ V		2.3		V
SM3	Smeter 3	$V_{FMLIMIN} = 80$ dB μ V		3.7		V
SM4	Smeter 4	$V_{FMLIMIN} = 100$ dB μ V		4.9		V
$SM_{Min\ shift}$	Smeter minimum shift voltage	$V_{FMLIMIN} = 70$ dB μ V; FSL4-0 set to 00000		0.0		V
$SM_{Max\ shift}$	Smeter maximum shift voltage	$V_{FMLIMIN} = 70$ dB μ V; FSL4-0 set to 11111		1.5		V
G_{DEM}	Demodulator conversion gain	$V_{FMLIMIN} > LS$		2		mV _{RMS} /kHz
G_{DEMADJ}	Demodulator adjustment conversion gain	$V_{FMLIMIN} > LS$		14		mV _{RMS} /kHz
CA _{AdjDem}	Value of the minimum adjusting capacitance step	DEM6-0 set to 0000001		50		fF
FM audio amplifier						
Ref: FM test circuit, $V_{FMLIMIN} = 95$ dB μ V, $f_{IN} = 10.7$ MHz; measure:						
– MPX output at V_{AUDIO} , BPF 200 Hz to 15 kHz, 50 μ s de-emphasis.						
– muting voltage at $V_{MUTE, DRIVE}$						
V_{MUTE}	Mute voltage	$V_{MUTE,DRIVE}$ for which $\Delta V_{AF} = -11.5$ dB; AUM1-0 set to 11	2			V
V_{PLAY}	Play voltage	$V_{MUTE,DRIVE}$ for which $\Delta V_{AF} = -1$ dB, AUM1-0 set to 11			0.3	V
$G_{AMP,PLAY}$	Audio amplifier gain in play conditions	$V_{MUTE,DRIVE} < V_{PLAY}$		9		dB
MUTEATT _{MIN}	Minimum mute attenuation	$V_{MUTE,DRIVE} > V_{MUTE}$; AUM1-0 set to 00		-5		dB
MUTEATT _{MAX}	Maximum mute attenuation	$V_{MUTE,DRIVE} > V_{MUTE}$; AUM1-0 set to 11		-12.5		dB
V_{AF}	AF output level	$f_{DEV} = 75$ KHz, $F_{MOD} = 1$ kHz, $V_{MUTE,DRIVE} < V_{MUTE}$		400		mV _{RMS}
THD	AF total harmonic distortion	$f_{DEV} = 40$ kHz, $F_{MOD} = 1$ kHz, $V_{MUTE,DRIVE} < V_{MUTE}$		0.3		%

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
S+N/N	AF signal to noise ratio	$f_{DEV} = 40 \text{ kHz}$, $F_{MOD} = 1 \text{ kHz}$, $V_{MUTE,DRIVE} < V_{MUTE}$		80		dB
AMR	Amplitude modulation rejection	AM modulation depth 30 %, $f_{MOD} = 1 \text{ kHz}$, with respect to FM modulated signal with $f_{DEV} = 40 \text{ kHz}$, $V_{MUTE,DRIVE} < V_{MUTE}$		67		dB
AUDIO _{curr}	Output current capability		5			mA
MUTE R _{out}	Mute drive output resistance			1		K Ω
FM quality detectors						
Field strength detector Ref: FM test circuit, HDDIS and BWDIS set to 1, measure: – Input at $V_{FMLIMIN}$, $f_{IN} = 10.7 \text{ MHz}$, CW – output at $V_{MUTE,DRIVE}$						
FSD _{MIN}	Field strength detector minimum threshold	$V_{FMLIMIN}$ level at which $V_{MUTE,DRIVE} = V_{MUTE}$, FSM3-0 set to 0000				dB μ V
FSD _{MAX}	Field strength detector maximum threshold	$V_{FMLIMIN}$ level at which $V_{MUTE,DRIVE} = V_{MUTE}$, FSM3-0 set to 1111		67.5		dB μ V
Detuning detector						
Ref: FM test circuit; HDDIS and SMDIS set to 1, measure: – Input at $V_{FMLIMIN}$, CW – output at $V_{MUTE,DRIVE}$						
DD _{START}	Detuning detector starting point	frequency shift from 10.7 MHz at which $V_{MUTE,DRIVE} = V_{PLAY}$		± 23		kHz
DD _{Slope,min}	Detuning detector minimum muting slope	frequency shift from 10.7 MHz + DD _{START} at which $V_{MUTE,DRIVE} = V_{MUTE}$, BWM2-0 set to 100, SEEK set to 0		30		kHz
DD _{Slope,max}	Detuning detector maximum muting slope	frequency shift from 10.7 MHz + DD _{START} at which $V_{MUTE,DRIVE} = V_{MUTE}$, BWM2-0 set to 001, SEEK set to 0		10		kHz
DD _{TRC}	Detuning Detector Time Constant Ratio	ratio of "reception" mode integration time constant inside the Detuning Detector with respect to "seek" mode		34/6		s/s
Adjacent channel detector						
Ref: FM test circuit; BWDIS and SMDIS set to 1, measure: – Input at $V_{FMLIMIN}$: desired 10.7 MHz, 95 dB μ V CW; undesired 10.8 MHz CW – output at $V_{MUTE,DRIVE}$						
ACD _{MAX}	Adjacent channel quality detector maximum sensitivity threshold	amplitude of undesired signal at which $V_{MUTE,DRIVE} = V_{MUTE}$, HDM4-0 set to 1111		91		dBu

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ACD _{MIN}	Adjacent channel quality detector minimum sensitivity threshold	amplitude of undesired signal at which V _{MUTE,DRIVE} = V _{PLAY} ; HDM4-0 set to 00000		94.8		dBu
Field strength station detector						
Ref: FM Test circuit; SEEK set to 1, HDDIS and BWDIS set to 1, measure: – Input at V _{FMLIMIN} : desired 10.7MHz, CW – Output at V _{FMDS}						
FSSD _{MIN}	Field strength station detector minimum threshold	V _{FMLIMIN} level at which V _{FMDS} = 2.5V; FSS4-0 set to 00000				dB _μ V
FSSD _{MAX}	Field strength station detector maximum threshold	V _{FMLIMIN} level at which V _{FMDS} = 2.5V; FSS4-0 set to 11111				dB _μ V
Detuning station detector						
Ref: FM test circuit; SEEK set to 1, HDDIS and SMDIS set to 1, measure: – Input at V _{FMLIMIN} ; CW; – Output at V _{FMDS}						
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DSD	Detuning Station Detector Threshold	frequency shift from 10.7MHz at which V _{FMDS} = 2.5V		±28		KHz
Adjacent channel station detector						
Ref: FM test circuit; SEEK set to 1, HDDIS and SMDIS set to 1, measure: - Input at V _{FMLIMIN} : desired 10.7MHz, 95dB _μ V CW; undesired 10.8MHz CW - output at V _{FMDS}						
ACSD _{MAX}	Adjacent channel detector maximum sensitivity threshold	amplitude of undesired signal at which V _{FMDS} = 2.5V, HDM4-0 set to 11111		92.5		dB _μ V
ACSD _{MIN}	Adjacent channel detector minimum sensitivity threshold	amplitude of undesired signal at which V _{FMDS} = 2.5V, HDM4-0 set to 00000		94.9		dB _μ V
AM mixer 1						
Ref: AM test circuit, measure input at V _{MIX1AMIN} , output at V _{MIXOUT}						
R _{IN,MIX1}	Input resistance			1.2		KΩ
G _{MIX1}	Conversion gain	f _{IN} = 1 MHz		7.6		dB
IP _{3MIX1}	3rd order intermodulation distortion intercept point	f _d = 1MHz; f _{u1} = 1.1MHz; f _{u2} = 1.2MHz		131		dB _μ V
CP _{1MIX1}	1dB compression point	f _{IN} = 1MHz		110		dB _μ V
CAdj1	Value of the minimum adjusting capacitance step	T1A3-0 set to 1000		0.38		pF

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
AM wide and narrow AGC						
Ref: AM test circuit; measure input at $V_{MIX1AMIN}$ and $V_{MIX2AMIN}$, output at $V_{AMAGC1AMP}$ and $V_{AMAGC1PIN}$						
$V_{WAGCMIN}$	Open loop wide AGC minimum starting point	$f_{WAGCIN} = 999 \text{ kHz}$, AAGW1-0 set to 11; $V_{MIX1AMIN}$ at which $V_{AMAGC1AMP} = 2.5V$		95		$\text{dB}\mu\text{V}$
$V_{WAGCMAX}$	Open loop wide AGC maximum starting point	$f_{WAGCIN} = 999 \text{ kHz}$, AAGW1-0 set to 00; $V_{MIX1AMIN}$ at which $V_{AMAGC1AMP} = 2.5V$		101		$\text{dB}\mu\text{V}$
$V_{NAGCMIN}$	Open loop narrow AGC minimum starting point	$f_{NAGCIN} = 10.7 \text{ MHz}$, AAGN1-0 set to 11; $V_{MIX2AMIN}$ at which $V_{AMAGC1AMP} = 2.5V$		81		$\text{dB}\mu\text{V}$
$V_{NAGCMAX}$	Open loop narrow AGC maximum starting point	$f_{NAGCIN} = 10.7 \text{ MHz}$, AAGN3-0 set to 00; $V_{MIX2AMIN}$ at which $V_{AMAGC1AMP} = 2.5V$		87		$\text{dB}\mu\text{V}$
$R_{OutAMAGC1}$	Output resistance			23.3		$\text{k}\Omega$
$I_{AMAGC1PIN}$	Maximum antenna attenuation diode current	$f_{WAGCIN} = 999 \text{ kHz}$; $V_{MIX1AMIN} = 120\text{dB}\mu\text{V}$; AAGW1-0 set to 00		1.4		mA
AM mixer 2						
Ref: AM Test Circuit; measure input at $V_{MIX2AMIN}$, output at $V_{MIX2OUT}$ (switches must be in position 2 for AGC measurements).						
$R_{IN,MIX2}$	Input resistance			5		$\text{K}\Omega$
G_{MIX2}	Maximum conversion gain	$f_{IN} = 10.7 \text{ MHz}$		25		dB
$IP3_{MIX2}$	3rd order intermodulation distortion intercept point	$f_d = 10.7 \text{ MHz}$; $f_{u1} = 10.8 \text{ MHz}$; $f_{u2} = 10.9 \text{ MHz}$		117		$\text{dB}\mu\text{V}$
$CP1_{MIX2}$	1dB compression point	$f_{IN} = 10.7 \text{ MHz}$		107		$\text{dB}\mu\text{V}$
CA_{dj2}	Value of the minimum adjusting capacitance step	T2A3-0 set to 0001		1.57		pF
AGC_{MIXSP}	AGC2 starting point on mixer 2	$f_{IN} = 10.7 \text{ MHz}$; Value of $V_{MIX2AMIN}$ for which $V_{MIX2OUT}$ is 1 dB compressed; IF2A1-0 set to 10		48		$\text{dB}\mu\text{V}$
AGC_{MIXIS}	AGC2 intervention slope on mixer 2	$f_{IN} = 10.7 \text{ MHz}$; $\Delta V_{MIX2OUT}$ for $\Delta V_{MIX2AMIN} = 1 \text{ dB}$; IF2A1-0 set to 10		0.1		dB/dB
AGC_{MIXR}	AGC2 range on mixer 2	$f_{IN} = 10.7 \text{ MHz}$; range of $V_{MIX2AMIN}$ above AGC_{MIXSP} for which $V_{MIX2OUT}$ is not increasing linearly with a 1dB/dB slope; IF2A1-0 set to 10	50			dB
AM IF2 amplifier						
Ref: AM test circuit; $f_{IN} = 450 \text{ kHz}$, measure input at $V_{IF2AMPIN}$, output at $V_{IF2AMPOUT}$ (switches must be in position 1).						
$R_{IN,IF2AMP}$	Input resistance			2		$\text{k}\Omega$

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$G_{IF2AMP\text{MIN}}$	Minimum gain	$V_{IF2AMP\text{PIN}} = 10 \text{ dB}\mu\text{V}$; IF2A1-0 set to 00		50		dB
$G_{IF2AMP\text{MAX}}$	Maximum gain	$V_{IF2AMP\text{PIN}} = 10 \text{ dB}\mu\text{V}$; IF2A1-0 set to 11		59		dB
$AGC_{AMP\text{PSP}}$	AGC2 starting point on IF2 amp	Value of $V_{IF2AMP\text{PIN}}$ for which $V_{IF2AMP\text{OUT}}$ is 1dB compressed, IF2A1-0 set to 01		60		$\text{dB}\mu\text{V}$
$AGC_{AMP\text{PR}}$	AGC2 range on IF2 amp	$f_{IN} = 10.7\text{MHz}$ Range of $V_{IF2AMP\text{PIN}}$ above $AGC_{AMP\text{PSP}}$ for which $V_{IF2AMP\text{OUT}}$ is not increasing linearly with a 1dB/dB slope; IF2A1-0 set to 01		33		dB
$AGC_{AMP\text{PIS}}$	AGC2 intervention slope on IF2 amp	$f_{IN} = 10.7\text{MHz}$; $\Delta V_{IF2AMP\text{OUT}}$ for $\Delta V_{IF2AMP\text{PIN}} = 1\text{dB}$; IF2A1-0 set to 1		0.1		dB/dB
AGC_{TCR}	AGC2 time constant ratio	Ratio of AGC2 "reception" Time Constant and "seek" Time Constant		150/5		s/s
$IF_{AM\text{ST}}$	AM IF2 output level at pin 28	$V_{IF2AMP\text{PIN}} = 72\text{dBmV}$; AMSTEREO set to 1		106		$\text{dB}\mu\text{V}$
$IF_{AM\text{STcurr}}$	Current capability of pin 28	AMSTEREO set to 1		150		μA
AM Field strength meter and field strength station detector						
Ref: AM test circuit; $f_{IN} = 10.7 \text{ MHz}$, measure input at $V_{MIX2AMIN}$, outputs at $V_{AMSMETER}$ and at V_{AMSD} (switches in position 2).						
AMSM1	AM smeter 1 at $V_{AMSMETER}$	$V_{MIX2AMIN} = 40\text{dB}\mu\text{V}$		1.4		V
AMSM2	AM smeter 2 at $V_{AMSMETER}$	$V_{MIX2AMIN} = 60\text{dB}\mu\text{V}$		3.4		V
AMSM3	AM smeter 3 at $V_{AMSMETER}$	$V_{MIX2AMIN} = 80\text{dB}\mu\text{V}$		4.8		V
$AMSD_{\text{MIN}}$	Station detector minimum threshold	$V_{MIX2AMIN}$ at which $V_{AMSD} = 2.5\text{V}$; ASS3-0 set to 0000, SEEK set to 1		27		$\text{dB}\mu\text{V}$
$AMSD_{\text{MAX}}$	Station detector maximum threshold	$V_{MIX2AMIN}$ at which $V_{AMSD} = 2.5\text{V}$; ASS3-0 set to 1111, SEEK set to 1				$\text{dB}\mu\text{V}$
IF counter output						
Ref: AM & FM test circuit, measure at pin 28						
IFC_{FM}	FM IFC sensitivity	$V_{F\text{MLIMIN}}$ at which $V_{\text{pin 28}} = 2.5\text{V}$, SEEK set to 1, EW2-0 set to 101, IFS2-0 set to 010		34		$\text{dB}\mu\text{V}$
IFC_{AM}	AM IFC sensitivity	$V_{IF2AMP\text{PIN}}$ at which $V_{\text{pin 28}} = 2.5\text{V}$, SEEK set to 1, EW2-0 set to 011, IF2-0 set to 100, AMFM STBY1-0 set to 10		29		$\text{dB}\mu\text{V}$
IFC_{current}	IFC current capability			150		μA

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SD output impedance						
Measure output at $V_{FM\text{SD}}$						
$SD_{IMP,ON}$	SD output impedance	SDDIS set to 0			700	W
$SD_{IMP,TS}$	SD output impedance (Tri-state)	SDDIS set to 1	7			M Ω
Loop filter input/output						
(LP_IN1, LP_IN2, LP_IN3, LP_OUT)						
$-I_{IN}$	Input leakage current	$V_{IN} = \text{GND}; PD_{out} = \text{Tristate}$	-2	0	2	μA
I_{IN}	Input leakage current	$V_{IN} = V_{DD}; PD_{out} = \text{Tristate}$	-2	0	2	μA
V_{OL}	Output voltage low	$I_{IN} = -0.2 \text{ mA}; V_{CC} = 8.5 \text{ V}$			0.5	V
V_{OH}	Output voltage high	$I_{OUT} = 0.2 \text{ mA}; V_{CC} = 8.5 \text{ V}$	8			V
I_{OUT}	Output current sink	$V_{PLL} = 8.5 \text{ V};$	10			mA
I_{OUT}	Output current source	$V_{out} = 0.5 \text{ to } 8 \text{ V}$	10			mA
I²C bus Interface						
f_{SCL}	SCL clock frequency			100	500	kHz
t_{AA}	SCI low to SDA data valid			300		ns
t_{buf}	Time the bus must be free for the new transmission			4.7		μs
t_{HD-STA}	Start condition hold time			4.0		μs
t_{LOW}	Clock low period			4.7		μs
t_{HIGH}	Clock high period			4.0		μs
t_{SU-SDA}	Start condition setup time			4.7		μs
t_{HD-DAT}	Data input hold time			0		μs
t_{SU-DAT}	Date input setup time			250		ns
t_R	SDA & SCL rise time					μs
t_F	SDA & SCL Full Time					μs
t_{SU-STO}	Stop condition setup time			4.7		μs
t_{DH}	DATA out time			300		ns
V_{IL}	Input low voltage				1	V
V_{IH}	Input high voltage		3			V

Figure 3. AM test circuit

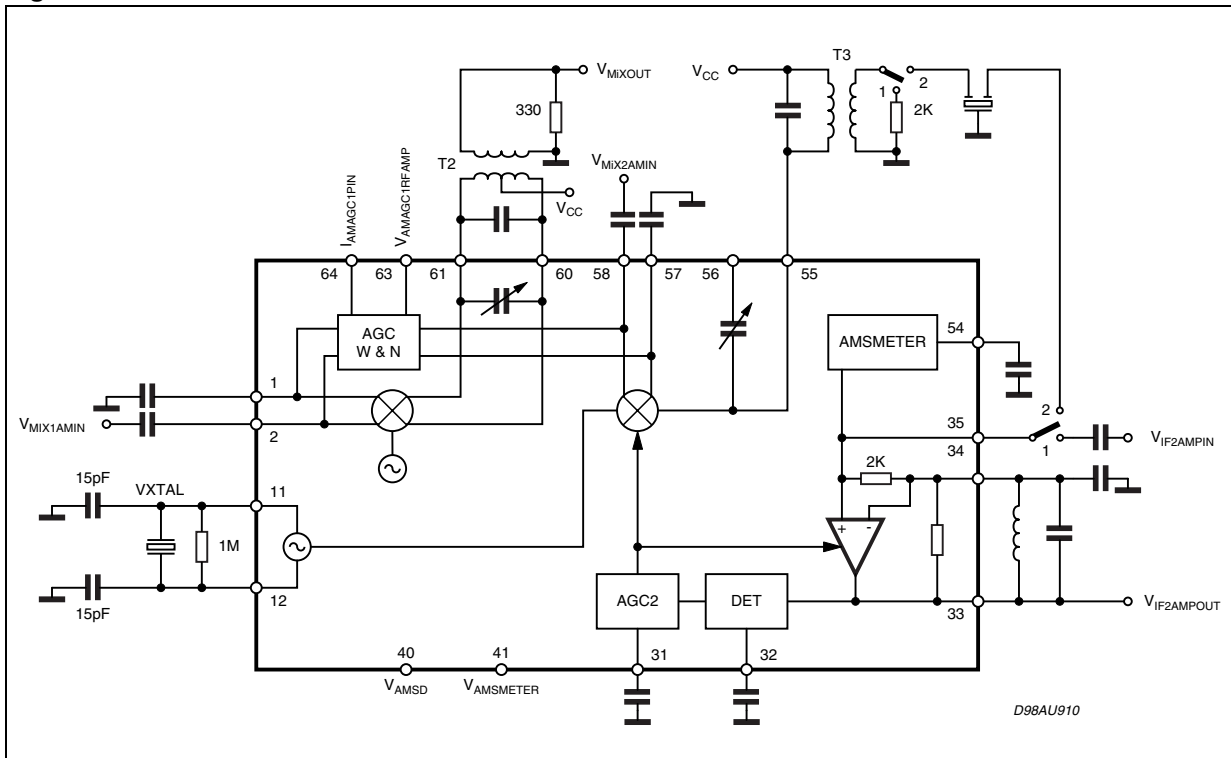
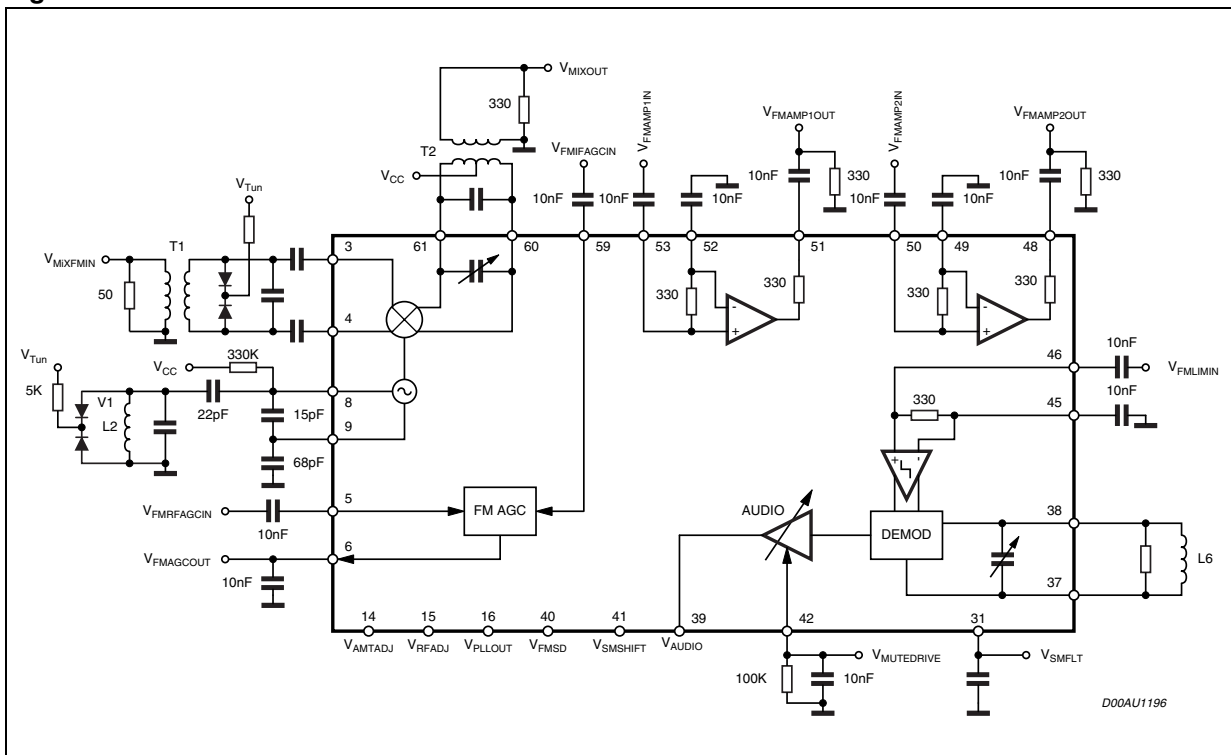


Figure 4. FM test circuit



4 Function description

4.1 FM section

Featuring a single conversion configuration, it comprises a multi-stage IF limiter whose gain is I²C controlled and a quadrature demodulator with detuning and adjacent channel detectors. Signal meter and stop station functions are also supported

4.2 AM section

AM signal is converted by means of UP-DOWN configuration (IF1 = 10.7 MHz, IF2 = 450 kHz) and MW/LW bands are covered.

4.3 PLL section

Three operating modes are available:

Table 8. Operating modes

PM0	PM1	Operating mode
0	0	Standby
1	0	AM
0	1	not used
1	1	FM

They are user programmable with the mode PM registers.

4.4 Standby mode

It stops all functions. This allows low current consumption without loss of information in all registers. The pin LP-OUT is forced to 0V in power on. All data registers are set to FE (11111110). The oscillator does not run in stand-by mode.

4.5 FM and AM operation

The FM or AM signal applies to a 32/33 prescaler, which is controlled by a 5 bit counter (A). The 5 bit register (PC0 to PC4) controls this divider.

The output of the prescaler connects to a 11 bit divider (B). The 11 bit register (PC5 to PC15) controls the divider 'B'.

4.5.1 Three state phase comparator

The phase comparator generates a phase error signal according to phase difference between fSYN and fREF. This phase error signal drives the charge pump current generator.

4.5.2 Charge pump current generator

This stage generates signed pulses of current. The phase error signal decides the duration and polarity of those pulses. The current absolute values are programmable by A0, A1, A2 registers for high current and B0, B1 registers for low current.

4.5.3 Low noise CMOS op-amp

An internal voltage divider at pin VREF connects the positive input of the low noise Op-Amp. The charge pump output connects the negative input. This internal amplifier in cooperation with external components can provide an active filter. The negative input is switchable to three input pins (LPIN 1, LPIN 2 and LPIN 3), to increase the flexibility in application. This feature allows two separate active filters for different applications. A logical "1" in the LPIN 1/2 register activates pin LPIN 1, otherwise pin LPIN 2 is active. While the high current mode is activated LPIN 3 is switched on.

4.5.4 Inlock detector

The charge pump is switched in low current mode as the truth table and the related figure shows.

Table 9. Truth table

Curr. high	Lock ENA	Lock (by inlock detector)	Charge pump current
0	X	X	low current
1	1	1	low current
1	1	0	high current
1	0	1	high current
1	0	0	high current

The charge pump is forced in low current mode when a phase difference of 10-40 μ s is reached.

A phase difference larger than the programmed values will switch the charge pump immediately in the high current mode.

Few programmable delays are available for inlock detection.

4.6 IF counter system for AM/FM

The IF counter mode is controlled by IFCM register:

Table 10. IF counter mode

IFCM1	IFCM0	Function
0	0	Not used
0	1	FM mode
1	0	AM mode
1	1	Not used

A sample timer to generate the gate signal for the main counter is built with a 14 bit programmable counter to have the possibility to use any frequency. In FM mode a 6.25 KHz, in AM mode a 1KHz signal is generated. This counter is followed by an asynchronous divider to generate several sampling times.

Table 11. Address organization (PLL and IF counter)

Function	Subadd	MSB								LSB	
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
PLL CHARGE PUMP	00H	LPIN1/2	CURRH	B1	B0	A3	A2	A1	A0		
LL COUNTER	01H	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0		
PLL COUNTER	02H	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8		
LL REF COUNTER	03H	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0		
LL REF COUNTER	04H	RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8		
LL LOCK DETECT	05H	LDENA	-	D3	D2	D1	D0	PM1	PM0		
FC REF COUNTER	06H	IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0		
FC REF COUNTER	07H	IFCM1	IFCM0	IRC13	IRC12	IRC11	IRC10	IRC9	IRC8		
FC CONTROL	08H	IFENA	-	-	-	-	EW2	EW1	EW0		
C CONTROL	09H	IFS2	IFS1	IFS0	CF4	CF3	CF2	CF1	CF0		

4.7 Intermediate frequency main counter (IFMC)

This counter is a 13-21 bit synchronous autoreload down-counter. Four bits are programmable to have the possibility for an adjust to the frequency of the IF filter. The counter length is automatically adjusted to the chosen sampling time and the counter mode. At the start the counter will be loaded with a defined value which is an equivalent to the divider value ($t_{\text{sample}} \cdot f_{\text{IF}}$). If a correct frequency is applied to the IF counter frequency inputs IF-AM and IF-FM, at the end of the sampling time the main counter is changing its state from 0 to 1FFFFFFH. This is detected by a control logic. The frequency range inside which a successful count results is detected is adjustable setting bits EW 0, 1, 2.

4.8 Up-down counter filter

The information coming from the IF main counter control logic is shifted into a 5 bit up down counter circuit clocked by the sampling time signal. At the start (rising edge of the IFENA signal) the counter is set to 10H and the SSTOP signal is forced to "1". Only when the counter reaches the value 10H - step, SSTOP goes to "0". SSTOP will be "1" again, if the counter reaches the value 10h + step.

Figure 5. Charge pump logic

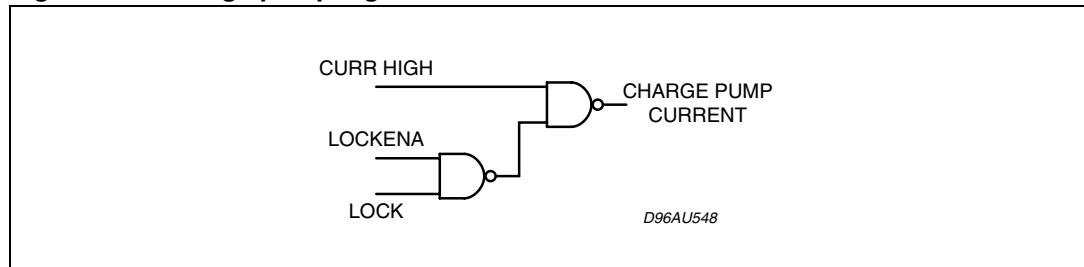
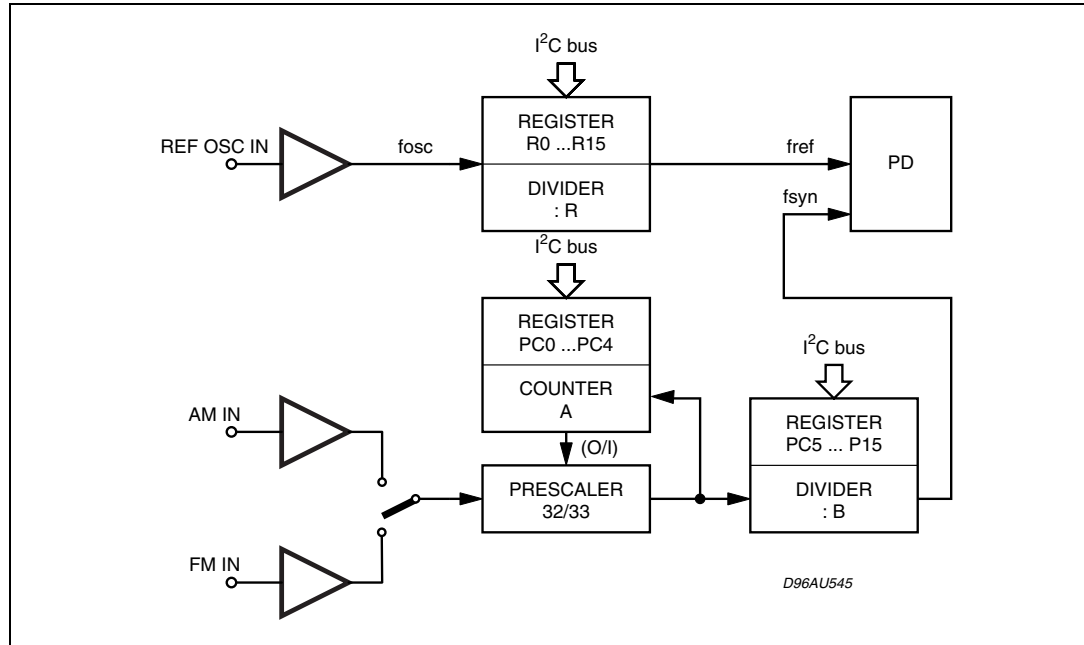


Figure 6. FM and AM operation (swallow mode)



$$t_{tim} = (IFRC + 1) / f_{osc}$$

$$t_{cnt} = (CF + 1697) / f_{IF \text{ FM mode}}$$

$$t_{cnt} = (CF + 44) / f_{IF \text{ AM mode}}$$

Counter result succeeded:

$$t_{tim} > t_{cnt} - t_{err} \text{ and}$$

$$t_{tim} > t_{cnt} + t_{err}$$

Counter result failed:

$$t_{tim} < t_{cnt} + t_{err} \text{ or}$$

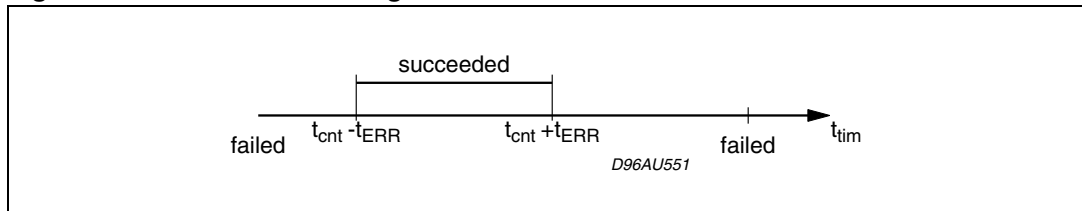
$$t_{tim} > t_{cnt} - t_{err}$$

where:

t_{tim} = IF time cycle time

t_{cnt} = IF counter cycle time

t_{err} = discrimination window (controlled by the EW registers)

Figure 7. Counter result diagram

The precision of the measurements is adjustable by controlling the discrimination window. This is adjustable by programming the control registers EW0...EW2.

The measurement time per cycle is adjustable by setting the register IFS0 - IFS2.

The center frequency of the discrimination window is adjustable by the control register "CF0" to "CF4". The available values are reported in databyte specification

5 I²C bus interface

5.1 General description

The TDA7421N supports the I²C bus protocol. This protocol defines the devices sending data into the bus as transmitter and the receiving device as the receiver.

The device that controls the transfer is a master and the device being controlled is the slave. The master will always initiates data transfer and provide the clock to transmit or receive operations.

5.2 Data transition

Data transition on the SDA line must only occur when the clock SCL is low. SDA transitions while SCL is high will be interpreted as START or STOP condition.

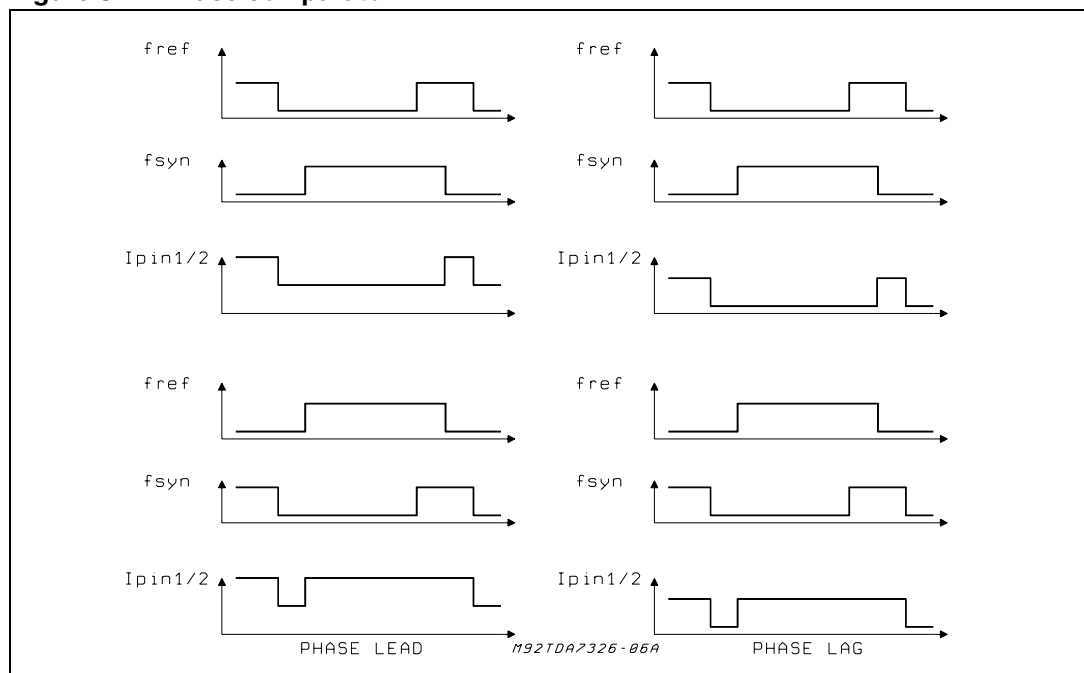
Start condition

A start condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus. The TDA7421N continuously monitors the SDA and SCL lines for a valid START and will not response to any command if this condition has not been met.

5.3 Stop condition

A STOP condition is defined by a LOW to HIGH transition of the SDA while the SCL line is at a stable HIGH level. This condition terminate the communication between the devices and force's the bus interface of the TDA7421N into the initial condition.

Figure 8. Phase comparator



5.4 Acknowledge

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will pull the SDA line to LOW level to indicate it has received the eight bits of data correctly.

5.5 Data transfer

During data transfer the TDA7421N samples the SDA line on the leading edge of the SCL clock, Therefore, for proper device operation the SDA line must be stable during the SCL LOW to HIGH transition.

5.6 Device addressing

To start the communication between two devices, the bus master must initiate a start instruction sequence, followed by an eight bit word corresponding to the address of the device it is addressing. The most significant 6 bits of the slave address identify the device type.

The TDA7421N device code is fixed as "110001".

The next significant bit is used either to address the tuner section (1) or the PLL section (0) of the chip.

Following a START condition the master sends slave address word; the TDA7421N will "acknowledge" after this first transmission and wait for a second word (the word address field). This 8 bit address field provides an access to any of the 8 internal addresses. Upon receipt of the word address the TDA7421N slave device will respond with an "acknowledge".

At this time, all the following words transmits to the TDA7421N will be considered as data. The internal address will be automatically incremented. After each word receipt the TDA7421N will answer with an "acknowledge".

The interface protocol comprises:

- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- a start condition (S)
- a chip address byte

Table 12. Control register function

REGISTER NAME	FUNCTION
PC	Programmable counter for VCO frequency
RC	Reference counter PLL
IRC	Reference counter IF
IFCM	IF Counter Mode
EW	Frequency error window
IFENA	Enable IF counter

Table 12. Control register function (continued)

REGISTER NAME	FUNCTION
CF	Center frequency IF counter
IFS	Sampling time IF counter
PM	Standby, FM, AM, AM swallow mode (PLL mode)
D	Programmable delay for lock detector
LPIN1/2	Loop filter input select
A	Charge pump high current
B	Charge pump low current
LDENA	Lock detector enable
CURRH	Set current high

Figure 9. IF counter block diagram

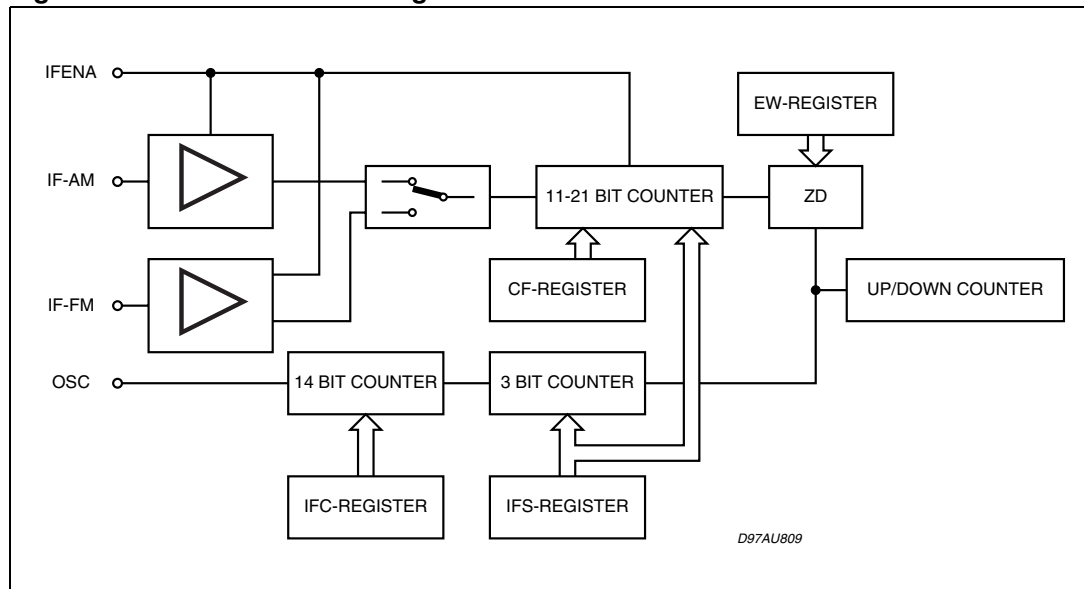
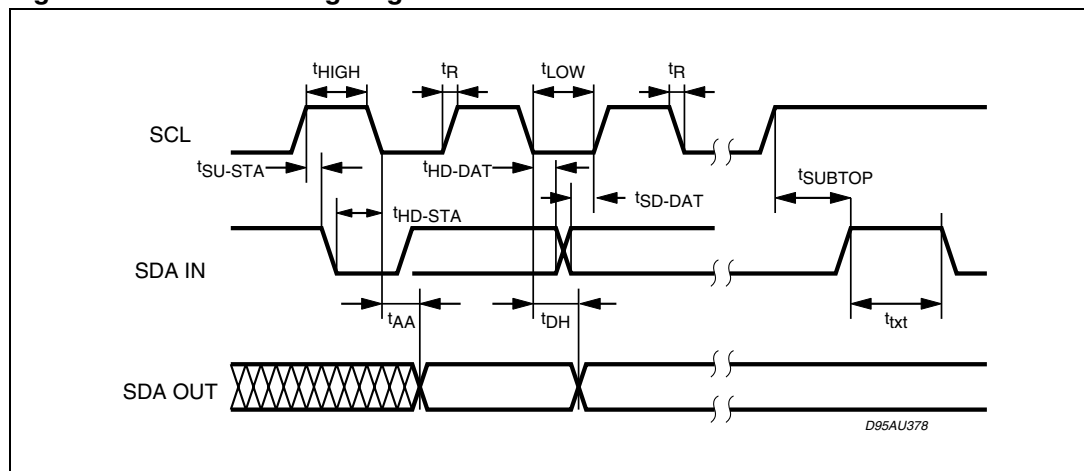


Figure 10. I²C bus timing diagram



5.7 Frame examples

Figure 11. Example for addressing the PLL part

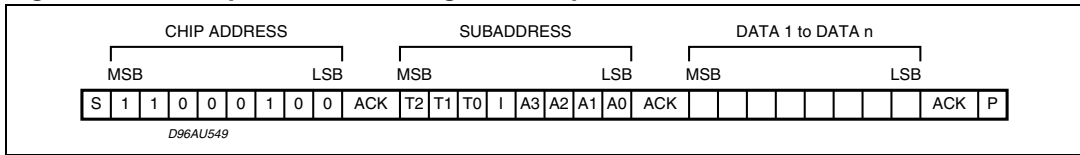
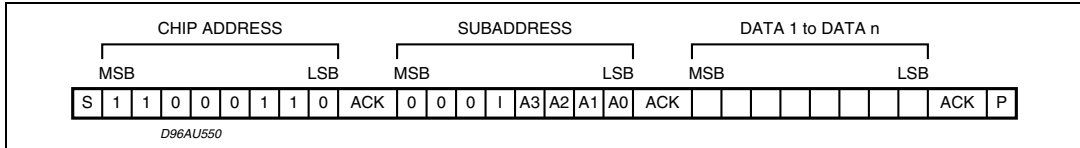


Figure 12. Example for addressing the tuner part:



- ACK: Acknowledge
- S: Start
- P: Stop
- I: Page mode
- T2, T1, T0: Used in test mode (for PLL only, for TUNER addressing they must be 0)
- A3, A2, A1, A0: Mode selection

Table 13. Tuner subaddress

MSB			LSB				Function	
X	X	X	I	A3	A2	A1		A0
				0	0	0	0	Status
				0	0	0	1	FM stop station/FM IF AGC
				0	0	1	0	FM smeter slider/ AM IF2 AMP
				0	0	1	1	AM AGC1/AM stop station
				0	1	0	0	IFT1/IFT2
				0	1	0	1	Front-end adjustment
				0	1	1	0	FM demod. adjustment
				0	1	1	1	FM audio mute gain/FM IF buffers/FM soft mute
				1	0	0	0	FM hole detector/FM detuning
				1	0	0	1	Tuner testing
			0					Page mode disabled
			1					Page mode enabled
0	0	0						must be "0"

Table 14. PLL subaddress

MSB				LSB				Function
T3 ⁽¹⁾	T2	T1	I	A3	A2	A1	A0	
				0	0	0	0	Charge pump control
				0	0	0	1	PLL counter 1 (LSB)
				0	0	1	0	PLL counter 2 (MSB)
				0	0	1	1	PLL reference counter 1 (LSB)
				0	1	0	0	PLL reference counter 2 (MSB)
				0	1	0	1	PLL lock detector control and PLL mode select
				0	1	1	0	IFC reference counter 1 (LSB)
				0	1	1	1	IFC reference counter 2 (MSB) and IFC mode select
				1	0	0	0	IF counter control 1
				1	0	0	1	IF counter control 2
			0					Page mode disabled
			1					Page mode enabled

1. T1, T2, T3 are used for testing the PLL, in application mode they have to be "0".

6 Data byte specification

6.1 PLL data byte specification

Table 15. Charge pump control

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
				0	0	0	0	High current = 0 mA
				0	0	0	1	High current = 0.5 mA
				0	0	1	0	High current = 1.0 mA
				0	0	1	1	High current = 1.5 mA
				0	1	0	0	High current = 2.0 mA
				0	1	0	1	High current = 2.5 mA
				0	1	1	0	High current = 3.0 mA
				0	1	1	1	High current = 3.5 mA
				1	0	0	1	High current = 4.5 mA
				1	0	1	0	High current = 5.0 mA
				1	0	1	1	High current = 5.5 mA
				1	1	0	0	High current = 6.0 mA
				1	1	0	1	High current = 6.5 mA
				1	1	1	0	High current = 7.0 mA
				1	1	1	1	High current = 7.5 mA
		0	0					Low current = 0 μ A
		0	1					Low current = 15 μ A
		1	0					Low current = 100 μ A
		1	1					Low current = 115 μ A
	0							Select low Current
	1							Select high Current
0								Select loop filter 1
1								Select loop filter 2
LPIN1/2	CURRH	B1	B0	A3	A2	A1	A0	Bit name Subaddress = 00H

Table 16. PLL counter 1 (LSB)

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	LSB = 0	
0	0	0	0	0	0	0	1	LSB = 1	
0	0	0	0	0	0	1	0	LSB = 2	
all combinations allowed									
1	1	1	1	1	1	0	0	LSB = 252	
1	1	1	1	1	1	0	1	LSB = 253	
1	1	1	1	1	1	1	0	LSB = 254	
1	1	1	1	1	1	1	1	LSB = 255	
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	Bit name Subaddress = 01H	

Table 17. PLL counter 2 (MSB)

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	MSB = 0	
0	0	0	0	0	0	0	1	MSB = 256	
0	0	0	0	0	0	1	0	MSB = 512	
all combinations allowed									
1	1	1	1	1	1	0	0	MSB = 64768	
1	1	1	1	1	1	0	1	MSB = 65024	
1	1	1	1	1	1	1	0	MSB = 65280	
1	1	1	1	1	1	1	1	MSB = 65536	
PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	Bit name Subaddress = 02H	

Swallow mode: $fvco/fsyn = LSB + MSB + 32$

Table 18. PLL reference counter 1 (LSB)

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	LSB = 0	
0	0	0	0	0	0	0	1	LSB = 1	
0	0	0	0	0	0	1	0	LSB = 2	
all combinations allowed									
1	1	1	1	1	1	0	0	LSB = 252	
1	1	1	1	1	1	0	1	LSB = 253	
1	1	1	1	1	1	1	0	LSB = 254	
1	1	1	1	1	1	1	1	LSB = 255	
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	Bit name Subaddress = 03H	

Table 19. PLL reference counter 2 (MSB)

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	MSB = 0	
0	0	0	0	0	0	0	1	MSB = 256	
0	0	0	0	0	0	1	0	MSB = 512	
all combinations allowed									
1	1	1	1	1	1	0	0	MSB = 64768	
1	1	1	1	1	1	0	1	MSB = 65024	
1	1	1	1	1	1	1	0	MSB = 65280	
1	1	1	1	1	1	1	1	MSB = 65536	
RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8	Bit name Subaddress = 04H	

$$f_{\text{OSC}}/f_{\text{REF}} = \text{LSB} + \text{MSB} + 1$$

Table 20. Lock detector and PLL mode control

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
						0	0	PLL standby mode	
						0	1	PLL AM	
						1	0	not used	
						1	1	PLL FM mode	
				0	0			PD phase difference threshold 10ns	
				0	1			PD phase difference threshold 20ns	
				1	0			PD phase difference threshold 30ns	
				1	1			PD phase difference threshold 40ns	
		0	0					Not used in application mode	
		0	1					Activation delay = $4 \cdot f_{\text{ref}}$	
		1	0					Activation delay = $6 \cdot f_{\text{ref}}$	
		1	1					Activation delay = $8 \cdot f_{\text{ref}}$	
0								No lock detector controlled charge pump	
1								Lock detector controlled charge pump	
LDENA		D3	D2	D1	D0	PM1	PM0	Bit name : Subaddress = 05H	

Table 21. IF counter reference control 1 (LSB)

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	LSB = 0	
0	0	0	0	0	0	0	1	LSB = 1	
0	0	0	0	0	0	1	0	LSB = 2	
all combinations allowed									
1	1	1	1	1	1	0	0	LSB = 252	
1	1	1	1	1	1	0	1	LSB = 253	
1	1	1	1	1	1	1	0	LSB = 254	
1	1	1	1	1	1	1	1	LSB = 255	
IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0	Bit name Subaddress = 06H	

Table 22. IF counter reference control 2 (MSB) and IF counter mode select

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	MSB = 0	
0	0	0	0	0	0	0	1	MSB = 256	
0	0	0	0	0	0	1	0	MSB = 512	
all combinations allowed									
		1	1	1	1	0	1	MSB = 15616	
		1	1	1	1	1	0	MSB = 15872	
		1	1	1	1	1	1	MSB = 16128	
0	0							NOT USED IN APPLICATION MODE	
0	1							IF counter FM mode	
1	0							IF counter AM mode	
1	1							not used	
IFCM1	IFCM0	IRC13	IRC12	IRC11	IRC10	IRC9	IRC8	Bit name Subaddress = 07H	

$$fosc/ftim = LSB + MSB + 1$$

Table 23. IF counter control 1

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
					0	0	0	don't use	
					0	0	1	don't use	
					0	1	0	don't use	
					0	1	1	EW delta f = ± 6.25 kHz (FM); ± 1 kHz (AM)	
					1	0	0	EW delta f = ± 12.5 kHz (FM); ± 2 kHz (AM)	
					1	0	1	EW delta f = ± 25 kHz (FM); ± 4 kHz (AM)	
					1	1	0	EW delta f = ± 50 kHz (FM); ± 8 kHz (AM)	
					1	1	1	EW delta f = ± 100 kHz (FM); ± 16 kHz (AM)	
0								IF counter disabled / standby	
1								IF counter enabled	
IFENA					EW2	EW1	EW0	Bit name Subaddress = 08H	

Table 24. IF counter control 2

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
			0	0	0	0	0	fcenter = 10.60000 MHz (FM) 448 kHz (AM)	
			0	0	0	0	1	fcenter = 10.60625 MHz (FM) 449 kHz (AM)	
			0	0	0	1	0	fcenter = 10.61250 MHz (FM) 450 kHz (AM)	
			0	0	0	1	1	fcenter = 10.61875 MHz (FM) 451 kHz (AM)	
			0	0	1	0	0	fcenter = 10.62500 MHz (FM) 452 kHz (AM)	
			0	0	1	0	1	fcenter = 10.63125 MHz (FM) 453 kHz (AM)	
			0	0	1	1	0	fcenter = 10.63750 MHz (FM) 454 kHz (AM)	
			0	0	1	1	1	fcenter = 10.64375 MHz (FM) 455 kHz (AM)	
			0	1	0	0	0	fcenter = 10.65000 MHz (FM) 456 kHz (AM)	
			0	1	0	0	1	fcenter = 10.65625 MHz (FM) 457 kHz (AM)	
			0	1	0	1	0	fcenter = 10.66250 MHz (FM) 458 kHz (AM)	
			0	1	0	1	1	fcenter = 10.66875 MHz (FM) 459 kHz (AM)	
			0	1	1	0	0	fcenter = 10.67500 MHz (FM) 460 kHz (AM)	
			0	1	1	0	1	fcenter = 10.68125 MHz (FM) 461 kHz (AM)	
			0	1	1	1	0	fcenter = 10.68750 MHz (FM) 462 kHz (AM)	
			0	1	1	1	1	fcenter = 10.69375 MHz (FM) 463 kHz (AM)	
			1	0	0	0	0	fcenter = 10.70000 MHz (FM) 464 kHz (AM)	
			1	0	0	0	1	fcenter = 10.70625 MHz (FM) 465 kHz (AM)	
			1	0	0	1	0	fcenter = 10.71250 MHz (FM) 466 kHz (AM)	

Table 24. IF counter control 2 (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
			1	0	0	1	1	fcenter = 10.71875 MHz (FM) 467 kHz (AM)
			1	0	1	0	0	fcenter = 10.72500 MHz (FM) 468 kHz (AM)
			1	0	1	0	1	fcenter = 10.73125 MHz (FM) 469 kHz (AM)
			1	0	1	1	0	fcenter = 10.73750 MHz (FM) 470 kHz (AM)
			1	0	1	1	1	fcenter = 10.74375 MHz (FM) 471 kHz (AM)
			1	1	0	0	0	fcenter = 10.75000 MHz (FM) 472 kHz (AM)
			1	1	0	0	1	fcenter = 10.75625 MHz (FM) 473 kHz (AM)
			1	1	0	1	0	fcenter = 10.76250 MHz (FM) 474 kHz (AM)
			1	1	0	1	1	fcenter = 10.76875 MHz (FM) 475 kHz (AM)
			1	1	1	0	0	fcenter = 10.77500 MHz (FM) 476 kHz (AM)
			1	1	1	0	1	fcenter = 10.78125 MHz (FM) 477 kHz (AM)
			1	1	1	1	0	fcenter = 10.78750 MHz (FM) 478 kHz (AM)
			1	1	1	1	1	fcenter = 10.79375 MHz (FM) 479 kHz (AM)
0	0	0						tsample = 20.48 ms (FM mode); 128 ms (AM; MODE)
0	0	1						tsample = 10.24 ms (FM mode); 64 ms (AM; MODE)
0	1	0						tsample = 5.12 ms (FM mode); 32 ms (AM; MODE)
0	1	1						tsample = 2.56 ms (FM mode); 16 ms (AM; MODE)
1	0	0						tsample = 1.28 ms (FM mode); 8 ms (AM;MODE)
1	0	1						tsample = 640 ms (FM mode); 4 ms (AM;MODE)
1	1	0						tsample = 320 ms (FM mode); 2 ms (AM; MODE)
1	1	1						tsample = 160 ms (FM mode); 1 ms (AM; MODE)
IFS2	IFS1	IFS0	CF4	CF3	CF2	CF1	CF0	bit name Subaddress = 09H

6.2 Tuner data byte specification

Table 25. Address organization (Tuner AM/FM)

Function	Subad	MSB							LSB	
		B7	B6	B5	B4	B3	B2	B1	B0	
STATUS	00H	N.U.	FMMUTE	FMADJ	AM STEREO	SEEK	AM/FM/STBY	AM/FM/STBY	AM/FM/STBY	
FM STOP STATION/ FM IF AGC	01H	FAG2	FAG1	FAG0	FSS4	FSS3	FSS2	FSS1	FSS0	
FM SMETER SLIDER/ AM IF2 AMP	02H	FSL4	FSL3	FSL2	FSL1	FSL0	IF2A1	IF2A0	N.U.	
AM AGC1/AM STOP STATION	03H	ASS3	ASS2	ASS1	ASS0	AAGN1	AAGN0	AAGW1	AAGW0	
IFT1/IFT2	04H	T2A3	T2A2	T2A1	T2A0	T1A3	T1A2	T1A1	T1A0	
FRONT-END ADJUSTMENT	05H	ANA3	ANA2	ANA1	ANA0	RFA3	RFA2	RFA1	RFA0	
FM DEMOD ADJUSTMENT	06H	N.U.	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0	
FM AUDIO MUTE GAIN/FM IF BUFFERS/FM SOFT MUTE	07H	FSM3	FSM2	FSM1	FSM0	FFBL1	FBL0	AUM1	AUM0	
FM HOLE DETECTOR/FM DETUNING	08H	BWM2	BWM1	BWM0	HDM4	HDM3	HDM2	HDM1	HDM0	
TUNER TESTING	09H	PLLTEST	T2	T1	T0	SDDIS	BWDIS	HDDID	SMDIS	

Table 26. Status (subaddress 00H)

MSB							LSB		Function
S6	S5	S4	S3	S2	S1	S0			
FM MUTE	FM ADJ	AM STEREO	SEEK	AM/FM/Standby	AM/FM/Standby	AM/FM/Standby			
				0	0	0	Standby		
				0	0	1	FM on		
				0	1	0	AM on (/6)		
				1	1	0	AM on (/10)		
				1	0	0	AM on (/8)		
			0				RECEPTION		
			1				SEEK		
		0		AM	AM	AM	AM IFC Out		
		1		AM	AM	AM	AM Stereo OUT		

Table 26. Status (subaddress 00H) (continued)

MSB							LSB	Function
S6	S5	S4	S3	S2	S1	S0		
FM MUTE	FM ADJ	AM STEREO	SEEK	AM/FM/ Standby	AM/FM/ Standby	AM/FM/ Standby		
0	1			FM	FM	FM	FM on for demodulator adjustment, demod. on	
1	1			FM	FM	FM	FM on for demodulator adjustment, demod. muted	

Table 27. FM stop station / FM IF AGC (subaddress 01H)

MSB							LSB	Function
FAG2	FAG1	FAG0	FSS4	FSS3	FSS2	FSS1	FSS0	
FM IF AGC MSB	FM IF AGC	FM IF AGC LSB	FM stop station MSB	FM stop station	FM stop station	FM stop station	FM stop station LSB	
								FM stop station threshold
			0	0	0	0	0	Maximum sensitivity
			X	X	X	X	X	
			1	1	1	1	1	Minimum sensitivity
all combinations allowed								
								FM IF AGC threshold
0	0	0						Maximum sensitivity
X	X	X						
1	1	0						Minimum sensitivity
1	1	1						Keyed AGC disabled
all combinations allowed								

Table 28. FM smeter slider\IF2 amplifier (subaddress 02H)

MSB							LSB	Function
FSL4	FSL3	FSL2	FSL1	FSL0	IF2A1	IF2A0		
FM smeter slider MSB	FM smeter slider	FM smeter slider	FM smeter slider	FM smeter slider LSB	AM if 2Amp MSB	AM if 2Amp LSB		
								FM smeter sliding (mV)
0	0	0	0	0				0

Table 28. FM smeter slider\IF2 amplifier (subaddress 02H) (continued)

MSB					LSB			Function
FSL4	FSL3	FSL2	FSL1	FSL0	IF2A1	IF2A0		
FM smeter slider MSB	FM smeter slider	FM smeter slider	FM smeter slider	FM smeter slider LSB	AM if 2Amp MSB	AM if 2Amp LSB		
0	0	0	0	1			48	
X	X	X	X	X				
1	1	1	1	1			1500	
all combinations allowed								
							IF2 amplifier gain	
					0	0	50dB	
					0	1	53dB	
					1	0	56dB	
					1	1	59dB	

Table 29. AM stop station / AM AGC1 (subaddress 03H)

MSB					LSB			Function
ASS3	ASS2	ASS1	ASS0	AAGN1	AAGN0	AAGW1	AAGW0	
AM stop station MSB	AM stop station	AM stop station	AM stop station LSB	AM NAGC MSB	AM NAGC LSB	AM WAGC MSB	AM WAGC LSB	
							0 0	Minimum sensitivity
							X X	
							1 1	Maximum sensitivity
					all comb. allowed			
								AM NAGC threshold
					0	0		Minimum sensitivity
					X	X		
					1	1		Maximum sensitivity
					all comb. allowed			
								AM stop station threshold
0	0	0	0					Maximum sensitivity
X	X	X	X					
1	1	1	1					Minimum sensitivity
all combinations allowed								

Table 30. IFT1/IFT2 (subaddress 04H)

MSB				LSB				Function
T2A3	T2A2	T2A1	T2A0	T1A3	T1A2	T1A1	T1A0	
IF T2 adjust MSB	IF T2 adjust	IF T2 adjust	IF T2 adjust LSB	IF T1 adjust MSB	IF T1 adjust	IF T1 adjust	IF T1 adjust LSB	
								Adjustment capacitor
				0	0	0	0	15Cift1
				0	1	1	1	8Cift1
				1	0	1	0	4Cift1
				1	1	0	1	2Cift1
				1	1	1	0	Cift2 (= 380 pF)
				1	1	1	1	0
				all combinations allowed				
0	0	0	0					0
0	0	0	1					Cift1 (= 1.57 pF)
0	0	1	0					2Cift2
0	1	0	0					4Cift2
1	0	0	0					8Cift2
1	1	1	1					15Cift2
all combinations allowed								

Table 31. Front-end adjustment (subaddress 05H)

MSB				LSB				Function
ANA3	ANA2	ANA1	ANA0	RFA3	RFA2	RFA1	RFA0	
ANT adjustm ±	ANT adjustm MSB	ANT adjustm	ANT adjustm LSB	RF adjustm ±	RF adjustm MSB	RF adjustm	RF adjustm LSB	
								Voffset RF varicap / VPLL
				X	0	0	0	0
				0	0	0	1	-3.6 %
				0	0	1	0	-7.2 %
				0	1	0	0	-14.3 %
				0	1	1	1	-25 %
				1	0	0	1	3.6 %
				1	0	1	0	7.2 %
				1	1	0	0	14.3 %

Table 31. Front-end adjustment (subaddress 05H) (continued)

MSB				LSB				Function
ANA3	ANA2	ANA1	ANA0	RFA3	RFA2	RFA1	RFA0	
ANT adjustm ±	ANT adjustm MSB	ANT adjustm	ANT adjustm LSB	RF adjustm ±	RF adjustm MSB	RF adjustm	RF adjustm LSB	
				1	1	1	1	25 %
				all combinations allowed				
								Voffset antenna varicap / VPLL
X	0	0	0					0
0	0	0	1					-3.6 %
0	0	1	0					-7.2 %
0	1	0	0					-14.3 %
0	1	1	1					-25 %
1	0	0	1					3.6 %
1	0	1	0					7.2 %
1	1	0	0					14.3 %
1	1	1	1					25 %
all combinations allowed								

Table 32. FM demodulator adjustment (subaddress 06H)

MSB				LSB				Function
	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0	
	demadj MSB	demadj	demadj	demadj	demadj	demadj	demadj LSB	
								Adjustment capacitor
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	$C_{\text{demod}} (= 50\text{fF})$
	0	0	0	0	0	1	0	$2C_{\text{demod}}$
	0	0	0	0	1	0	0	$4C_{\text{demod}}$
	0	0	0	1	0	0	0	$8C_{\text{demod}}$
	0	0	1	0	0	0	0	$16C_{\text{demod}}$
	0	1	0	0	0	0	0	$32C_{\text{demod}}$
	1	0	0	0	0	0	0	$64C_{\text{demod}}$
	1	1	1	1	1	1	1	$127C_{\text{demod}}$
all combinations allowed								

Table 33. FM soft mute / FM IF amplifier/fm audio mute gain (subaddress 07H)

MSB				LSB				Function
FSM3	FSM2	FSM1	FSM0	FBL1	FBL0	AUM1	AUM0	
FM softmute MSB	FM softmute	FM softmute	FM softmute LSB	buff 2 gain	buff 2 gain	Mute Depth MSB	Mute Depth LSB	
								FM soft mute threshold
0	0	0	0					Maximum sensitivity
X	X	X	X					
1	1	1	1					Minimum sensitivity
all combinations allowed								
								Audio max mute attenuation
						0	0	-5
						0	1	-7.5
						1	0	-10
						1	1	-12.5
						all comb. allowed		
								Buffer 2 Gain (dB)
				0	0			10
				0	1			6
				1	0			8
				all else not allowed				

Table 34. FM hole detector / FM detuning detector (subaddress 08H)

MSB				LSB				Function
BWM2	BWM1	BWM0	HDM4	HDM3	HDM2	HDM1	HDM0	
BW Slope 30 kHz	BW Slope 15 kHz	BW Slope 10 kHz	Hole det MSB	Hole det	Hole det	Hole det	Hole det LSB	
								Muting sensitivity (hole depth)
			0	0	0	0	0	Minimum (deep hole)
			X	X	X	X	X	
			1	1	1	1	1	Maximum (shallow hole)
			all combinations allowed					
RECEPTION								Detuning mute range (kHz)
0	0	1						10
0	1	0						15

Table 34. FM hole detector / FM detuning detector (subaddress 08H) (continued)

MSB			LSB					Function
BWM2	BWM1	BWM0	HDM4	HDM3	HDM2	HDM1	HDM0	
BW Slope 30 kHz	BW Slope 15 kHz	BW Slope 10 kHz	Hole det MSB	Hole det	Hole det	Hole det	Hole det LSB	
1	0	0						30
all else not allowed								
SEEK								Clamping window
0	0	X						Not allowed
0	1	0						Faster Clamping Window (± 1 kHz over Threshold)
X	X	X						
1	1	1						Slower Clamping Window (± 4 kHz over Threshold)
all combinations allowed								

Table 35. Tuner testing

MSB				LSB				Function
PLL test	T2	T1	T0	SDDIS	BWDIS	HDDIS	SMDIS	
Test mode PLL	Test mode MSB	Test mode	Test mode LSB	SD output disable	Bandwidth disable	Hole detector disable	Soft mute disable	
0	0	0	0	0	0	0	0	no test
								Test modes
					1	1	0	Soft Mute Test
					1	0	1	Hole Detector Test
					0	1	1	Bandwidth Test
					1	1	1	Audio Mute and SD Disabled
				all else not allowed				
	0	0	1					AMSSDAC Test
	0	1	0					FMSSDAC Test
	0	1	1					FMSMDAC Test
	1	0	0					FMHDDAC Test
	1	1	0					FMIFAGCDAC Test
all else not allowed								
1								PLL Test

7 Component description

Table 36. Component description

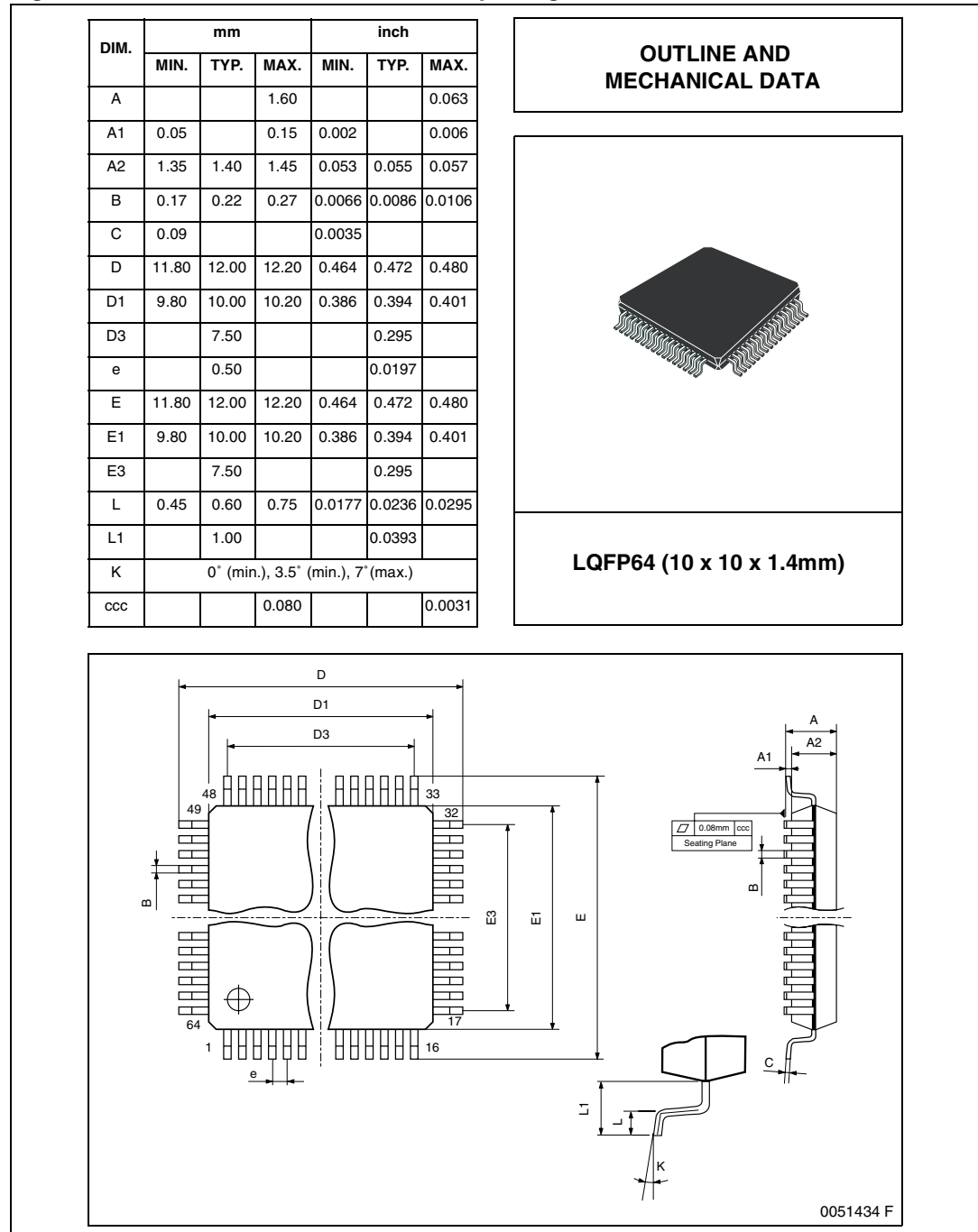
Component	Description
CF1	Ceramic filter 10.7 MHz, 180 kHz BW
CF3-CF4	Ceramic filter 10.7 MHz, 150 kHz BW
CF2	Ceramic filter 450 kHz, 6 kHz BW
T1	FM RF transformer Unloaded Q= 69 3-1= 3 3/4T - 6-4= 3T 0.12f2UEW CTUNING(3-1)= 26.6 pF @ 100 MHz
T2	AM/FM IF1 transformer Unloaded Q= 70 1-3= 12T - 1-5= 6 - 5-3= 6 - 4-6= 2T 0.08f2UEW CINT(1-3) = 51 pF; CEXT(1-3) = 5 pF
T3	AM IF2 transformer Unloaded Q= 40 1-3= 178T - 1-2= 89T - 2-3= 89T - 4-6= 33T 0.05f2UEW CINT(1-3) = 180 pF; CEXT(1-3) = 20 pF
L2	Oscillator coil Unloaded Q= 8 06-4= 2 1/2T 0.12f2UEW CTUNING(6-4)= 36.8 pF @ 100 MHz
L6	Demodulator Coil Unloaded Q= 35 6-4= 27T 0.1f2UEW CINT(4-6)= 47 pF; CEXT(4-6) = 13.5 pF
AM BPF RC	<p>The diagram shows an RC network. It starts with a series resistor of 2.7K. This is followed by a shunt capacitor of 27nF connected to ground. Then, there is a series capacitor of 18nF. Finally, there is a shunt resistor of 100K connected to ground. The component number D984U915 is noted below the diagram.</p>

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

ECOPACK[®] is an ST trademark.

Figure 13. LQFP64 mechanical data and package dimensions



9 Revision history

Table 37. Document revision history

Date	Revision	Changes
24-Aug-2000	1	Initial release.
23-Jan-2009	2	Document reformatted. Document status changed from preliminary data to not for new design. Updated Table 1: Device summary on page 1 . Updated Section 8: Package information on page 45 .

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