DATA SHEET

TDF5242T
Brushless DC motor drive circuit

Preliminary specification
Supersedes data of 1997 Apr 23
File under Integrated Circuits, IC11

1997 Sep 12

Philips
Semiconductors

PHILIPS

FEATURES

- Full-wave commutation without position sensors
- Built-in start-up circuitry
- Six outputs that can drive three external transistor pairs:
  - output current 0.2 A (typ.)
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor
- Brake control input
- Direction control input.

APPLICATIONS

- High-power applications, for instance:
  - high-end hard disk drives
  - automotive applications.

GENERAL DESCRIPTION

The TDF5242T is a bipolar integrated circuit for driving 3-phase brushless DC motors in full-wave mode.
The device functions sensorless, thus saving 3 hall-effect sensors, using the back-EMF (Electro Motive Force) sensing technique to sense the rotor position. It includes 6 pre-drivers able to control external FETs (Field Effect Transistors) or bipolar transistors. It offers brake and direction control. It is ideally suited for high-power applications such as high-end hard disk drives and automotive applications.

QUICK REFERENCE DATA

Measured over full voltage and temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4	–	18	V
V_{VMOT}	input voltage to the output driver stages		3	–	18	V
V_O	driver output voltage	I_O = 100 mA; lower transistor	–	–	0.35	V
		I_O = 100 mA; upper transistor	1.05	–	–	V
I_{LIM}	current limiting	V_{VMOT} = 14.5 V; R_O = 47 Ω	150	200	250	mA

Note

1. An unstabilized supply can be used.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NUMBER	DESCRIPTION	VERSION
TDF5242T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

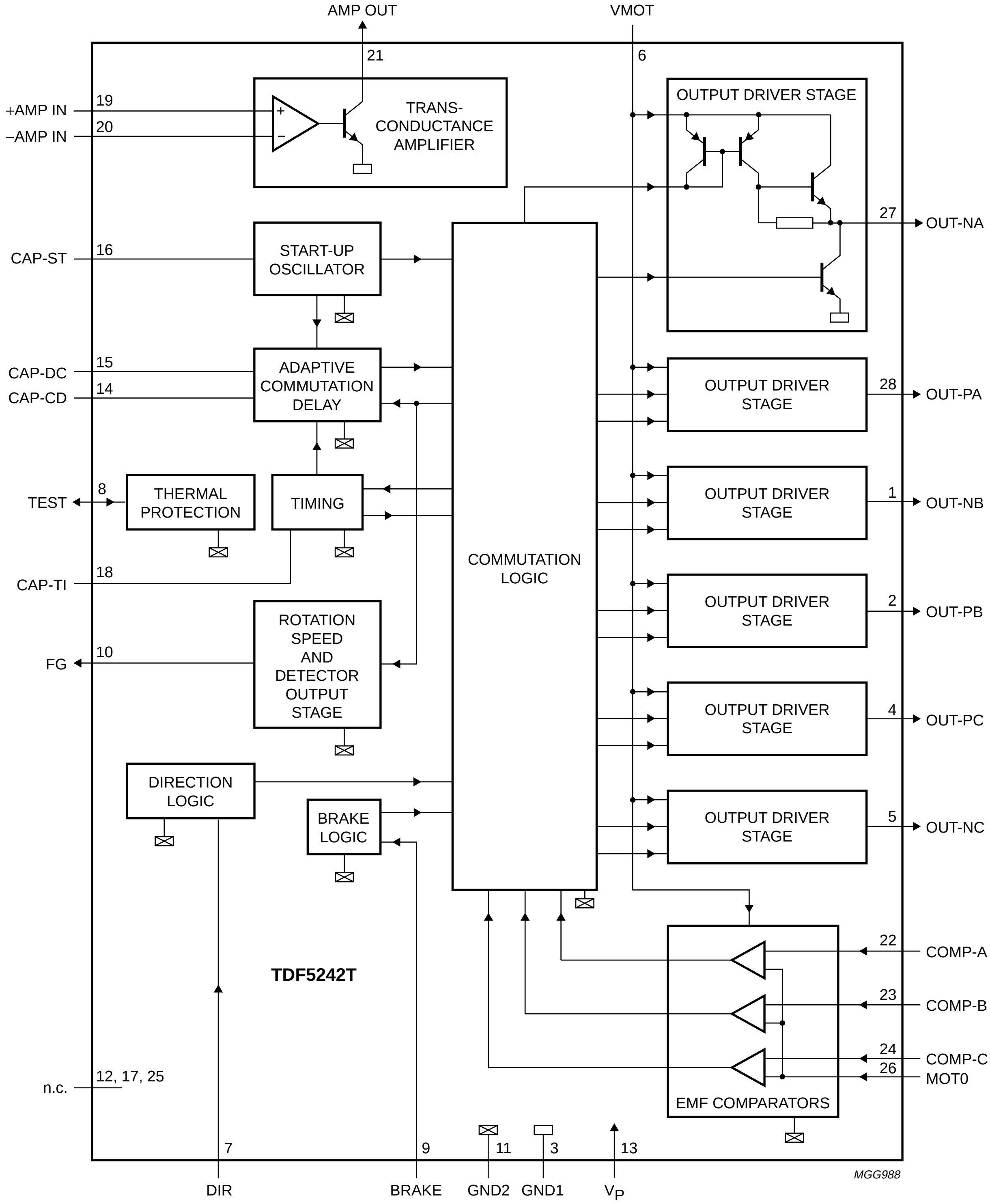


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT-NB	1	driver output B for driving the n-channel power FET or power NPN
OUT-PB	2	driver output B for driving the p-channel power FET or power PNP
GND1	3	ground (0 V) motor supply return for output stages
OUT-PC	4	driver output C for driving the p-channel power FET or power PNP
OUT-NC	5	driver output C for driving the n-channel power FET or power NPN
VMOT	6	input voltage for the output driver stages
DIR	7	direction input command
TEST	8	test input/output
BRAKE	9	brake input
FG	10	frequency generator: output of the rotation speed detector stage
GND2	11	ground supply return for control circuits
n.c.	12	not connected
V_P	13	supply voltage
CAP-CD	14	external capacitor connection for adaptive communication delay timing
CAP-DC	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	16	external capacitor connection for start-up oscillator
n.c.	17	not connected
CAP-TI	18	external capacitor connection for timing
+AMP IN	19	non-inverting input of the transconductance amplifier
–AMP IN	20	inverting input of the transconductance amplifier
AMP OUT	21	transconductance amplifier output (open collector)
COMP-A	22	comparator input corresponding to output A
COMP-B	23	comparator input corresponding to output B
COMP-C	24	comparator input corresponding to output C
n.c.	25	not connected
MOT0	26	input from the star point of the motor coils
OUT-NA	27	driver output A for driving the n-channel power FET or power NPN
OUT-PA	28	driver output A for driving the p-channel power FET or power PNP

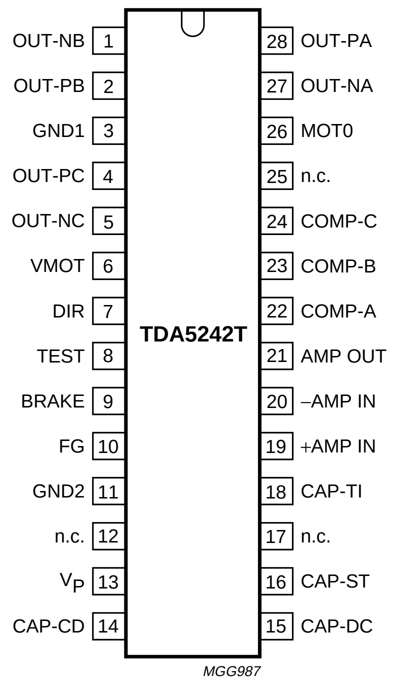


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Introduction

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing (H) and one sinking (L). The third output presents a high impedance (Z) to the motor, which enables measurement of the motor back-EMF (Electro Motive Force) in the corresponding motor coil by the EMF comparator at each output.
The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator. In Table 1, the six possible states of the externally connected output transistors have been depicted and the corresponding output levels on the NA, PA, NB, PB, NC and PC outputs of the TDF5242T.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

The output stages are protected by a current limiting circuit and by thermal protection.

The detected zero-crossings are used to provide speed information. The information has been made available on the FG output pin. This output provides an output signal with a frequency equal to the commutation frequency.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDF5242T also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDF5242T is designed for systems with low current consumption. It uses I^2L logic and adaptive base drive for the output transistors (patented).

Start-up and commutation control

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals.

Table 1 Output states (note 1)

DIR	STATE	MOT1	OUT-NA	OUT-PA	MOT2	OUT-NB	OUT-PB	MOT3	OUT-NC	OUT-PC
H	1	Z	L	H	L	H	H	H	L	L
H	2	H	L	L	L	H	H	Z	L	H
H	3	H	L	L	Z	L	H	L	H	H
H	4	Z	L	H	H	L	L	L	H	H
H	5	L	H	H	H	L	L	Z	L	H
H	6	L	H	H	Z	L	H	H	L	L
L	1	Z	L	H	L	H	H	H	L	L
L	2	L	H	H	Z	L	H	H	L	L
L	3	L	H	H	H	L	L	Z	L	H
L	4	Z	L	H	H	L	L	L	H	H
L	5	H	L	L	Z	L	H	L	H	H
L	6	H	L	L	L	H	H	Z	L	H

Note

1. H = HIGH state; L = LOW state; Z = high-impedance OFF-state.

START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 to 2.2 V and back to 0.05 V. The time to complete one cycle is:

$$t_{start} = (2.15 \times C) \text{ s (with C in } \mu\text{F)} \quad (1)$$

The start oscillator is reset by a commutation pulse and is only active when the system is in the start-up mode.
A pulse from the start oscillator will cause the outputs to change to the next state. If the movement of the motor generates enough EMF, the TDF5242T will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The start capacitor should be chosen to meet this requirement.

The oscillation frequency of the motor is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{\frac{K_t \times I \times p}{J}}}$$

where:

K_t = torque constant (Nm/A)

I = current (A)

p = number of magnetic pole-pairs

J = inertia J ($kg.m^2$).

Example: $J = 72 \times 10^{-6}$ $kg.m^2$, $K = 25 \times 10^{-3}$ Nm/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high, a start frequency of 2 Hz can be chosen or t = 500 ms, thus, according to equation (1): C = 0.5/2.15 = 0.23 μF (choose 220 nF).

ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit the capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period the capacitor is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

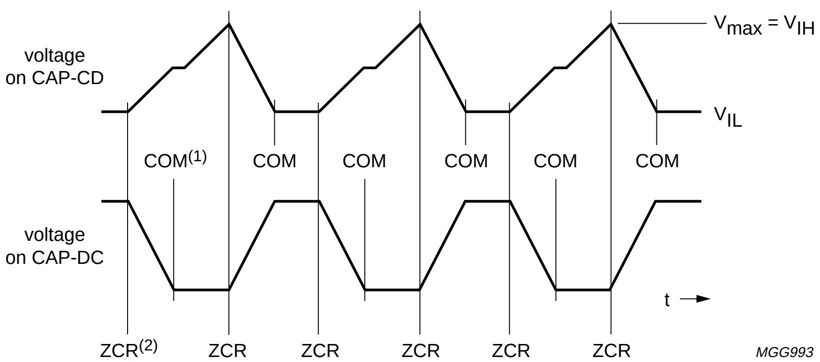
$$C = \frac{8.1 \times 10^{-6}}{f \times 1.3} = \frac{6231}{f_{C1}} \text{ (C in nF)}$$

If the commutation frequency is lower, a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 down to 0.9 V at 16.2 μA; maximum delay = $(0.076 \times C)$ ms (with C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz; so:

$$\text{CAP-CD} = \frac{6231}{400} = 15.6 \text{ (choose 18 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 15.5 μA. The same value can be chosen as for CAP-CD. Figure 3 illustrates typical voltage waveforms.



(1) COM = commutation.
(2) ZCR = zero-crossing.

Fig.3 CAP-CD and CAP-DC typical voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<1 ms). However, if the motor is motionless or rotating in the reverse direction, the time can be longer (>>1 ms).

A watchdog time must be chosen such that it is long enough for a motor without detectable EMF, however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged with a current of 57 μA from 0.2 to 0.3 V. Above this level, it is charged with a current of 5 μA up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V.

To ensure that the internal delays are covered CAP-TI must have a minimum value of 2 nF. For the watchdog function a value for CAP-TI of 10 nF is recommended.

To ensure a good start-up and commutation, care must be taken that no oscillations occur at the trailing edge of the flyback pulse. Snubber networks at the outputs should be critically damped.

Typical voltage waveforms are illustrated by Fig.4.

Miscellaneous functions

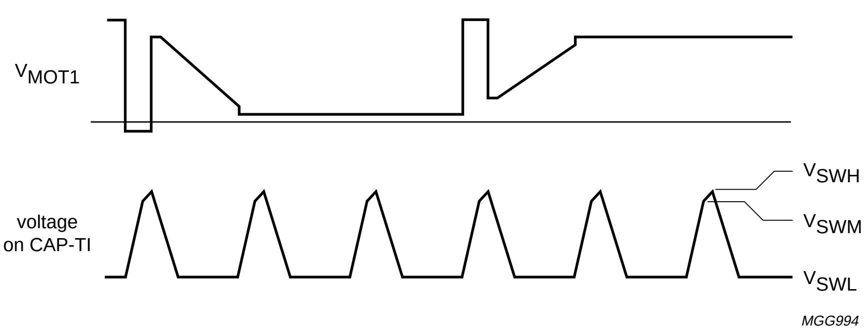
In addition to start-up and commutation control, the TDF5242T provides the following functions:

- Generation of the tacho signal FG
- General purpose Operational Transconductance Amplifier (OTA)
- Possibilities of motor control
- Direction function and brake function
- High current and temperature protection.

THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sink current enables the OTA to drive a power transistor directly in an analog control amplifier or in a SMPS driver.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation is provided.



If the chosen value of CAP-TI is too small, oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

Fig.4 Typical CAP-TI and V_{MOT1} voltage waveforms in normal running mode.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as a load) connected from the output (AMP OUT) to the positive supply, a positive-going voltage is found when the non-inverting input (+AMP IN) is positive with respect to the inverting input (–AMP IN). Note that a ‘plus’ input causes less current, and consequently a positive voltage.

MOTOR CONTROL

DC motors can also be operated with analog control using the OTA.

For the analog control an external transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.8).

FG SIGNAL

The FG (Frequency Generator) signal is generated in the TDF5242T by using the zero-crossing of the motor EMF from the three motor windings and the commutation signal.

Output FG switches from HIGH-to-LOW on all zero crossings and from LOW-to-HIGH on all commutations. Output FG can source typically 75 μA and sink more than 3 mA.

Example: a 3-phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of $25 \times 6 \times 6$ = 900 Hz, and generates a tacho signal of 900 Hz.

DIRECTION FUNCTION

- If the voltage on pin 7 is <2.3 V the motor is running in one direction (depending on the motor connections)
- If pin 7 is floating or the voltage is >2.7 V the motor is running in the other direction.

BRAKE FUNCTION

- If the voltage on pin 9 (pin BRAKE) is <2.3 V the motor brakes; in this condition the external outputs are driven to a HIGH voltage level
- If pin 9 is floating or the voltage is >2.7 V the motor runs normally.

RELIABILITY

The output stages are protected in two ways:

- Current limiting of the ‘lower’ output transistors. The ‘upper’ output transistors use the same base current as the conducting ‘lower’ transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved in such a way that the transistors are switched off when the junction temperature becomes too high.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		4	18	V
V_I	input voltage; all pins except VMOT, CAP-ST, CAP-TI, CAP-CD and CAP-DC	V_I < 18 V	–0.3	V_P + 0.5	V
V_{VMOT}	VMOT input voltage		3	18	V
V_O	output voltage				
	FG		GND	V_P	V
	AMP OUT		–	18	V
	OUT-NA, OUT-NB and OUT-NC		–	V_{VMOT} – 0.9	V
	OUT-PA, OUT-PB and OUT-PC		0.2	–	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC		–	2.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
P_{tot}	total power dissipation	see Fig.5	–	–	
V_{es}	electrostatic handling	see Chapter “Handling”	–	500	V

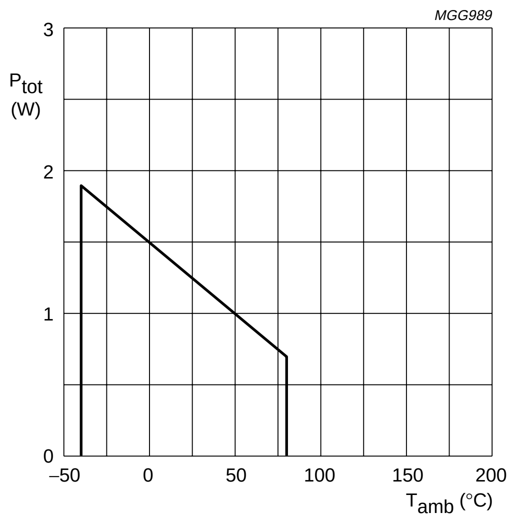


Fig.5 Power derating curve.

HANDLING

Every pin withstands the ESD test according to *“MIL-STD-883C class 2”*. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”*. The number of the quality specification can be found in the *”Quality Reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

CHARACTERISTICS

V_P = 14.5 V ±10%; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	4	–	18	V
I_P	supply current	note 2	–	5.2	6.25	mA
V_{VMOT}	input voltage to the output driver stages	see Fig.1	3	–	18	V
Thermal protection						
T_{SD}	temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	decrease in temperature before switch-on after shut-down		–	T_{SD} – 30	–	K
COMP-A, COMP-B, COMP-C and MOT0						
V_I	input voltage		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	μA
V_{CSW}	comparator switching level	note 3	±20	±25	±30	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_{hys}	comparator input hysteresis	T_{amb} = 25 °C	–	75	–	μV
OUT-NA, OUT-NB, OUT-NC, OUT-PA, OUT-PB and OUT-PC						
$V_{O(n)}$	n-channel driver output voltage	upper transistor; I_O = –100 mA; T_{amb} = 25 °C	–1.05	–	–	V
		lower transistor; I_O = 10 mA; T_{amb} = 25 °C	–	–	0.35	V
$V_{O(p)}$	p-channel driver output voltage	upper transistor; I_O = –10 mA; T_{amb} = 25 °C	–1.05	–	–	V
		lower transistor; I_O = 100 mA; T_{amb} = 25 °C	–	–	0.35	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA; T_{amb} = 25 °C	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA; T_{amb} = 25 °C	–	–	180	mV
I_{LIM}	current limiting	lower transistor; R_O = 47 Ω	150	180	250	mA
+AMP IN and –AMP IN						
V_I	input voltage		–0.3	–	V_P – 1.7	V
	differential mode voltage without ‘latch-up’		–	–	$\pm V_P$	V
I_b	input bias current	T_{amb} = 25 °C	–	–	650	nA
C_I	input capacitance	T_{amb} = 25 °C	–	4	–	pF
V_{offset}	input offset voltage		–	–	10	mV

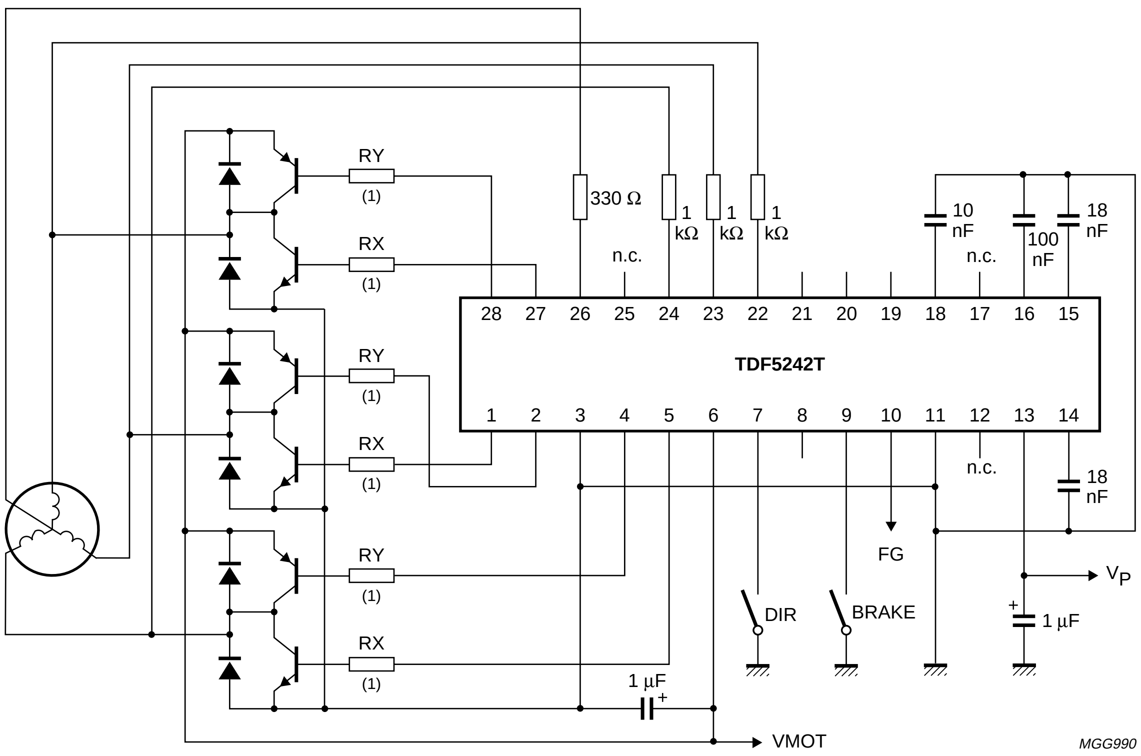
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AMP OUT (open collector)						
I_{sink}	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_O	output voltage		–0.5	–	+18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	40	–	–	mA/μs
$g_{m(tr)}$	transfer gain		0.3	–	–	S
DIR						
V_{IL}	LOW level input voltage (reverse rotation)	reverse mode; 4 V < V_P < 18 V	–	–	2.3	V
V_{IH}	HIGH level input voltage (normal rotation)	normal mode; 4 V < V_P < 18 V	2.7	–	–	V
I_{IL}	LOW level input current (reverse rotation)	reverse mode; T_{amb} = 25 °C	–	–20	–	μA
I_{IH}	HIGH level input current (normal rotation)	normal mode; T_{amb} = 25 °C	–	0	–	μA
BRAKE						
V_{BM}	brake-mode voltage	enable brake mode; 4 V < V_P < 18 V	–	–	2.3	V
		normal mode; 4 V < V_P < 18 V	2.7	–	–	V
I_I	input current	brake mode; T_{amb} = 25 °C	–	–20	–30	μA
		normal mode; T_{amb} = 25 °C	–	0	20	μA
FG (push-pull)						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = –60 μA	–	V_P – 0.3	–	V
t_{THL}	HIGH-to-LOW transition time	T_{amb} = 25 °C; C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	μs
$\frac{f_{FG}}{f_{comm}}$	ratio of FG frequency and commutation frequency	T_{amb} = 25 °C	–	1	–	
CAP-ST						
I_{sink}	output sink current		1.5	2.0	2.5	μA
I_{source}	output source current		–2.5	–2.0	–1.5	μA
V_{SWL}	LOW level switching voltage	T_{amb} = 25 °C	–	0.20	–	V
V_{SWH}	HIGH level switching voltage	T_{amb} = 25 °C	–	2.20	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-TI						
I_{sink}	output sink current		20	28	38	µA
I_{source}	output source current	0.2 V < V_{CAP-TI} < 0.3 V	–64	–57	–50	µA
		0.3 V < V_{CAP-TI} < 2.2 V	–6.5	–5.5	–4.5	µA
V_{SWL}	LOW level switching voltage	T_{amb} = 25 °C	–	50	–	mV
V_{SWM}	MIDDLE level switching voltage	T_{amb} = 25 °C	–	0.30	–	V
V_{SWH}	HIGH level switching voltage	T_{amb} = 25 °C	–	2.20	–	V
CAP-CD						
I_{sink}	output sink current		10.6	16.2	22	µA
I_{source}	output source current		–5.3	–8.1	–11	µA
I_{sink}/I_{source}	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage	T_{amb} = 25 °C	825	850	875	mV
$\frac{\Delta V_{IL}}{\Delta T}$	temperature coefficient of LOW level input voltage		–	–1.4	–	mV/K
V_{IH}	HIGH level input voltage		2.3	–	2.5	V
CAP-DC						
I_{sink}	output sink current		10.1	15.5	20.9	µA
I_{source}	output source current		–20.9	–15.5	–10.1	µA
I_{sink}/I_{source}	ratio of sink to source current		0.9	1.025	1.15	
V_{IL}	LOW level input voltage	T_{amb} = 25 °C	825	850	875	mV
$\frac{\Delta V_{IL}}{\Delta T}$	temperature coefficient of LOW level input voltage		–	–1.4	–	mV/K
V_{IH}	HIGH level input voltage		2.3	–	2.5	V

Notes

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; all other inputs at 0 V; all outputs at V_P; I_O = 0 mA.
3. Switching levels with respect to driver outputs OUT-NA, OUT-NB, OUT-NC, OUT-PA, OUT-PB and OUT-PC.

APPLICATION INFORMATION



(1) RX = RY > 8 (VMOT – 1.5).

Fig.6 Application diagram without use of the Operational Transconductance Amplifier (OTA) with bipolar power transistors.

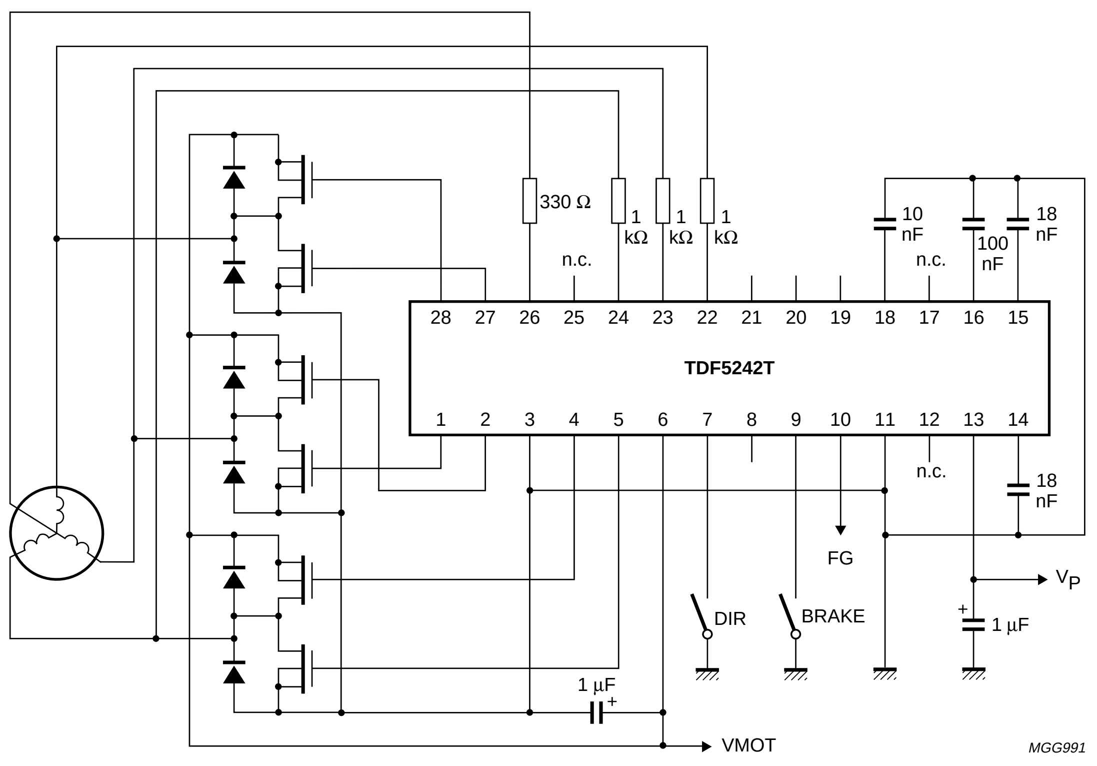


Fig.7 Application diagram without use of the Operational Transconductance Amplifier (OTA) with MOSFETs.

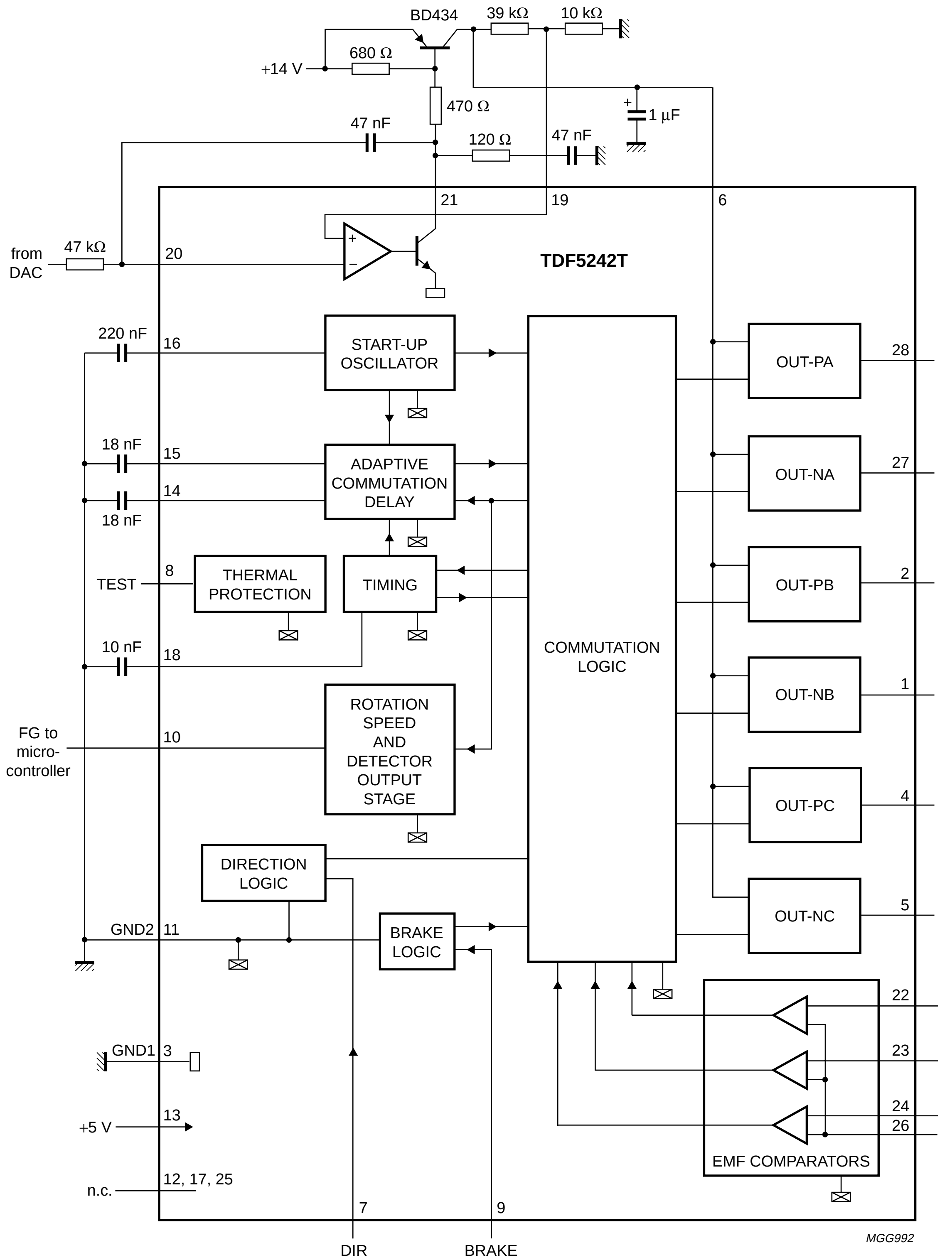
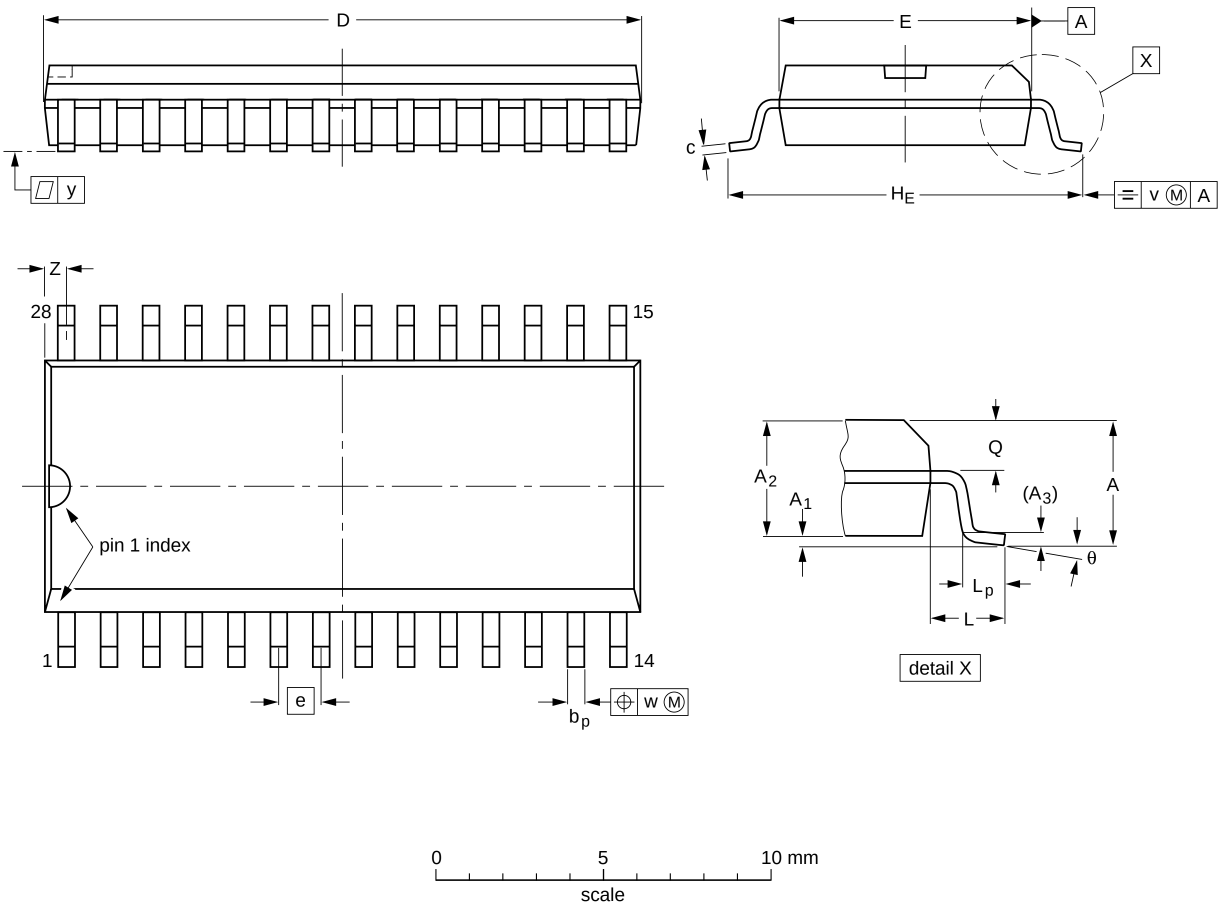


Fig.8 Application of the TDF5242T as a scanner driver, with the use of the uncommitted on-chip OTA.

PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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