

## Bi-directional ESD Protection Diode

### FEATURES

- Meet IEC61000-4-2 (ESD)  $\pm 15\text{kV}$  (air),  $\pm 8\text{kV}$  (contact)
- Designed for mounting on small surface
- Protects one Bi-directional I/O line
- Moisture sensitivity level 1
- Working Voltage : 5V, 12V, 24V
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21


**0603**


### MECHANICAL DATA

- Case: 0603 small outline plastic package
- Terminal : Gold plated, solder per MIL-STD-705, method 2026 guaranteed
- High temperature soldering guaranteed :  $260^{\circ}\text{C}/10\text{s}$
- Weight:  $3 \pm 0.5 \text{ mg}$



### APPLICATIONS

- Cell Phone Handsets and Accessories
- Notebooks, Desktops, and Servers
- Keypads, Side Keys, USB 2.0, LCD Displays
- Portable Instrumentation
- Touch Panel

### MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	VALUE	UNIT
Peak Pulse Power ( $t_p=8/20\mu\text{s}$ waveform)	TESDU5V0	75	W
	TESDU12V	25	
	TESDU24V	47	
ESD per IEC 61000-4-2 (Air)	$V_{\text{ESD}}$	$\pm 15$	KV
ESD per IEC 61000-4-2 (Contact)		$\pm 8$	
Junction and Storage Temperature Range	$T_J, T_{\text{STG}}$	-55 to +150	$^{\circ}\text{C}$

PARAMETER	SYMBOL	MIN	MAX	UNIT
Reverse Stand-Off Voltage	$V_{\text{RWM}}$	-	5	V
		-	12	
		-	24	
Reverse Breakdown Voltage	$V_{(\text{BR})}$	5.1	-	V
		13	-	
		25	-	
Reverse Leakage Current	$I_{\text{R}}$	$V_{\text{R}} = 5 \text{ V}$	2	$\mu\text{A}$
		$V_{\text{R}} = 12 \text{ V}$		
		$V_{\text{R}} = 24 \text{ V}$		
Clamping Voltage	$V_{\text{C}}$	$I_{\text{PP}} = 1 \text{ A}$	9.8	V
		$I_{\text{PP}} = 5 \text{ A}$	15	
Clamping Voltage	$V_{\text{C}}$	$I_{\text{PP}} = 1 \text{ A}$	25	V
		$I_{\text{PP}} = 5 \text{ A}$	33	
Clamping Voltage	$V_{\text{C}}$	$I_{\text{PP}} = 1 \text{ A}$	47	V
		$I_{\text{PP}} = 5 \text{ A}$	51	
Junction Capacitance	$C_{\text{J}}$	$V_{\text{R}} = 0 \text{ V}$	15	pF
		$f = 1.0 \text{ MHz}$	12	
			10	

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**RATINGS AND CHARACTERISTICS CURVES**

( $T_A=25^\circ\text{C}$  unless otherwise noted)

Fig. 1 Admissible Power Dissipation Curve

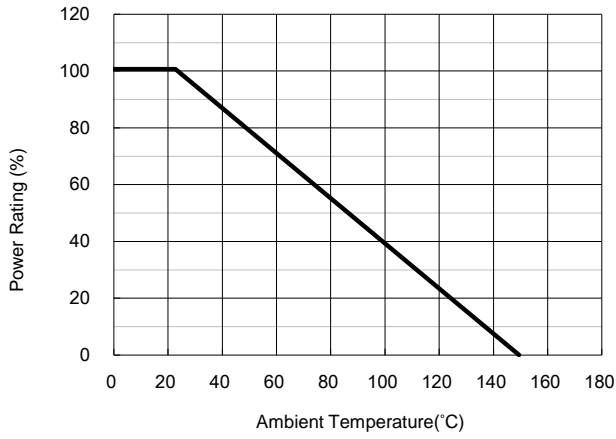


Fig. 2 Typical Junction Capacitance

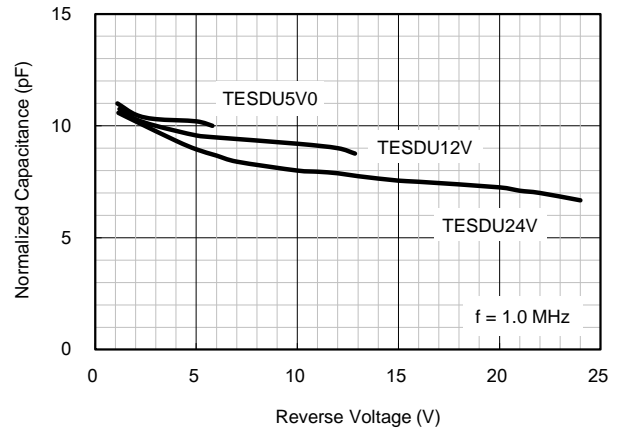
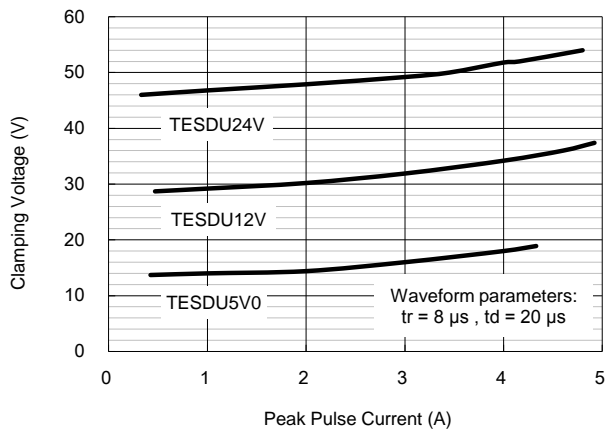


Fig. 3 Clamping Voltage VS. Peak Pulse Current



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**ORDERING INFORMATION**

PART NO.	PACKING CODE	PACKING CODE SUFFIX	PACKAGE	PACKING
TESDUxxx (Note1, 2)	RG	G	0603	4,000 / 7" Reel

Note 1: "xxx" defines voltage from 5V (TESDU5V0) to 24V (TESDU24V)

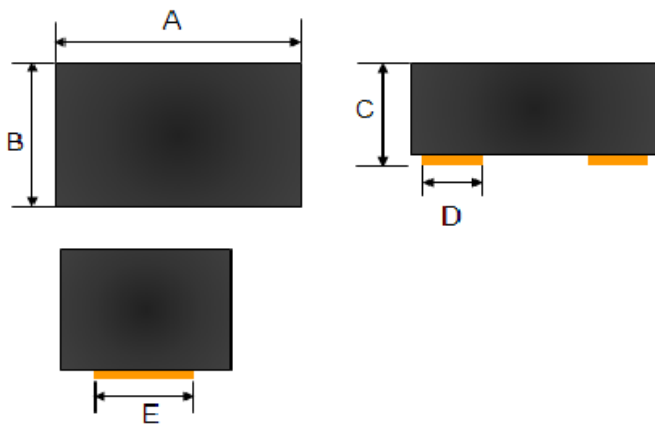
Note 2: Whole series with green compound

**EXAMPLE**

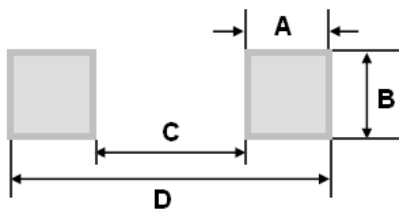
EXAMPLE P/N	PART NO.	PACKING CODE	PACKING CODE SUFFIX	DESCRIPTION
TESDU5V0 RGG	TESDU5V0	RG	G	Green compound

**PACKAGE OUTLINE DIMENSIONS**

0603



DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	1.60	1.80	0.063	0.071
B	0.80	1.00	0.031	0.039
C	0.70	0.85	0.028	0.033
D	0.45 (Typ.)		0.018 (Typ.)	
E	0.70 (Typ.)		0.028 (Typ.)	

**SUGGEST PAD LAYOUT**


DIM.	Unit (mm)	Unit (inch)
	Typ.	Typ.
A	0.60	0.024
B	1.00	0.039
C	0.65	0.026
D	1.85	0.073

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

**MARKING**

Part NO.	Marking
TESDU5V0	E05
TESDU12V	E12
TESDU24V	E24

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**APPLICATIONS INFORMATION**

- ◇ Designed to protect one data, I/O, or power supply line
- ◇ Designed to protect sensitive electronics from damage or latch-up due to ESD
- ◇ Designed to replace multilayer varistors (MLVs) in portable applications
- ◇ Features large cross-sectional area junctions for conducting high transient currents
- ◇ Offers superior electrical characteristics such as lower clamping voltage and no device degradation when compared to MLVs
- ◇ The combination of small size and high ESD surge capability makes them ideal for use in portable applications

**CIRCUIT BOARD LAYOUT RECOMMENDATIONS**

Good circuit board layout is critical for the suppression of ESD induced transients

- ◇ Place the ESD Protection Diode near the input terminals or connectors to restrict transient coupling
- ◇ Minimize the path length between the ESD Protection Diode and the protected line
- ◇ Minimize all conductive loops including power and ground loops
- ◇ The ESD transient return path to ground should be kept as short as possible
- ◇ Never run critical signals near board edges
- ◇ Use ground planes whenever possible

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