TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

2GBIT (256M × 8BITS) CMOS NAND E^{2}PROM

DESCRIPTION

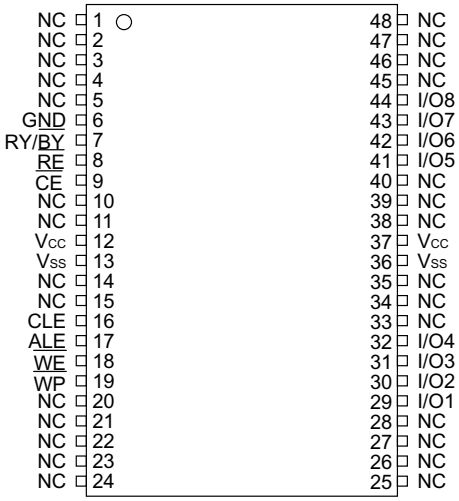
The TH58NVG1S3A is a single 3.3-V 2G-bit (2,214,592,512 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E²PROM) organized as (2048+64) bytes x 64 pages x 2048 blocks. The device has a 2112-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 2112-byte increments. The Erase operation is implemented in a single block unit (128 Kbytes + 4Kbytes: 2112 bytes x 64 pages).

The TH58NVG1S3A is a serial-type memory device which utilizes the I/O pins for both address and data input / output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization
  - Memory cell allay 2112 × 64K × 8 × 2
  - Register 2112 × 8
  - Page size 2112bytes
  - Block size (128K + 4K) bytes
- Modes
  - Read, Reset, Auto Page Program
  - Auto Block Erase, Status Read
- Mode control
  - Serial input／output
  - Command control
- Powersupply V_{CC} = 2.7 V to 3.6 V
- Program/Erase Cycles 1E5 Cycles(With ECC)
- Access time
  - Cell array to register 25 μs max
  - Serial Read Cycle 50 ns min
- Operating current
  - Read (50 ns cycle) 10 mA typ.
  - Program (avg.) 10 mA typ.
  - Erase (avg.) 10 mA typ.
  - Standby 50 μA max
- Package
  - TSOP I 48-P-1220-0.50
  - (Weight : 0.53 g typ.)

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

I/O1 to I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY / $\overline{BY}$	Ready / Busy
GND	Ground Input
V_{CC}	Power supply
V_{SS}	Ground

000707EBA1

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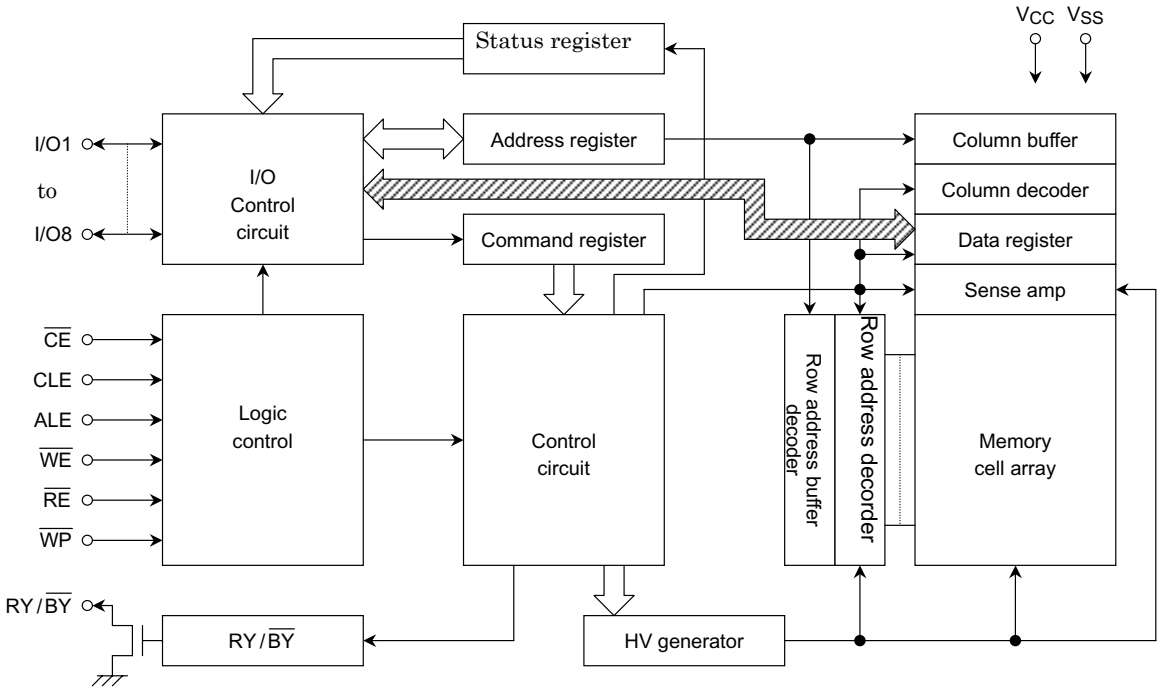
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	−0.6 V to V_{CC} + 0.3 V (≦ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10s)	260	°C
T_{STG}	Storage Temperature	-55 to 150	°C
T_{OPR}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	20	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	20	pF

* * This parameter is periodically sampled and is not tested for every device.

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VALID BLOCKS (1)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	2008	-	2048	Blocks

(1) The TH58NVG1S3A occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.

(2) The first block (block address #00) is guaranteed to be a valid block at the time of shipment.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	3.3	3.6	V
V_{IH}	High Level input Voltage	2.0	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	−0.3*	—	0.8	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta =0 to 70℃, V_{CC} = 2.7V ~ 3.3 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO1}	Reading	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, t_{cycle} = 50 ns	—	10	30	mA
I_{CCO7}	Programming Current	—	—	10	30	mA
I_{CCO8}	Erasing Current	—	—	10	30	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}, $\overline{WP}$ = 0V/VCC	—	—	1	mA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2 V, $\overline{WP}$ = 0V/VCC	—	—	50	μA
V_{OH}	High Level Output Voltage	Vcc, I_{OH} = −400 μA	2.4	—	—	V
V_{OL}	Low Level Output Voltage	Vcc, I_{OL} = 2.1 mA	—	—	0.4	V
I_{OL} (RY / $\overline{BY}$)	Output current of RY / $\overline{BY}$ pin	V_{OL} = 0.4 V	—	8	—	mA

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70℃, V_{CC} = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CLS}	CLE Setup Time	0	—	ns	
t_{CLH}	CLE Hold Time	10	—	ns	
t_{CS}	$\overline{CE}$ Setup Time	0	—	ns	
t_{CH}	$\overline{CE}$ Hold Time	10	—	ns	
t_{WP}	Write Pulse Width	25	—	ns	
t_{ALS}	ALE Setup Time	0	—	ns	
t_{ALH}	ALE Hold Time	10	—	ns	
t_{DS}	Data Setup Time	20	—	ns	
t_{DH}	Data Hold Time	10	—	ns	
t_{WC}	Write Cycle Time	50	—	ns	
t_{WH}	$\overline{WE}$ High Hold Time	15	—	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns	
t_{RW}	Ready to $\overline{WE}$ Falling Edge	20	—	ns	
t_{RP}	Read Pulse Width	35	—	ns	
t_{RC}	Read Cycle Time	50	—	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	—	35	ns	
t_{CEA}	$\overline{CE}$ Access Time	—	45	ns	
t_{CLEA}	CLE Access Time	—	45	ns	
t_{ALEA}	ALE Access Time	—	45	ns	
t_{REAID}	$\overline{RE}$ Access Time (ID Read)	—	35	ns	
t_{OH}	Data Output Hold Time	10	—	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	30	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns	
t_{REH}	$\overline{RE}$ High Hold Time	15	—	ns	
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	—	35	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	—	45	ns	
t_{CLSTO}	CLE Access Time (Status Read)	—	45	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	30	—	ns	
t_{R}	Memory Cell Array to Starting Address	—	25	μs	
t_{WB}	$\overline{WE}$ High to Busy	—	200	ns	
t_{RST}	Device Reset Time (Read/Program/Erase)	—	6/10/500	μs	

AC TEST CONDITIONS

PARAMETER	CONDITION
Input level	2.4 V, 0.4 V
Input pulse rise and fall time	3ns
Input comparison level	1.5 V, 1.5 V
Output data comparison level	1.5 V, 1.5 V
Output load	C_L (100 pF) + 1 TTL

PROGRAMMING AND ERASING CHARACTERISTICS

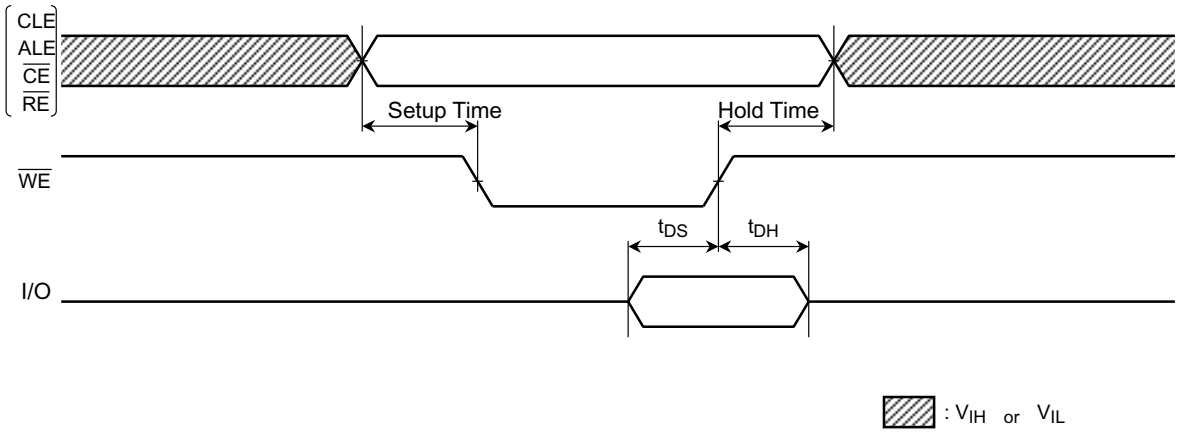
(Ta = 0 to 70℃, V_{CC} = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	200	700	μs	
N	Number of Programming Cycles on Same Page (per 512+16 bytes)	—	—	2		(1)
t_{BERASE}	Block Erasing Time	—	2	4	ms	

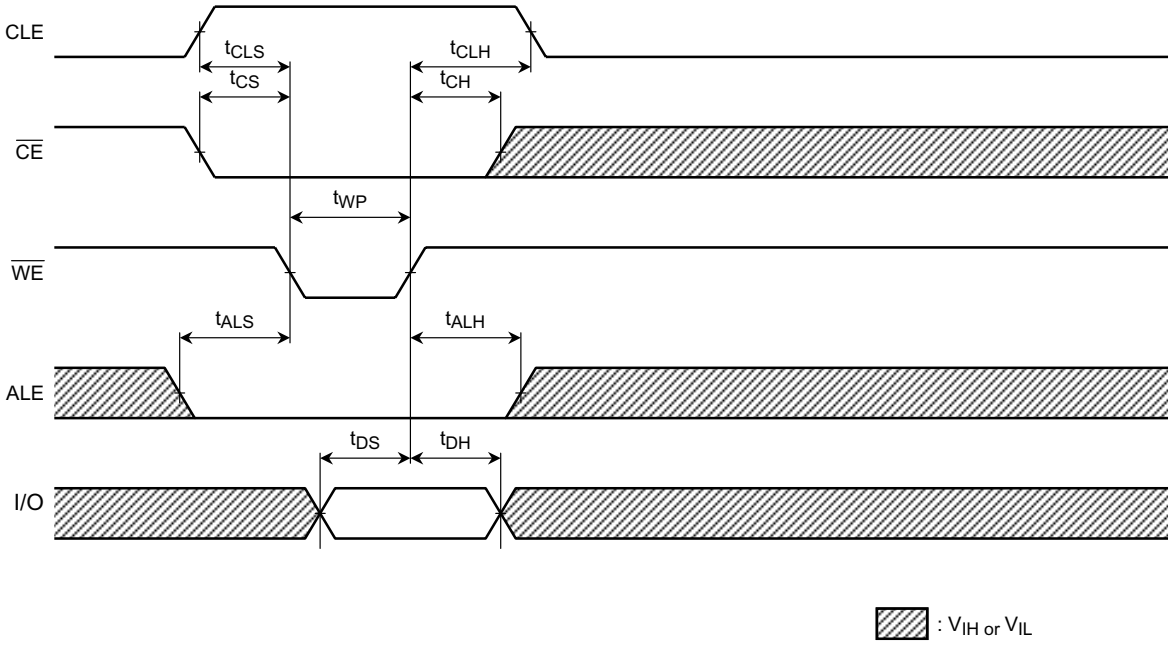
(1) Refer to Application Note (12) toward the end of this document.

TIMING DIAGRAMS

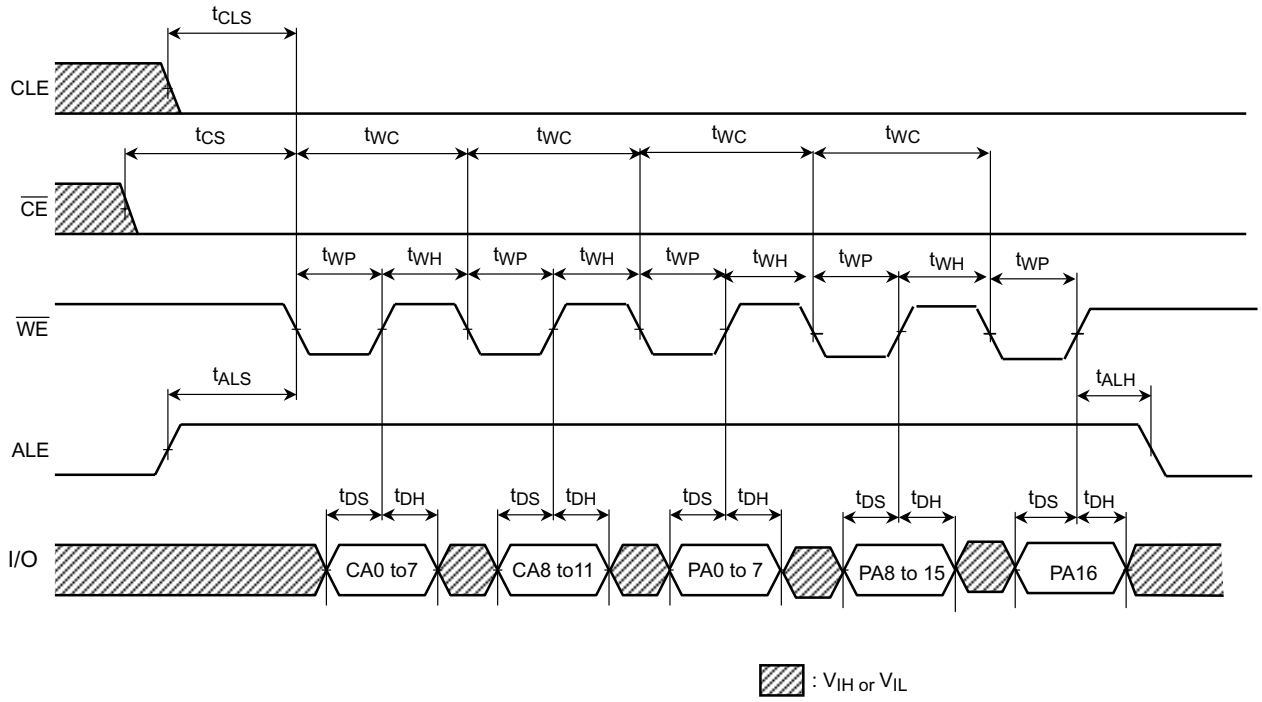
Latch Timing Diagram for Command/Address /Data



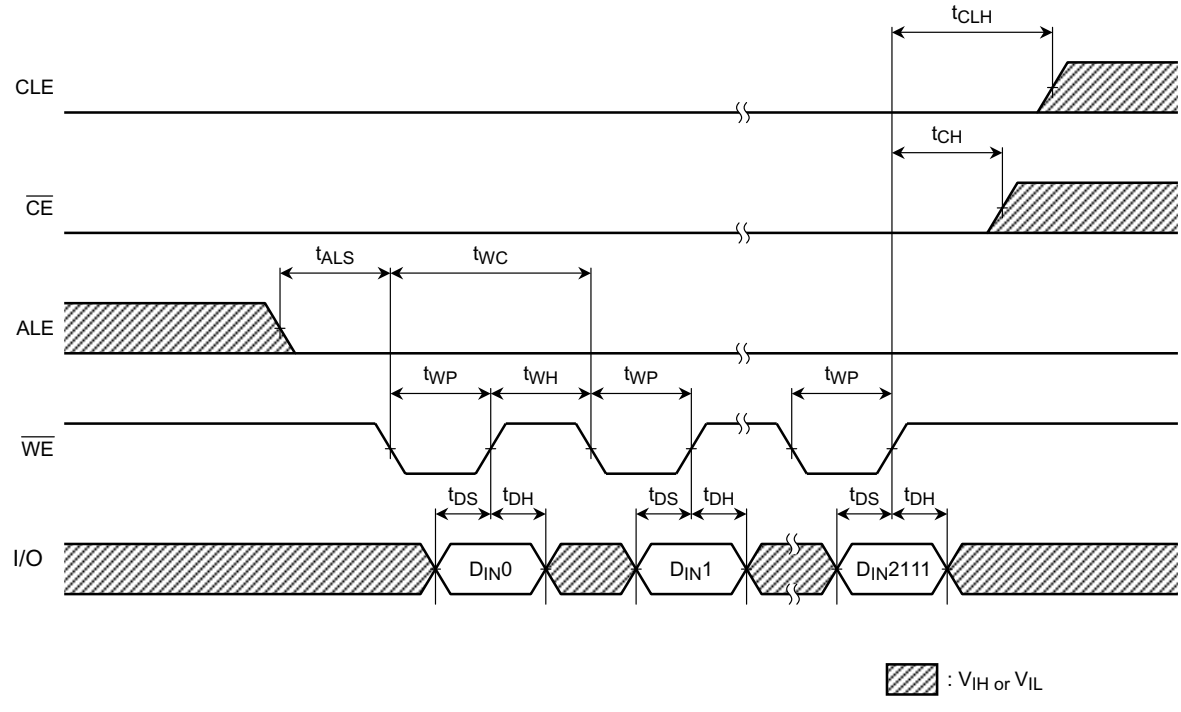
Command Input Cycle Timing Diagram



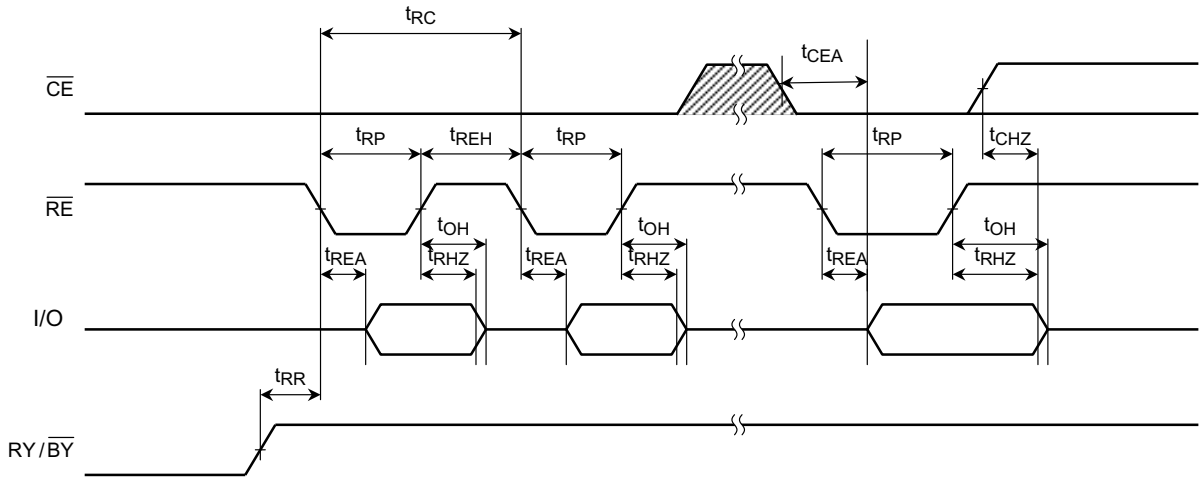
Address Input Cycle Timing Diagram



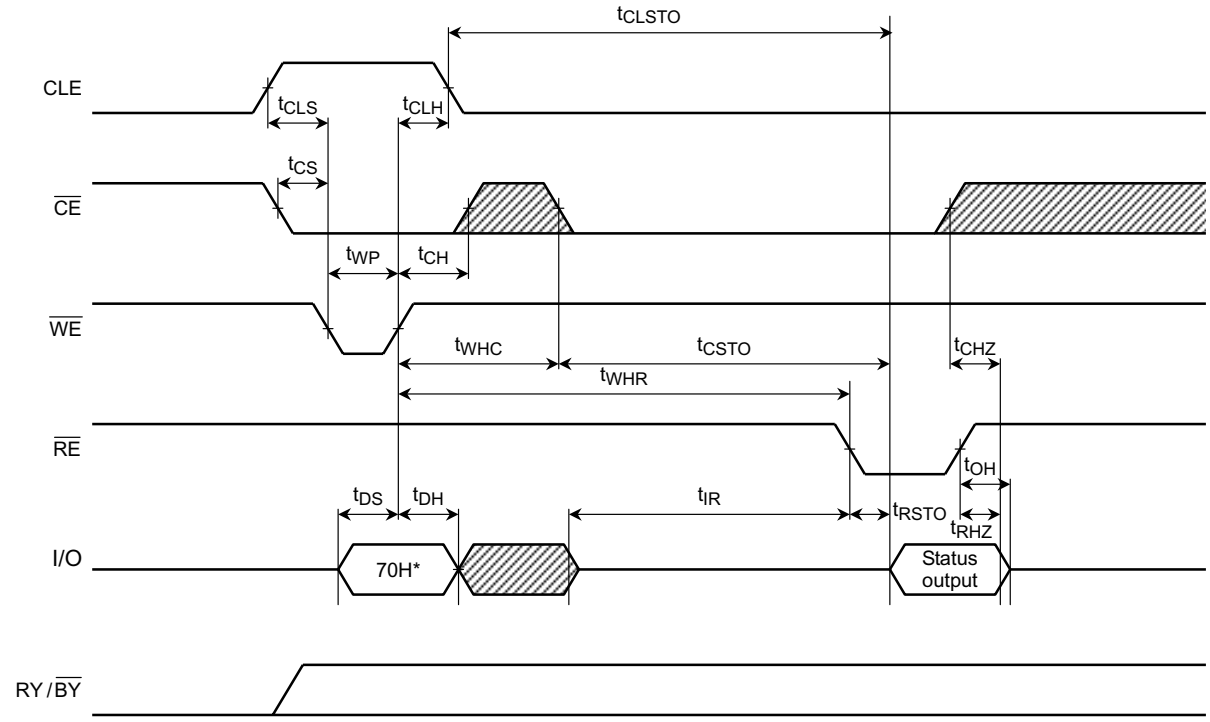
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



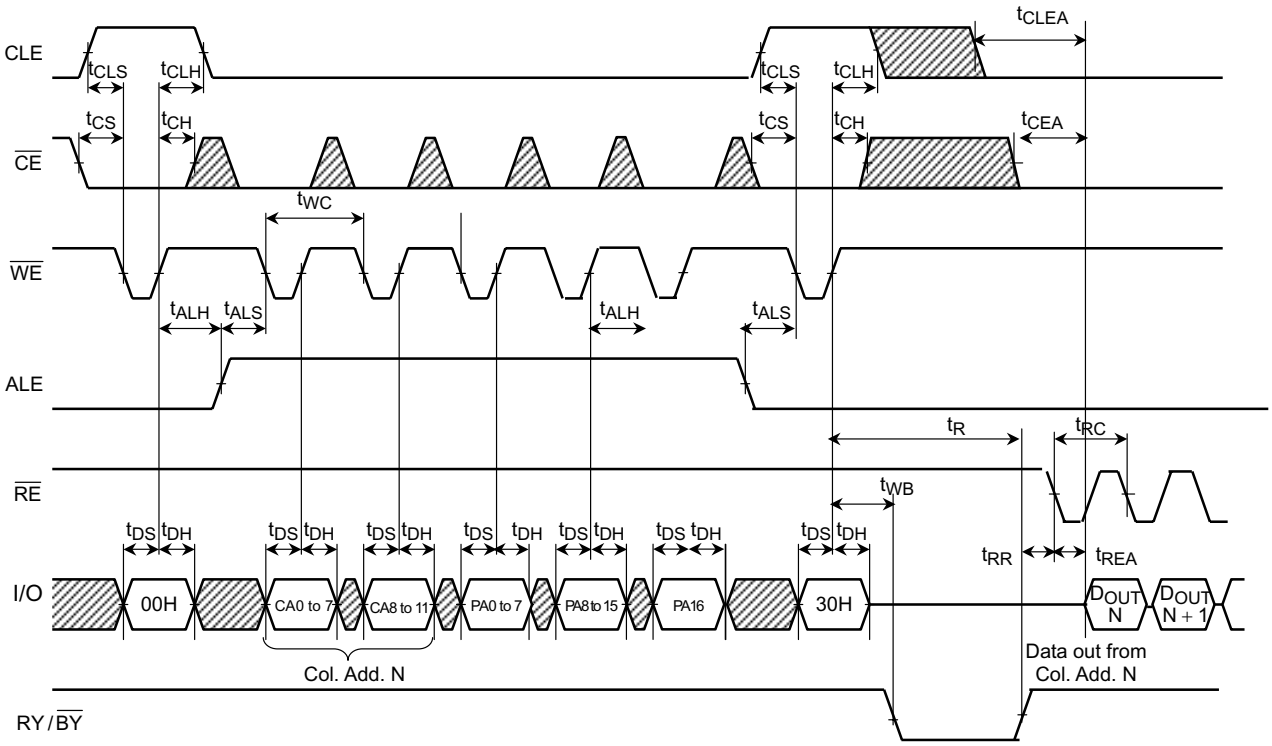
Status Read Cycle Timing Diagram



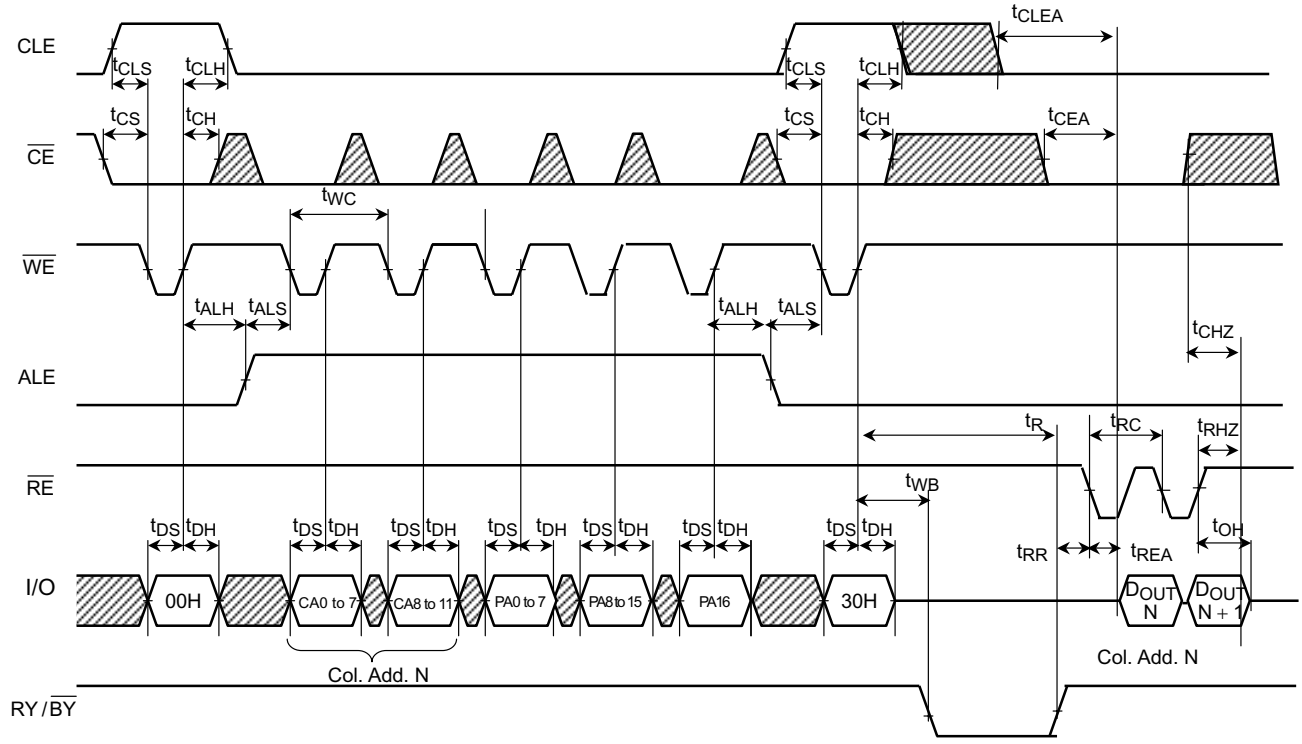
* 70H represents the hexadecimal number

: V_{IH} or V_{IL}

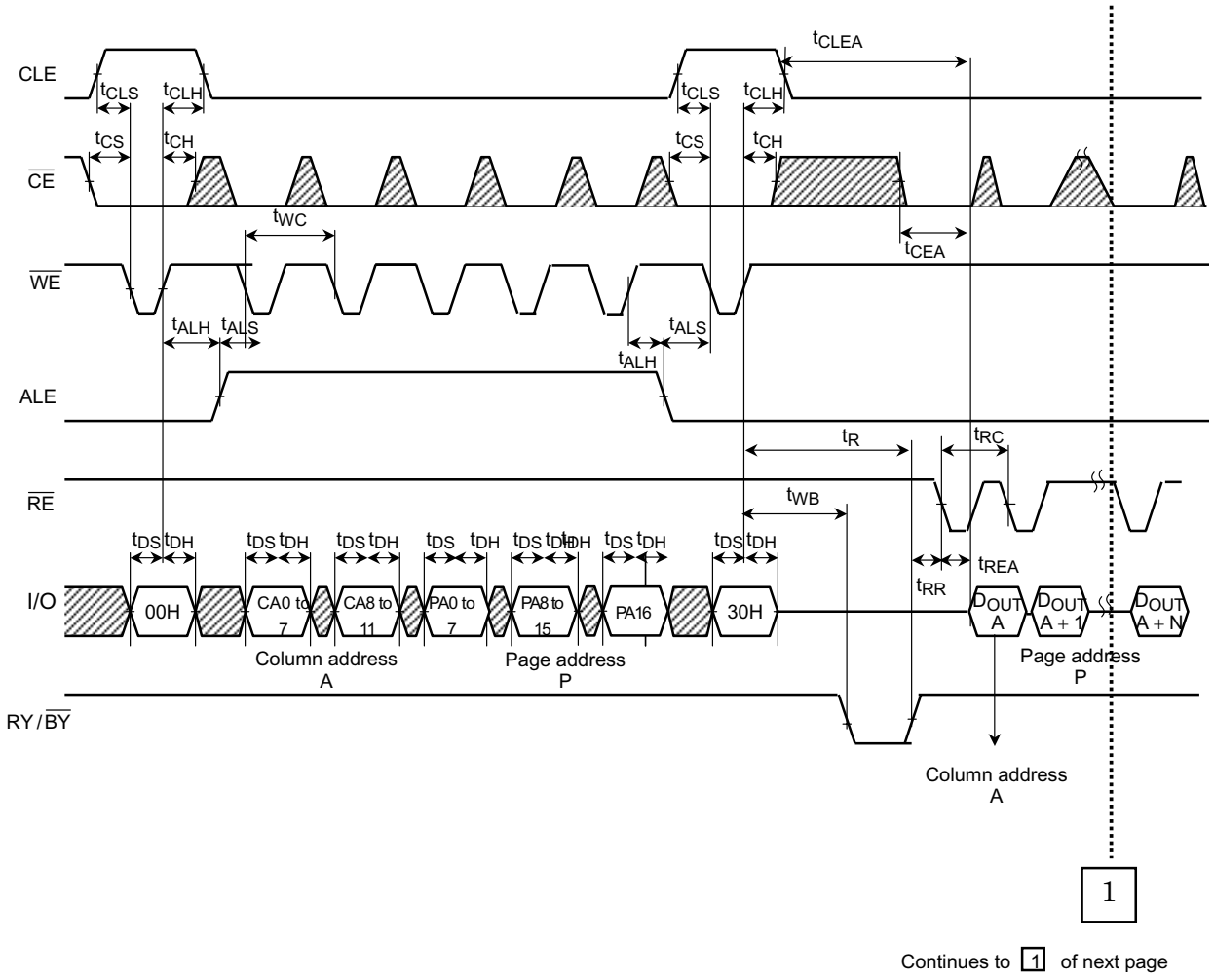
Read Cycle Timing Diagram



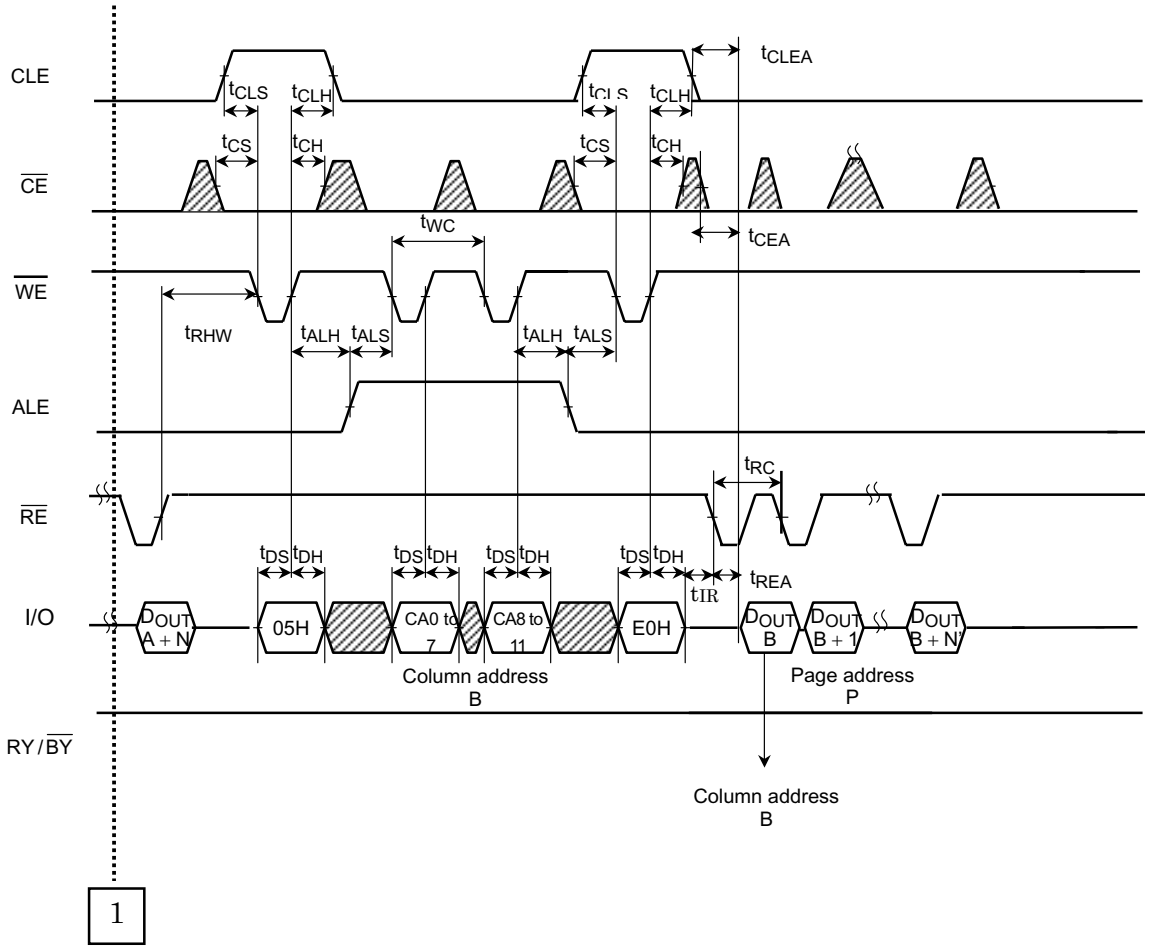
Read Cycle Timing Diagram : When Interrupted by /CE



Column Address Change in Read Cycle Timing Diagram (1/2)



Column Address Change in Read Cycle Timing Diagram (2/2)



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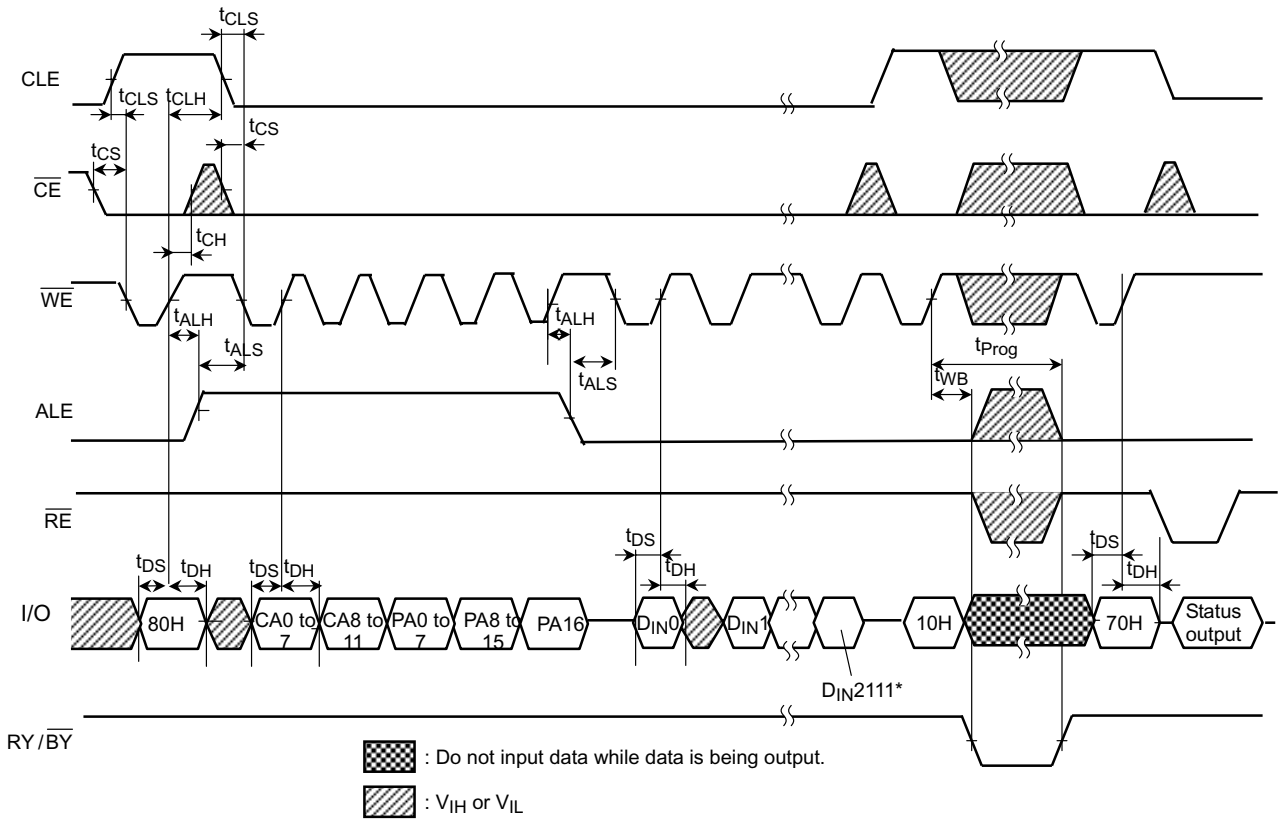
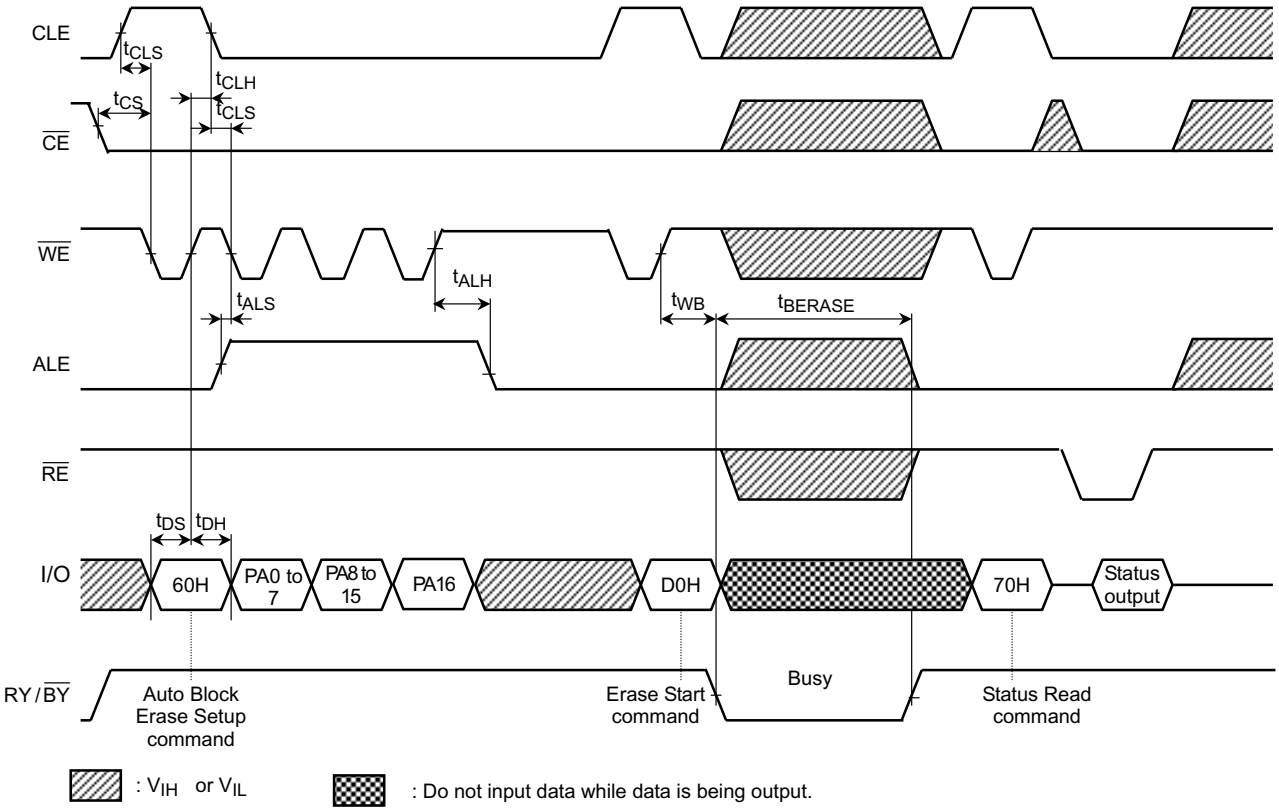
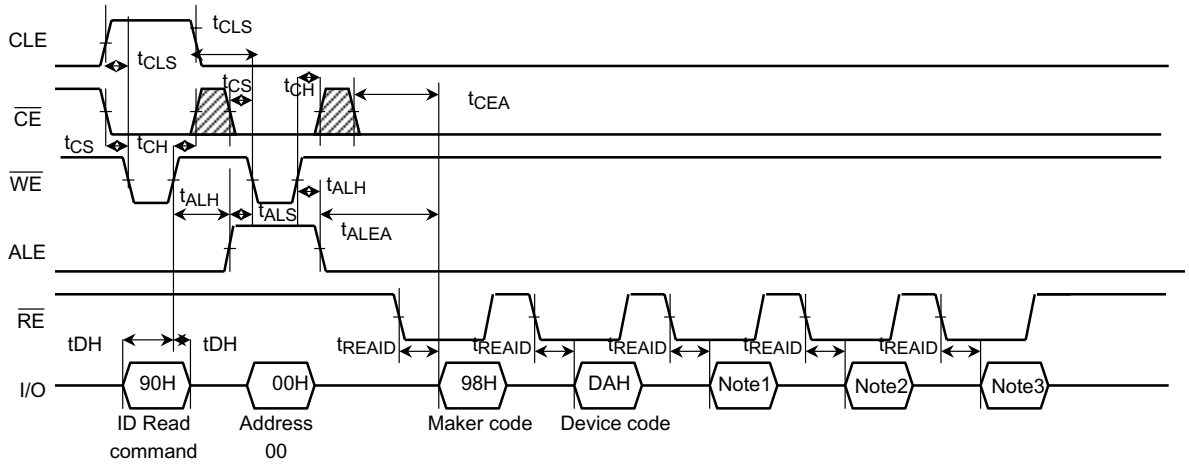
Auto-Program Operation Timing Diagram



Auto Block Erase Timing Diagram



ID Read Operation Timing Diagram



Note1 : 81H or 01H
Note2 : 95H or 15H
Note3 : 44H or C4H

: V_{IH} or V_{IL}

PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

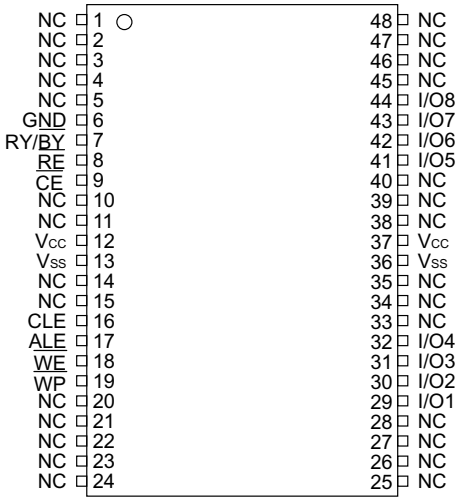


Figure 1. Pinout

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register.

Address information is latched on the rising edge of $\overline{WE}$ if ALE is High.

Input data is latched if ALE is Low.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state ($RY/\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.

The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $RY/\overline{BY}$

The $RY/\overline{BY}$ output signal is used to indicate the operating condition of the device. The $RY/\overline{BY}$ signal is in Busy state ($RY/\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($RY/\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to Vccq with appropriate resister..

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

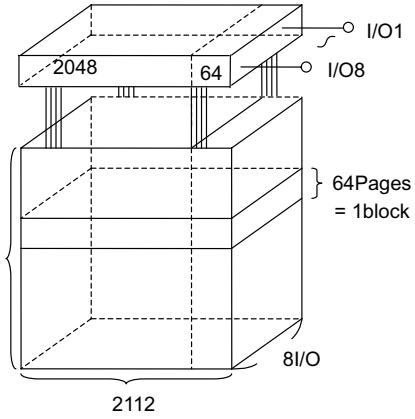


Figure 2. Schematic Cell Layout

A page consists of 2112 bytes in which 2048 bytes are used for main memory storage and 64 bytes are for redundancy or for other uses.

1 page = 2112bytes

1 block = 2112 bytes x 64 pages = (128K + 4K) bytes

Capacity = 2112bytes x 64pages x 2048blocks

An address is read in via the I/0 port over four consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	L	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
Fifth cycle	L	L	L	L	L	L	L	PA16

CA0 to CA11 : Column address
PA0 to PA16 : Page address

PA6 to PA16 : Block address
PA0 to PA5 : NAND address in block

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the eleven different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L	⎍	H	*
Data Input	L	L	L	⎍	H	H
Address input	L	H	L	⎍	H	*
Serial Data Output	L	L	L	H	⎎	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
During Reading (Busy)	*	*	*	*	*	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/Vcc

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Auto Program	10	—	
Read Address Input	00	—	
Column Address Change in Serial Data Output	05	—	
Read Start	30		
Read Column Change	E0	—	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70		○
Reset	FF		○

HEX data bit assignment

(Example)

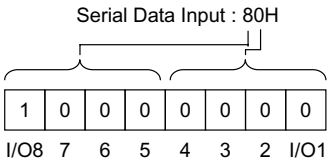


Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

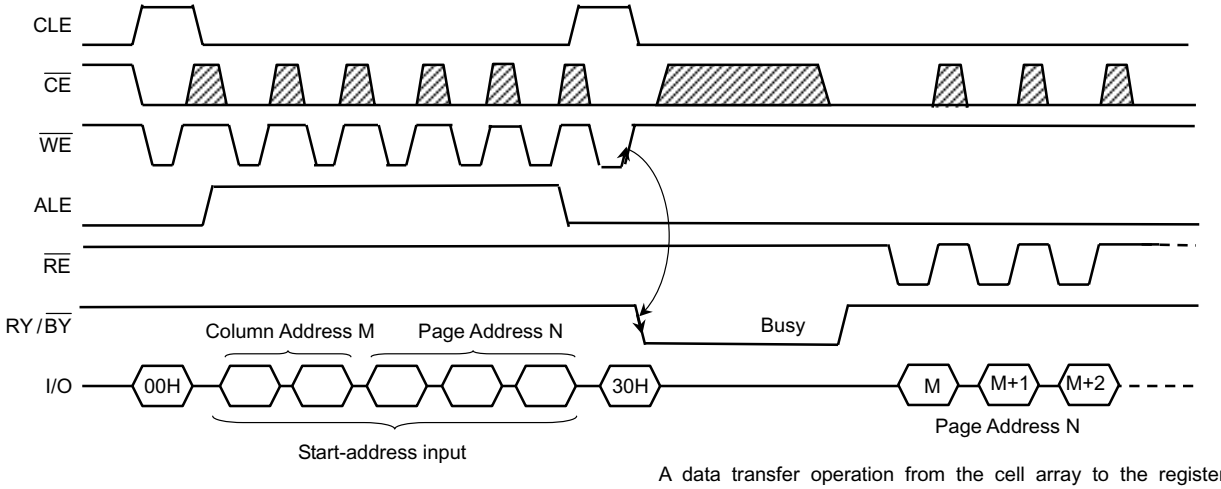
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby
Read Busy	*	*	*	*	*	High Impedance	Active

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

DEVICE OPERATION

Read Mode

Read mode is set when "00H" and "30H" commands are issued to the Command register. Between the commands, start address for the Read mode need to be issued. Refer to Figure 3 below for sequence and the block diagram (Refer to the detailed timing chart.).



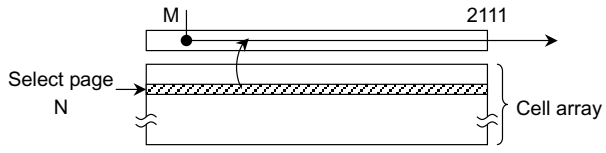
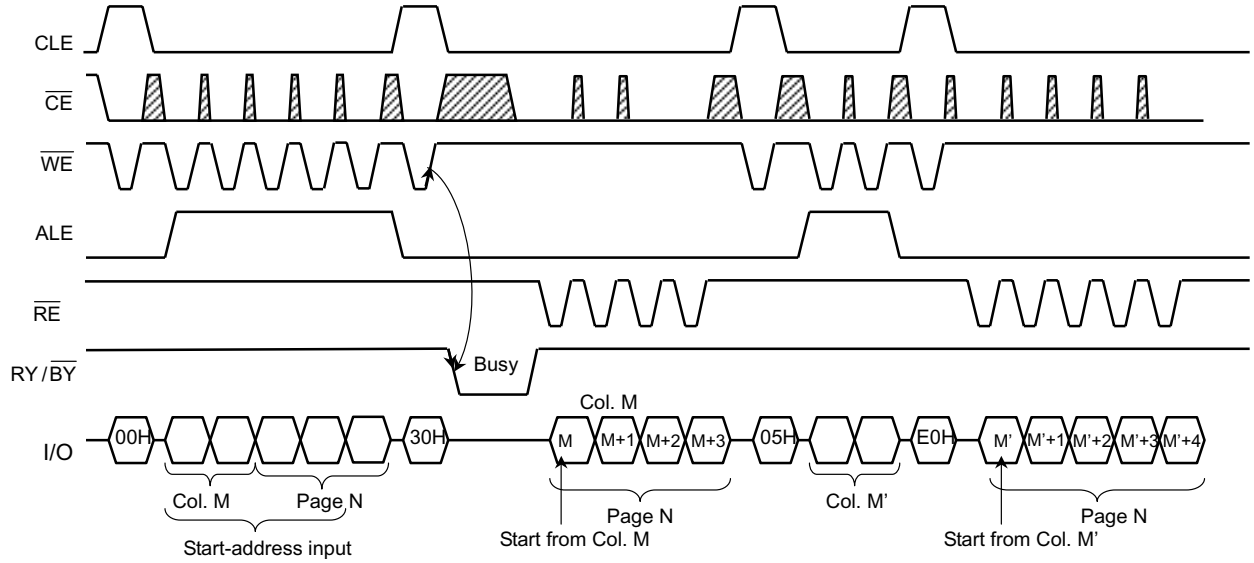


Figure 3. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the address information has been latched). The device will be in Busy state during this transfer period.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

Random Column Address Change in Read Cycle



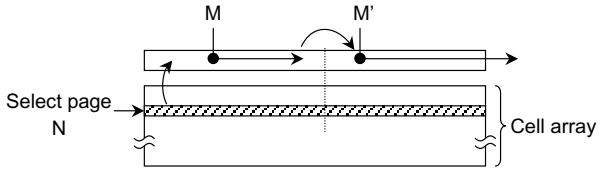


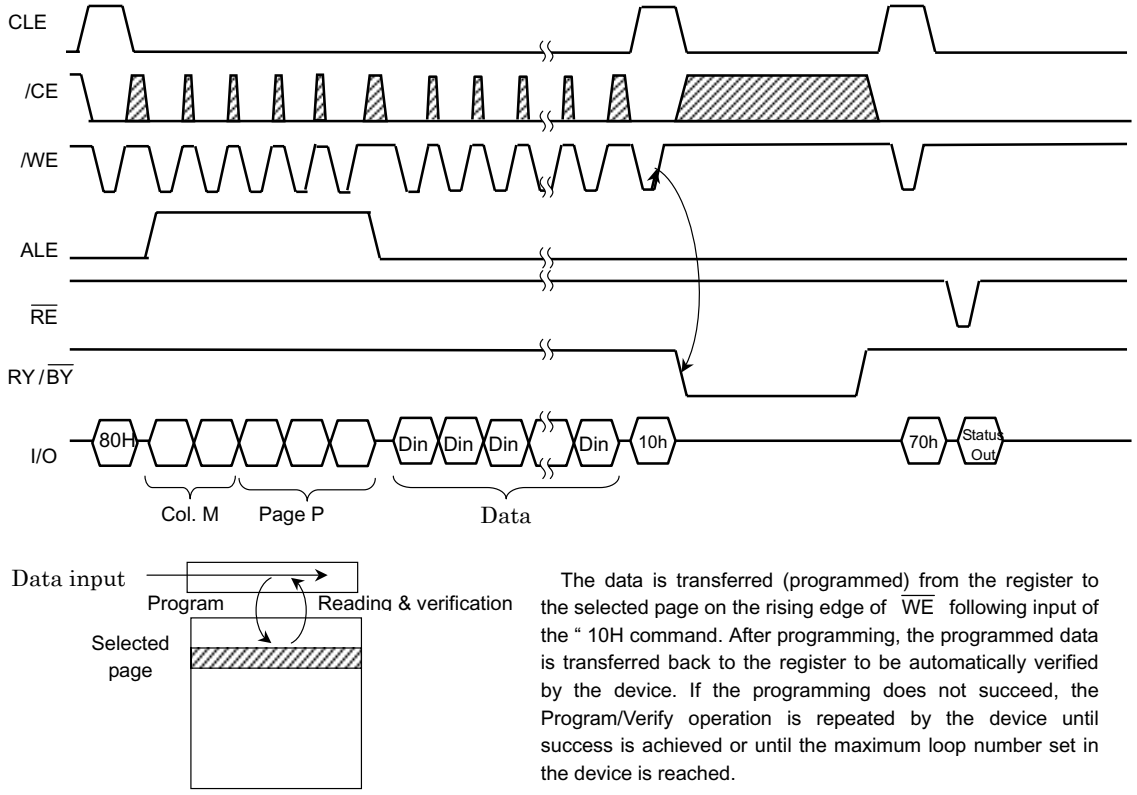
Figure 4. Random Column Address Change in Serial Read

In the serial data out from the register, the column address can be changed by inputting the column address with 05h and E0h commands.

The data are read out in serial from the column address which is input to the device by 05h and E0h commands with /RE clock.

Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10H" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

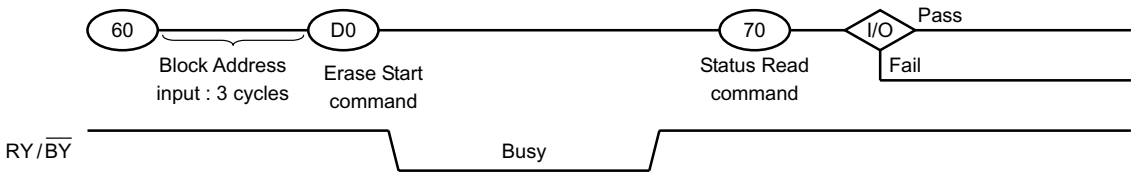


The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following input of the " 10H command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Figure 7. Auto Page Program operation

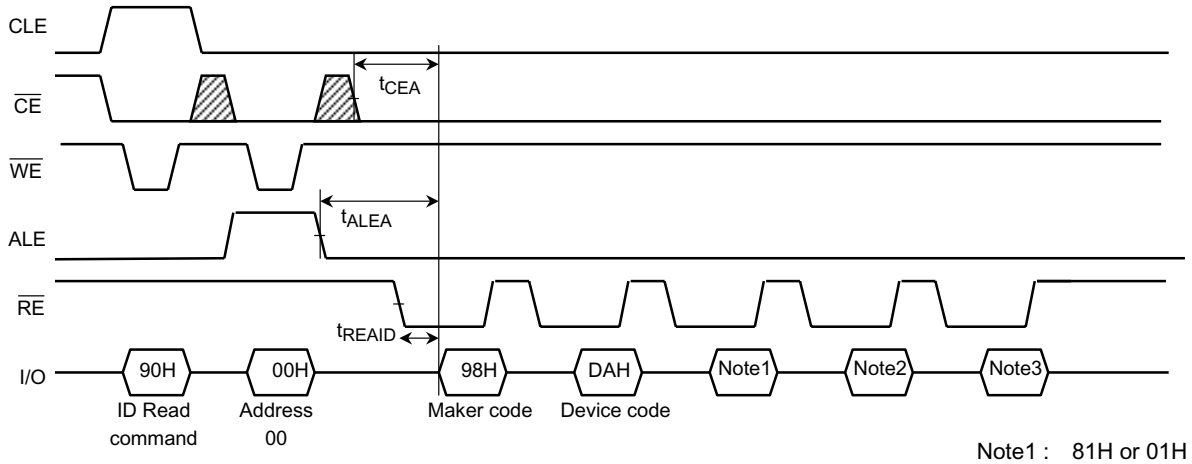
Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command "DOH" which follows the Erase Setup command "60H". This three-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



ID Read

The device contains ID code which identify the device type, the manufacturer, and some features of the device. The ID codes can be read out under the following timing conditions:



For the specifications of the access times t_{REAID} and t_{ALEA} refer to the AC Characteristics.

Note1 : 81H or 01H
Note2 : 95H or 15H
Note3 : 44H or C4H

Figure 13. ID Read timing

Table 6. Code table

	Descripton	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98H
2nd Data	Device Code	1	1	0	1	1	0	1	0	DAH
3rd Data	Chip Number, Cell Type, PGM Page, Write Cache	0 or 1	0	0	0	0	0	0	1	81H or 01H
4th Data	Page Size, Block Size, Redundant Size, Organization	0 or 1	0	0	1	0	1	0	1	95H or 15H
5th Data	Plane Number, Plane Size	0 or 1	1	0	0	0	1	0	0	44H or C4H

3rd Data

	Descripton	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 level cell					0	0		
	4 level cell					0	1		
	8 level cell					1	0		
	16 level cell					1	1		
Number of simultaneously programmed pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Reserved 1			0						
Reserved 2		0 or 1							

4th Data

	Descripton	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size (without redundant area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Block Size (without redundant area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Redundant area size (byte/512byte)	8					0	0		
	16					0	1		
	Reserved					1	0		
	Reserved					1	1		
Organization	X8		0						
	X16		1						
Reserved		0 or 1							

5th Data

	Descripton	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size	64Mb		0	0	0				
	128Mb		0	0	1				
	256Mb		0	1	0				
	512Mb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
Reserved		0 or 1						0	0

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass /fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the $\overline{RE}$ clock after a "70H" command input.

The resulting information is outlined in Table 5.

Table 5. Status output table

	STATUS	OUTPUT	
I/O1	Chip Status 1	Pass: 0	Fail: 1
I/O2	Chip Status 2	Pass: 0	Fail: 1
I/O3	Not Used	0	
I/O4	Not Used	0	
I/O5	Not Used	0	
I/O6	Ready/Busy	Ready: 1	Busy: 0
I/O7	Data Cache Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protected: 1

The Pass/Fail status on I/O1 and I/O2 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

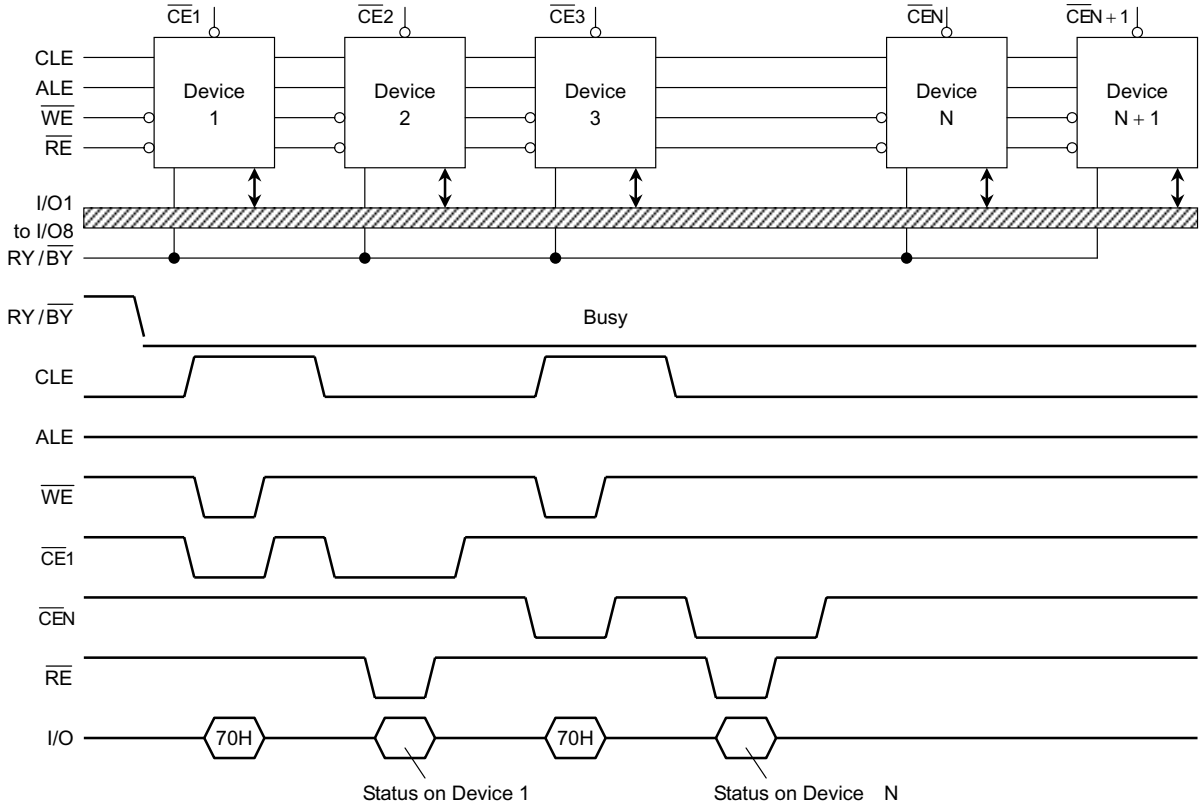


Figure 6. Status Read timing application example

System Design Note: If the RY / $\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.
The response to an "FFH" Reset command input during the various device operations is as follows:

When a Reset (FFH) command is input during programming

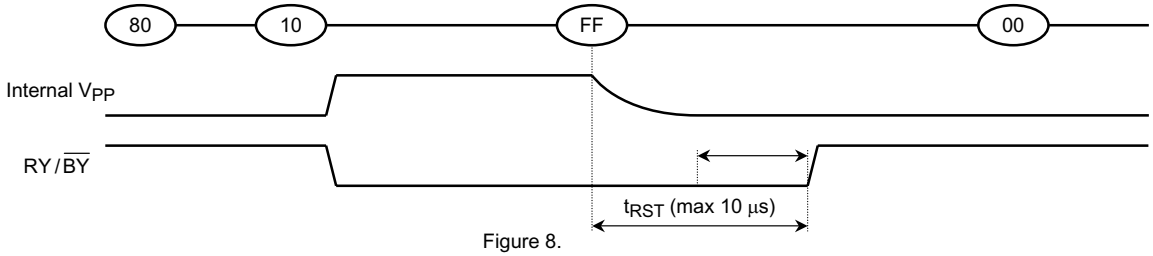


Figure 8.

When a Reset (FFH) command is input during erasing

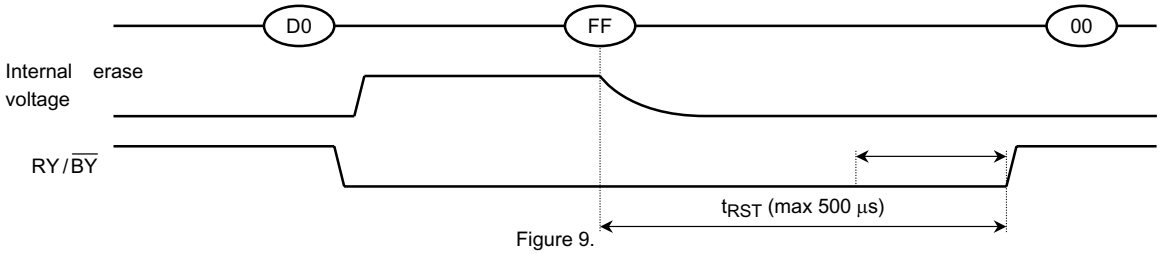


Figure 9.

When a Reset (FFH) command is input during Read operation

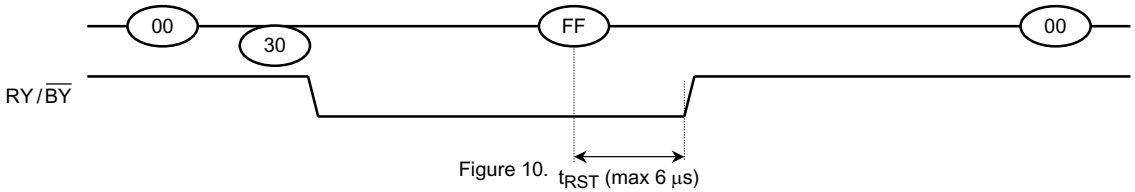
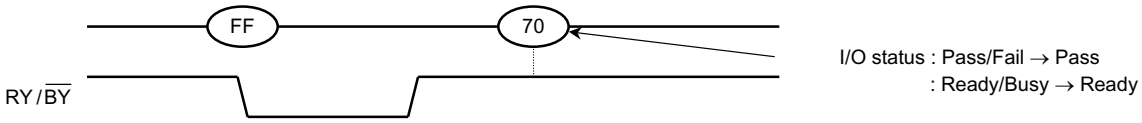


Figure 10.

When a Status Read command (70H) is input after a Reset



When two or more Reset commands are input in succession

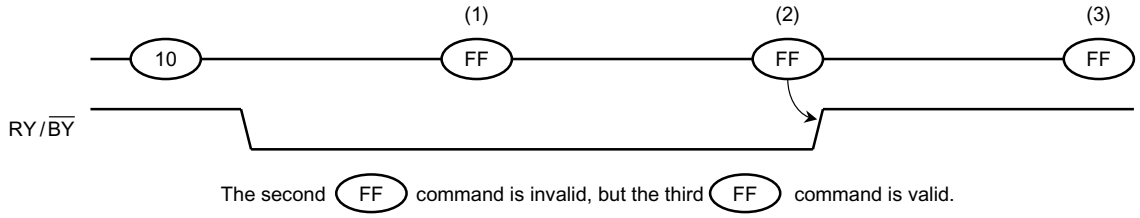


Figure 12.

APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The timing sequence shown in Figure 15 is necessary for power-on/off sequence.

The device internal initialization start after the power supply reaches appropriate level in power on sequence. During the initialization the device Ready/Busy signal outputs Busy state as shown in the Figure-15. In this time period, the acceptable commands are FFh or 70h.

The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off.

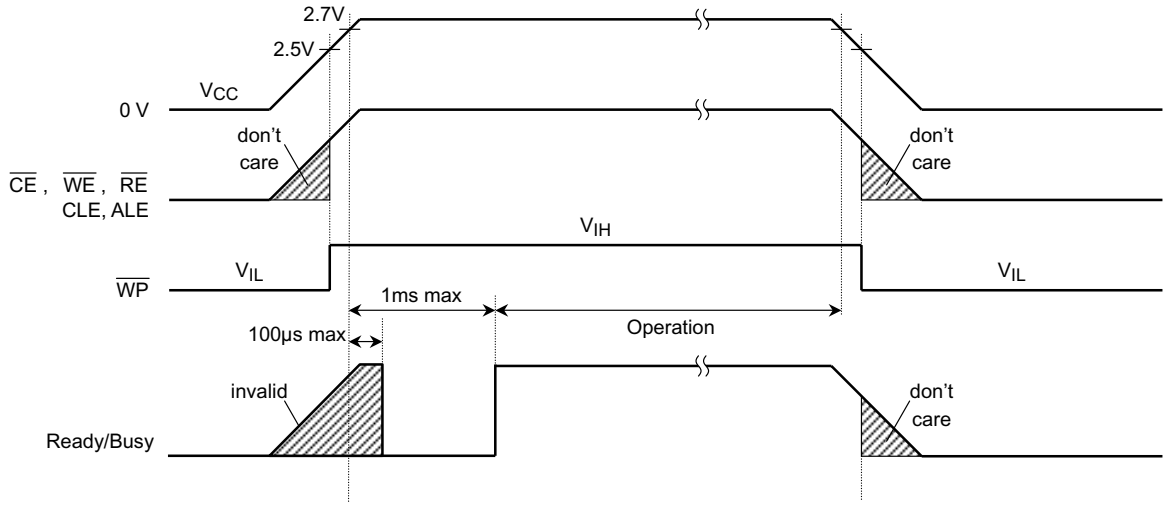


Figure 15. Power-on/off Sequence

(2) Status after power-on

The following sequence is necessary because some input signals may not be stable at power-on.

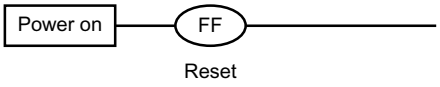


Figure 16.

(3) Prohibition of unspecified commands

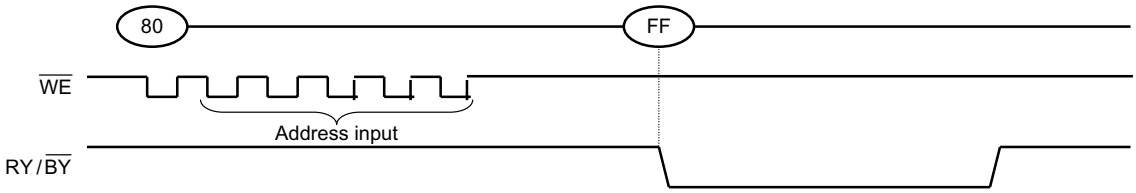
The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of command while Busy state

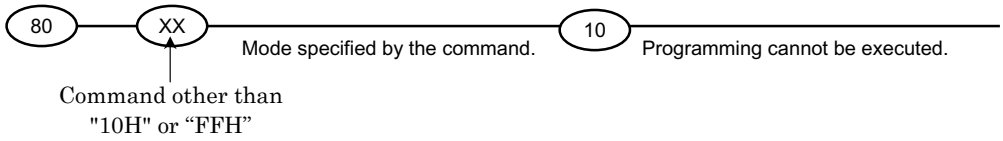
During Busy state, do not input any command except 70H, and FFH.

(5) Acceptable commands after Serial Input command "80H"

Once the Serial Input command "80H" has been input, do not input any command other than the Column Address Change in Auto Program command "10H" or the Reset command "FFH".



If a command other than "10H" or "FFH" is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies..



(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

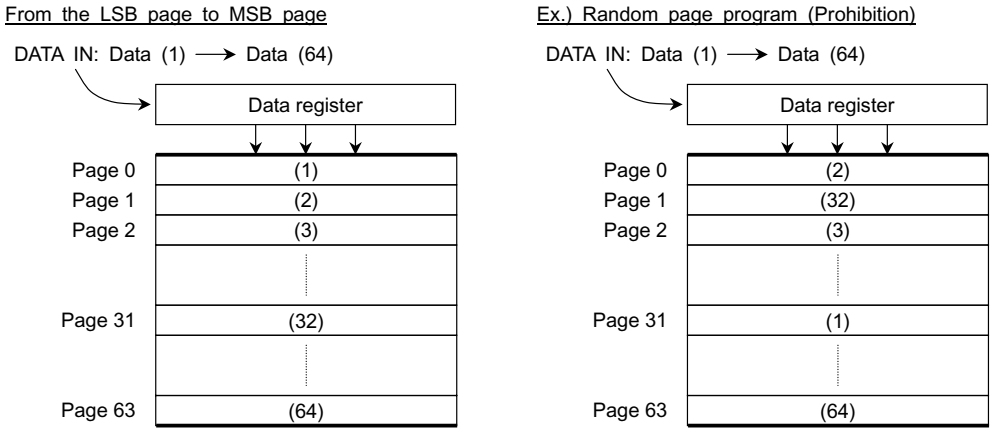


Figure 17. page programming within a block

(7) Status Read during a Read operation

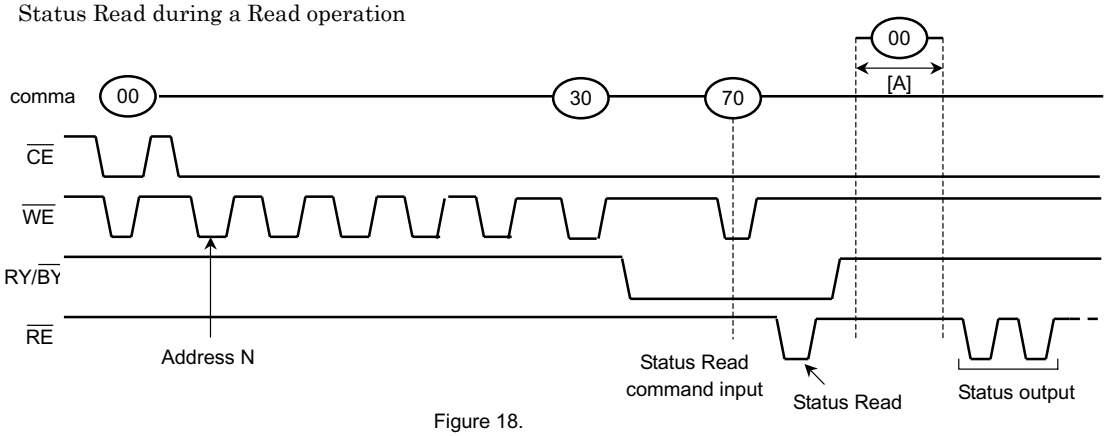


Figure 18.

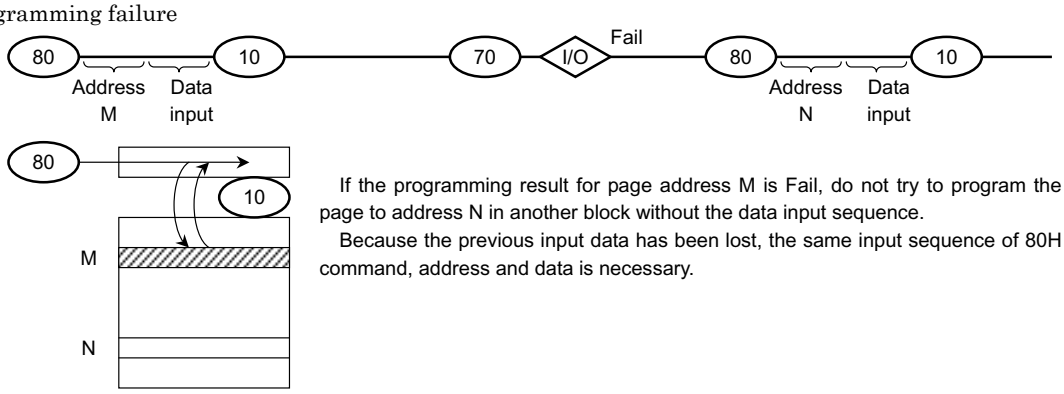
The device status can be read out by inputting the Status Read command "70H" in Read mode.

Once the device has been set to Status Read mode by a "70H" command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command "00H" is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

(8) Auto programming failure



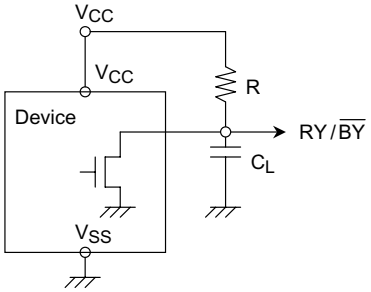
If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.

Because the previous input data has been lost, the same input sequence of 80H command, address and data is necessary.

Figure 19.

(9) RY / $\overline{BY}$: termination for the Ready/Busy pin (RY / $\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY / $\overline{BY}$ buffer consists of an open drain circuit.



This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

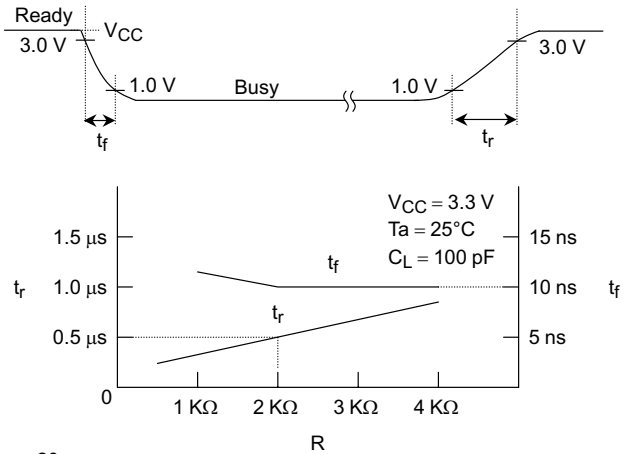
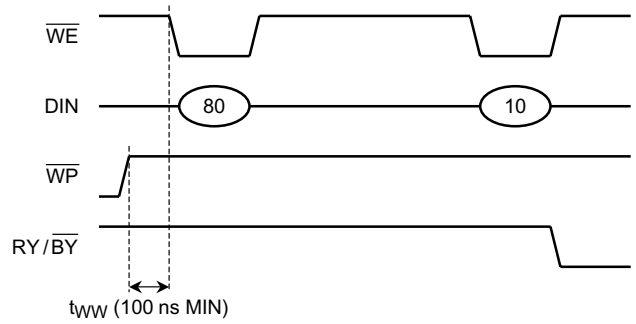


Figure 20.

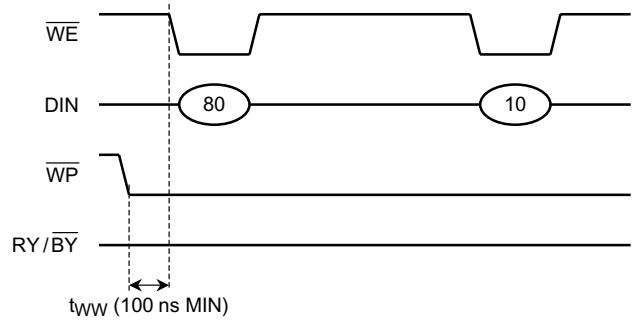
(10) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The operations are enabled and disabled as follows:

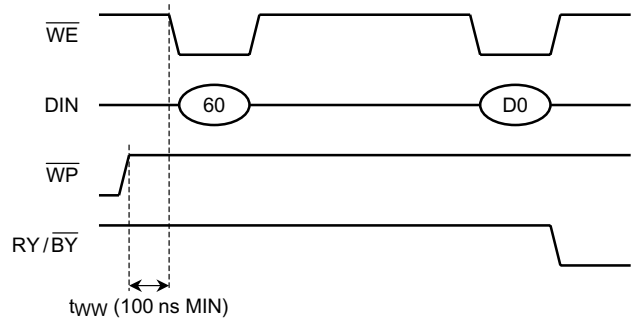
Enable Programming



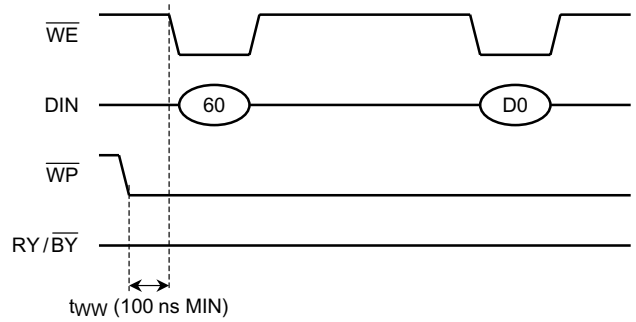
Disable Programming



Enable Erasing



Disable Erasing



(11) When six address cycles are input

Although the device may read in sixth address, it is ignored inside the chip.

Read operation

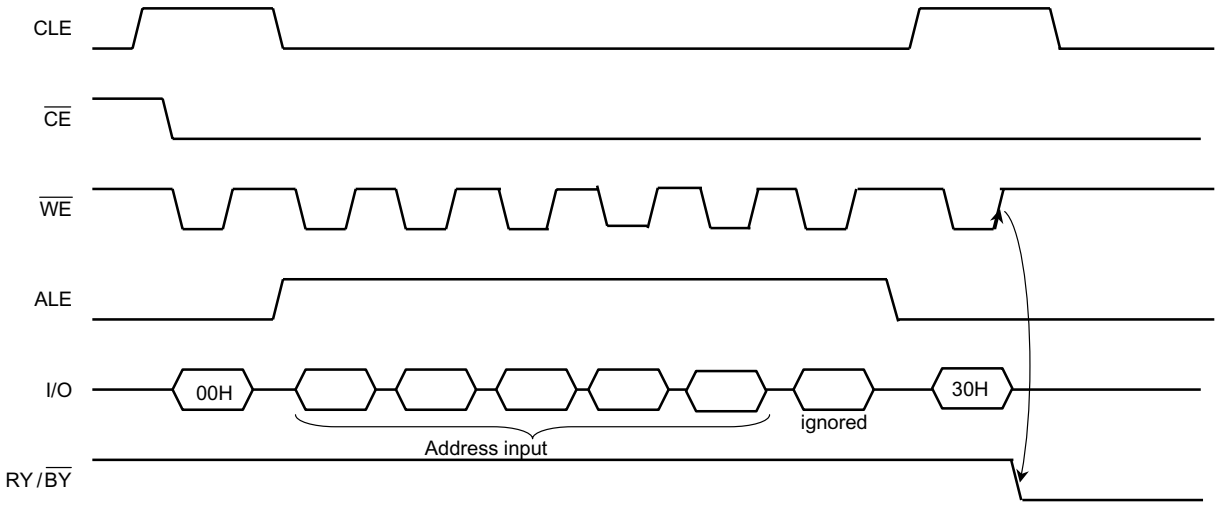


Figure 22.

Program operation

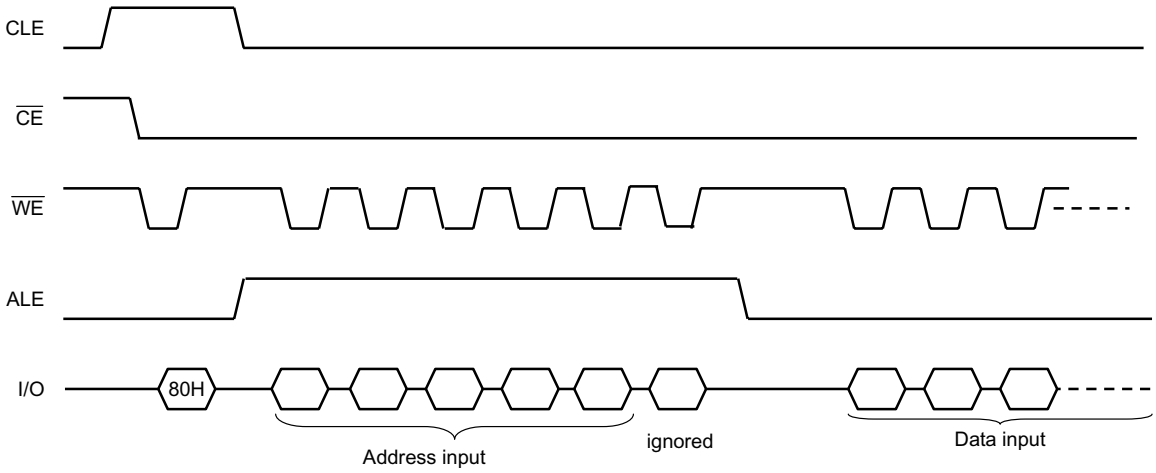


Figure 23.

(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 8 segments as follows :-

Data area (column address 0 to 2047) : 512 bytes x 4 segments
- 1st segment: column address 0 to 511
- 2nd segment: column address 512 to 1023
- 3rd segment: column address 1024 to 1535
- 4th segment: column address 1536 to 2047

Redundant area (column address 2048 to 2111) : 16 bytes x 4 segments
- 1st segment: column address 2048 to 2063
- 2nd segment: column address 2064 to 2079
- 3rd segment: column address 2080 to 2095
- 4th segment: column address 2096 to 2111

. Each segment can be programmed individually as follows:

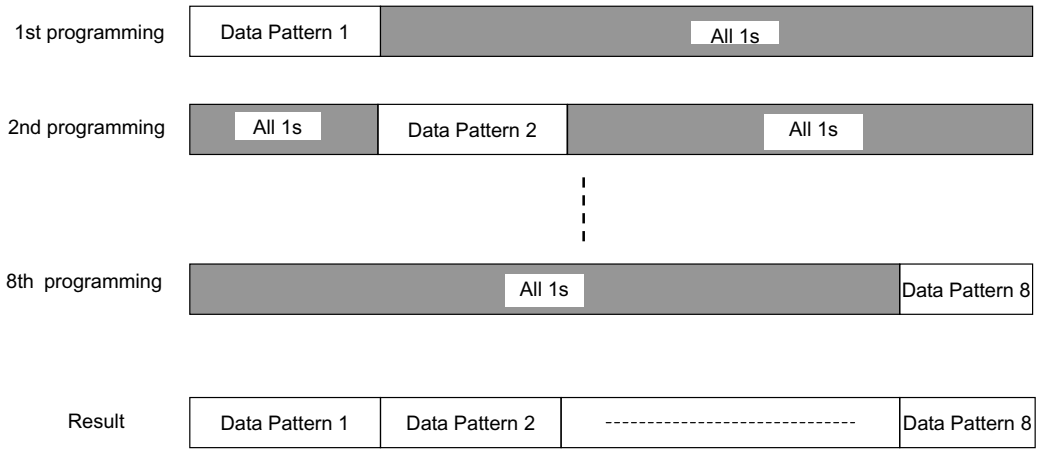


Figure 24.

Note: The input data for unprogrammed or previously programmed page segments must be "1"
(i.e. the inputs for all page bytes outside the segment which is to be programmed should be set to all “1”).

(13) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:

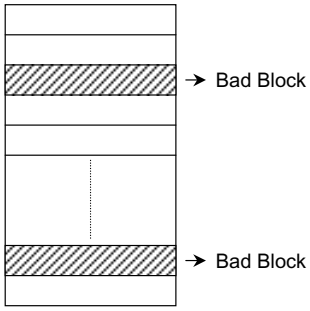


Figure 26.

At the time of shipment, all data bytes in a valid block are FFH. For bad blocks, all bytes are not in the FFH state. Please don't perform erase operation to bad blocks.

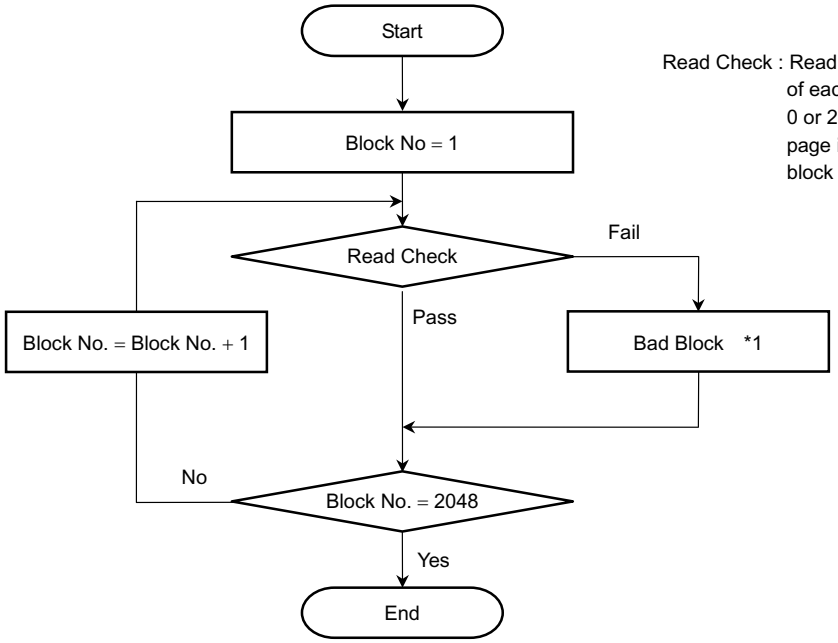
Check if the device has any bad blocks after installation into the system. Figure 27 shows the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the bit line by the select gate

The number of valid blocks at the time of shipment is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	2008	-	2048	Block

Bad Block Test Flow



Read Check : Read the 1st page or the 2nd page of each block. If the column address 0 or 2048 of the 1st page or the 2nd page is not FF (Hex), define the block as a bad block.

*1 : No erase operation is allowed to detected bad blocks

Figure 27.

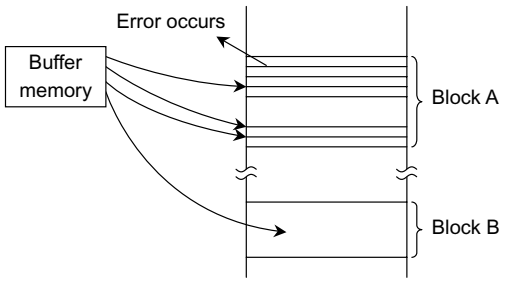
(14) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENIE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure " 1 to 0 "	(1) Block Verify after Program → Retry (2) ECC

- ECC : Error Correction Code .
- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Figure 28.

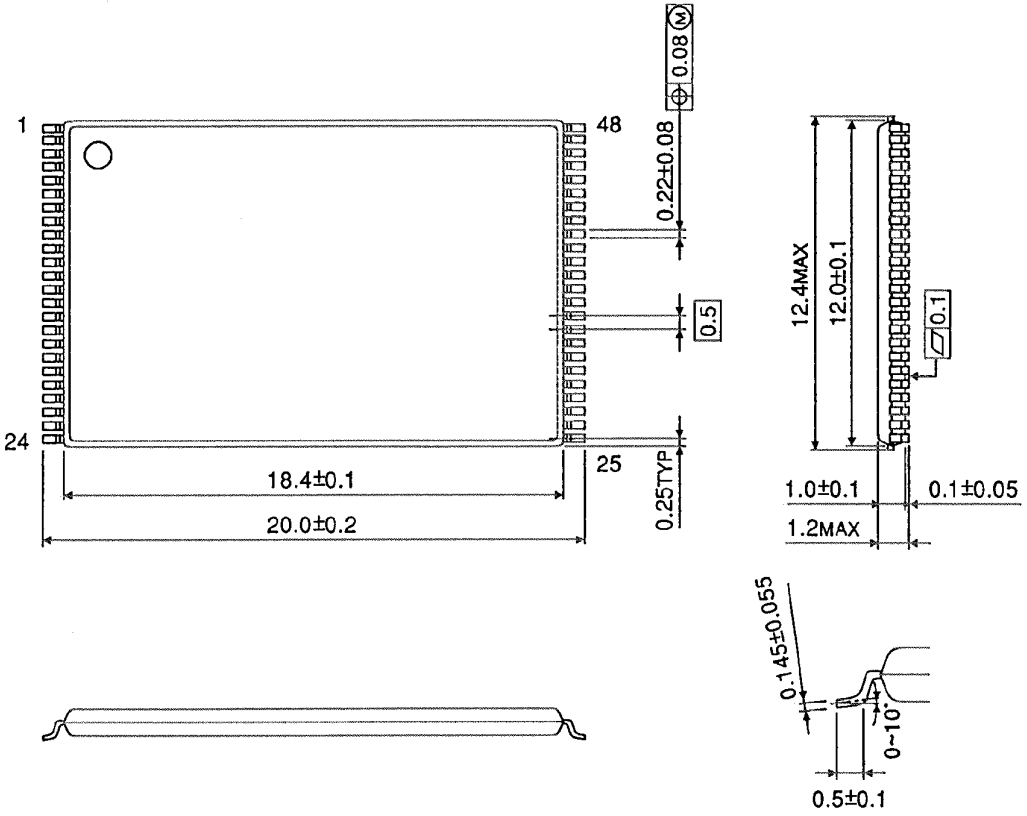
Erase

When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(15) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

Package Dimensions

TSOPI48-P-1220-0.50 Unit: mm



Weight: 0.53 g (typ.)