Melexis
Microelectronic Integrated Systems

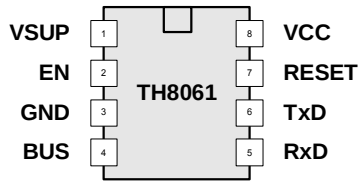
TH8061

LIN Bus Transceiver with integrated Voltage Regulator

Features and Benefits

Pin Diagram

SOIC8NB



- LIN-Bus Transceiver:
  - PNP-bipolar transistor driver with slew rate control and current limitation
  - BUS input voltage -24V ... 30V (independently of V_{SUP})
  - Possibility of BUS wake up
  - Baud rate up to 20 kBaud
- Operating voltage V_{SUP} = 5.5 ... 18 V
- Very low standby current consumption < 110 µA in normal mode (< 50 µA in sleep mode)
- Linear low drop voltage regulator:
  - Output voltage 5V± 1%
  - Output current max. 50mA
  - Output current limitation
- Overtemperature shutdown
- Reset time 100ms and reset threshold voltage 4.65V
- Load dump protected (40V)
- Wake-up by LIN BUS traffic and start-up capable independent of EN voltage level
- CMOS compatible interface to microcontroller

Ordering Information

Part No.	***Temperature Range***	***Package***
TH8061 JDC	-40ºC...125ºC	SOIC8, 150mil

General Description

The mini-ReLIN TH8061 is the low cost variant of our ReLIN-IC TH8060.

It consists a low drop voltage regulator 5V/50mA and a LIN Bus Transceiver. The LIN-Transceiver is suitable for LIN-Bus systems conform to “LIN-Protocol Specification” Rev.1.1. from 04/17/2000.

The combination of voltage regulator and bus transceiver make it possible to develop simple, but powerful and cheap slave nodes in LIN Bus systems.

Functional Diagram

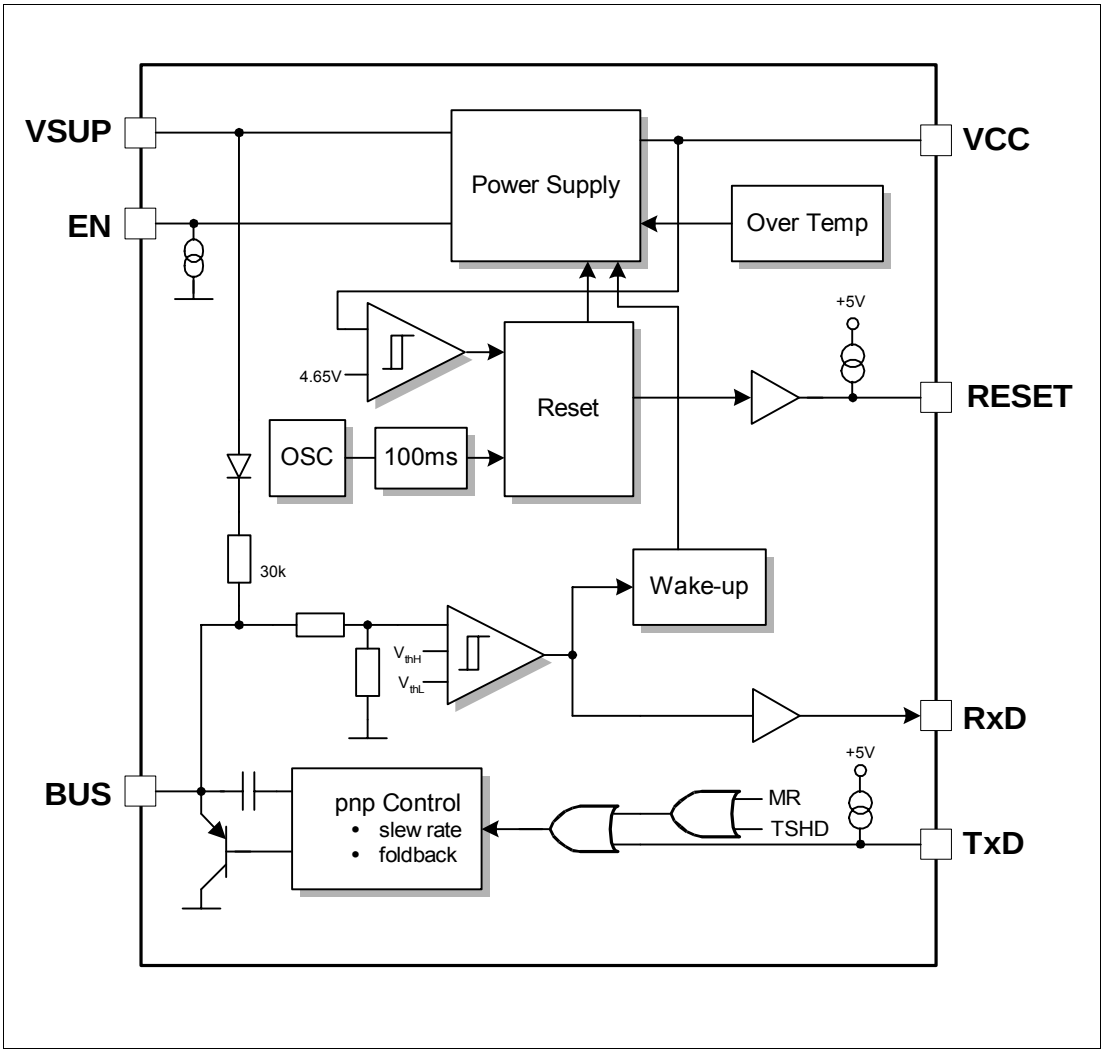


Figure 1 - Block Diagram

Functional Description

The TH8061 consists a low drop voltage regulator 5V/50mA and a LIN Bus transceiver, which is a bi-directional bus interface device for data transfer between LIN-Bus and the LIN protocol controller.

LIN-BUS Transceiver

The TH8061 is a bi-directional bus interface device for data transfer between LIN-Bus and the LIN protocol controller.

The transceiver consists a pnp-driver (1.2V@40mA) with slew rate control and fold-back characteristic and consists as well in the receiver a high voltage comparator followed by a debouncing unit.

The BUS pin has an integrated 30k pull up resistor with a diode, which prevent the reverse current of VBUS during differential voltage between VSUP and BUS (V_{BUS}>V_{SUP}).

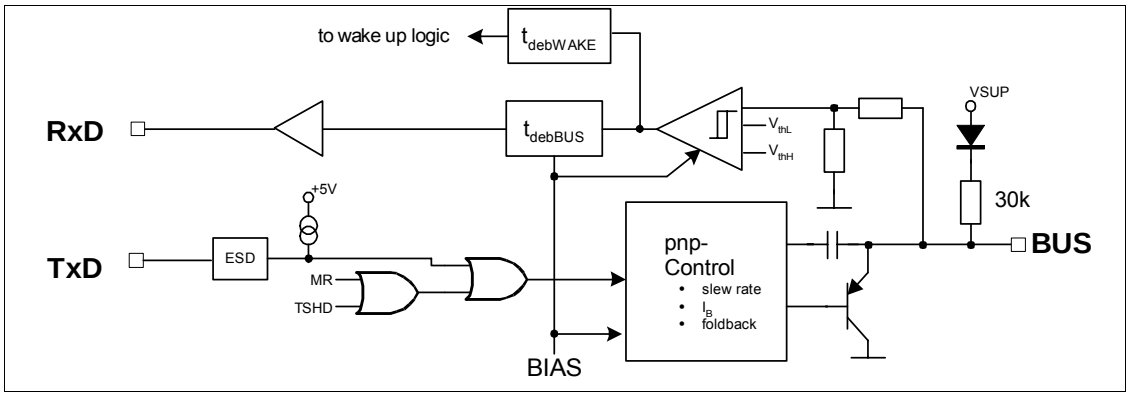


Figure 2 - Block Diagram LIN Bus Transceiver

Transmit Mode

During the transmission the data at the pin TxD will be transferred to the pin BUS. To minimize the electromagnetic emission of the bus line, the TH8061 has an integrated slew rate control.

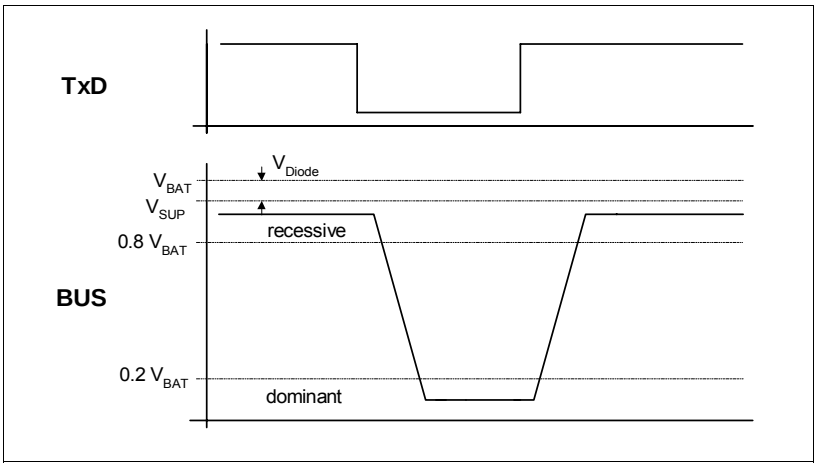


Figure 3 - Transmit Mode Pulse Diagram

Receive Mode

The data at the pin BUS will be transferred to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit.

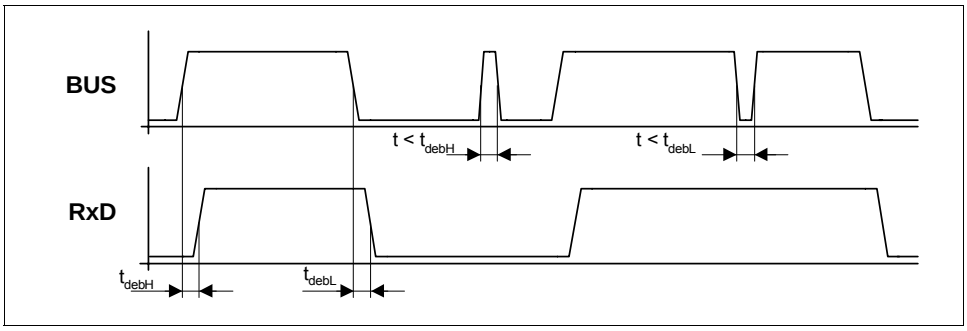


Figure 4 - Block Diagram LIN Bus Transceiver

Linear Regulator and Controlling Functions

Regulator

The TH8061 has an integrated linear regulator with an output voltage of 5V ±2% and an output current of ≤50mA. The regulator is switched on or off with a signal on the EN pin or wake up with a BUS signal.

Initialization

The initialization is started if the power supply is switched on, or after the temperature limitation has switched off the regulator or in case of BUS traffic (wake up).

If the V_{CC} voltage level is higher than V_{RES}=4.65V, the reset time t_{RES} = 100ms is started. After t_{RES} a rising edge on the RESET output is generated (see figure Initialization).

If V_{CC}>V_{POR} the bus-interface will be activated.

The regulator is active and can only switched off with a falling edge on EN. The regulator remain with EN=high in active mode and therefore also the V_{CC} voltage is active.

The input EN has an internal pull down resistor. If EN=high, the internal pull down current is switched off to minimize the quiescent current.

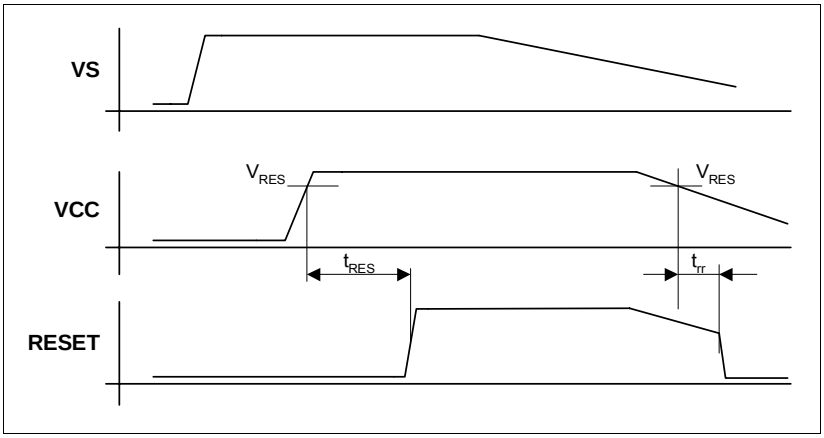


Figure 5 - Initialization and Undervoltage

RESET Output

The RESET output is switched from low to high if V_{SUP} is switched on and V_{CC}>V_{RES} after the time t_{RES}.

If the voltage V_{CC} drop below V_{RES} then the RESET output is switched from high to low after the time t_{rr} has been reached.

The voltage level for the RESET output is 4,65V and the corresponding reset time t_{RES} is 100ms.

Wake up with BUS traffic

If the regulator is put in standby mode it can be wake up with the BUS interface. Every pulse on the BUS (high pulse or low pulse) with a pulse width of min. 45µs will switch on the regulator.

After the BUS has wake up the regulator, it can only be switched off with a high level followed by a low level on the EN pin.

Temperature Limitation

If the Junction temperature 150ºC < T_j < 170ºC the over temperture recognition will be active and the regulator voltage will be switched off. After T_j fall below 140ºC the TH8061 will be initialized, not depending on of the voltage levels on EN and BUS.

The function of the TH8061 is possible between T_{Amax} and the switch off temperature, but small parameter differences can appear.

Application Hints

Operating during Disturbances

The absence of V_{SUP} ,V_{CC} or GND connection or ground shift either alone or in any combination, do not influence or disturb the communication between other bus nodes.

Undervoltage

The reset unit secures the correct behavior of the driver during undervoltage. The BUS pin generates the recessive state if $V_{CC} < V_{POR}$. The inputs have pull-up or pull-down characteristics.

With $4.5V \leq V_{CC} \leq 5.25V$ the bus connection operates within the correct parameters .

If $V_{CC} \leq 4.5V$ the TxD signal is transmitted to the bus. The receive mode is also activ.

Regulator Circuitry

The choice and dimension of the capacitor on VCC is determined by application point of view. Important parameters are the current difference on load changes and the maximum short time voltage drop.

The VCC pin must be connected to a min. 2µF capacitor for stable operating of the regulator in the whole operating range.

Short Circuit Proof

All in- and outputs are short circuit proof to battery and ground. A thermal shut down circuit prevent VCC and BUS from any damage

Baud Rate

The TH8061 has a maximum Baud rate of 20 kBaud (C_{BUS}<10nF). This baud rate is supported by the typically value for the slew rate at BUS of ± 2V/µs.

Application Circuitry

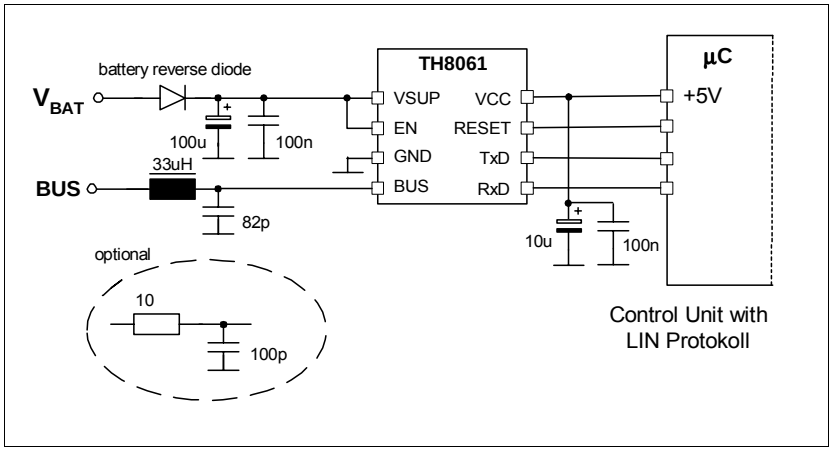


Figure 6 - Application Circuit

There should be used an LC-Filter to minimize the influence of EMI on the BUS lines.

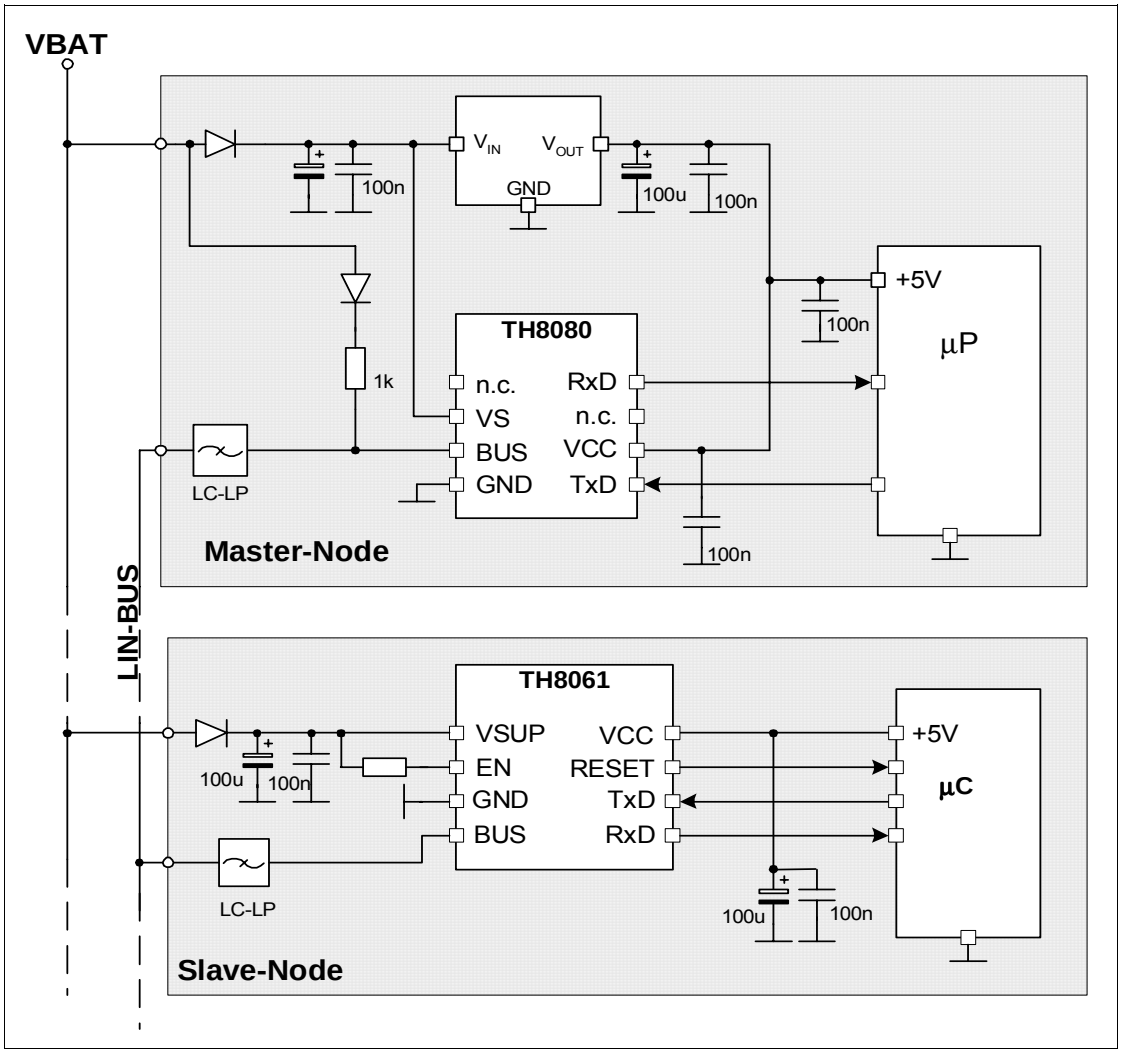


Figure 7 - Application Circuit for LIN Subbus

Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the TH8061 is only specified within the limits shown in ”Operating conditions”.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery voltage	V_{SUP}	5.25	18	V
Supply voltage	V_{CC}	4.75	5.25	V
Operating ambient temperature	T_A	-40	+125	°C
Junction temperature [1]	T_{Jc}		+150	°C

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at VSUP [2]	V_{SUP}		-1.0	18	V
		$T \leq 60$ s	-	30	
		$T \leq 500$ ms	-	40	
Input voltage at pin BUS [2]	V_{BUS}		-24	30	V
		$T \leq 500$ ms	-	40	
Difference VSUP-VCC	$V_{SUP-VCC}$		-0.3	40	V
Input voltage at pin EN	V_{INEN}		-0.3	V_{SUP}+0.3	V
Input voltage at pin TxD, RxD, RESET	V_{IN}		-0.3	V_{CC}+0.3	V
Input current at pin EN, TxD, RxD, RESET	I_{IN}		-25	25	mA
Input current for short circuit of pin VSUP and VCC	I_{INSH}		-500	500	mA
Power dissipation T_A = 85 °C [3]	P_0			400	mW
Thermal resistance from junction to ambient	R_{THJA}			160	K/W
Junction temperature [4]	T_J			150	°C
Storage temperature	T_{STG}		-55	150	°C

[1] Junction temperature is defined in IEC 747-1
[2] The current and voltage values are valid independent from each other.
[3] The maximum power dissipation is defined by the ambient temperature and the thermal resistance. It can be calculated with $P_0 = (V_{SUP}-V_{CC})*I_{VCC}+P_{BUS}$. P_{BUS} is the BUS driver output with normally ≤25 mW
[4] see over temperature protection

Static Characteristics

(V_{SUP} = 5.25 to 18V, V_{CC}= 4.75 to 5.25V, T_A = -40 to +125°C, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Linear Regulator						
Output voltage VCC	V_{CCn}	5.5V ≤ V_{SUP} ≤ 18V T_A = 25°C	4.95	5.0	5.05	V
	V_{CCt}	5.5V ≤ V_{SUP} ≤ 18V	4.90	5.0	5.10	V
	V_{CCh}	V_{SUP} > 18V	4.95	5.0	5.25	V
	V_{CCl}	3.3 V< V_{SUP}< 5.5 V	V_{SUP}-V_D		5.1	V
Supply current, „normal mode“	I_{Snl}	V_{EN} = V_{SUP} = 12V, Pins 4 to 8 open			110	µA
Supply current, „sleep mode“	I_{Ssleep}	V_{EN} = 0V		35	50	µA
Drop-out voltage	V_D	V_{SUP} ≥ 4.0V, I_{VCC} = 20mA			200	mV
		V_{SUP} ≥ 4.0V, I_{VCC} = 50mA			400	mV
		V_{SUP} ≥ 3.3V, I_{VCC} = 15mA			600	mV
Output current VCC	I_{VCC}	V_{SUP} ≥ 3.0V	50			mA
Current limitation VCC	I_{LVCC}	V_{SUP} > 0V			150	mA
Load capacity	C_{load}	ESR ≤ 5Ω	2			µF
Reset threshold	V_{RES}	refered to V_{CC}, V_{SUP} > 4.6V	4.5	4.65	4.8	V
Power-on-reset threshold	V_{POR}		3.0	3.15	3.3	V
Enable-Input EN						
Input voltage low	V_{ENL}		-0.3		1.75	V
Input voltage high	V_{ENH}		2.5		V_{SUP} +0.3	V
Hysteresis	V_{ENHYS}		100			mV
Pull-down current EN	I_{pdEN}	V_{EN} > V_{ENH}	1.8	4.0	7.5	µA
		V_{EN} < V_{ENL}	70	100	130	µA
Output RESET						
Output voltage low	V_{OL}	I_{OUT} = 1 mA, V_{SUP} > 5.5 V			0.8	V
		10 kΩ RESET to VCC V_{SUP} = V_{CC} = 0.8 V			0.2	V
Pull-up current	I_{pu}		-500	-375	-250	µA

Static Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LIN-Bus-Interface						
Pull-up current TxD	I_{pu}		-500	-375	-250	µA
Input voltage low TxD	V_{IL}				0.25	V_{CC}
Input voltage high TxD	V_{IH}		0.75			V_{CC}
Input voltage low BUS dominant	V_{IL}				0.45	V_{SUP}
Input voltage high BUS recessive	V_{IH}		0.55			V_{SUP}
Hysteresis BUS	V_{HYS}			50		mV
Input current BUS recessive	I_{INBUSR}	$8 \le V_{BUS} \le 18$ V, $V_{SUP} = V_{BUS}$ - 0.7V, TxD = high			20	µA
Input resistance	R_{INBUSR}	V_{BUS} = -12 V	12	60		kΩ
Input current BUS dominant	I_{INBUSD}	V_{BUS} = 0V, TxD = high	-1			mA
Pull up resistor bus	R_{BUSpu}		20	30	47	kΩ
Output voltage BUS dominant	V_{BUSD}	V_{SUP} = 12V, TxD = low I_{BUS} = 40 mA			1.2	V
Output voltage BUS recessive [1]	V_{BUSR}	$8 \le V_{SUP} \le 18$ V, TxD = high			0.8	V_{BAT}
Current limitation BUS	I_{LIM}	V_{BUS} > 2.5V, TxD = low	40		100	mA
Output voltage low RxD	V_{OL}	I_{OUT} = 1 mA			0.8	V
Output voltage high RxD	V_{OH}	I_{OUT} = -1 mA	V_{CC}-0.8			V
Temperature switch off						
Switch off temperature	T_{jab}		150		170	°C
Hysteresis switch on temerature	T_{jhys}		10		30	°C

[1] The recessive voltage at pin BUS don't should be less than 80% of voltage at KL30 $V_{BAT.}$ The voltage at V_{SUP} results with consideration of reverse diode $V_{SUP} = V_{BAT}$ - 0,7V

Dynamic Characteristics

All dynamic values of the table below refer to the test-schematic schown in Figure 9...12 - Test Circuit for Dynamic Characteristics. For the definition of delay and transitions times see Figure 8 - TH8061 Timing Diagram.

(7V ≤ V_{SUP} ≤ 18V, 4.75V ≤ V_{CC} ≤ 5.25V, -40°C ≤ T_A ≤ 125°C, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
RESET						
Reset time	t_{Res}		70	100	140	ms
Reset rising time	t_{rr}		3.0	6.5	10	µs
LIN-Bus-Interface						
Slew rate BUS falling edge [2]	dV/dT_{fall}	20% ≤ V_{BUS} ≤ 80% 100pF ≤ C_{BUS} ≤ 10nF	-2.5	-2.0	-1.0	V/µs
Slew rate BUS rising edge [2]	dV/dT_{rise}	20% ≤ V_{BUS} ≤ 80% C_{BUS} = 100 pF	1.0	2.0	2.5	V/µs
Symmetry of Slew rate BUS [1]	dV/dT_{sym}	dV/dT_{rise} - dV/dT_{fall} C_{BUS} = 100 pF	-0.3		0.3	V/µs
Debouncing time BUS	t_{debBUS}	Hig pulse or low pulse	1.5	2.8	4.0	µs
Symmetry of debouncing BUS	t_{debsym}		-0.5		0.5	µs
Propagation delay TxD -> BUS [1] [2]	t_{trans_pdr}, t_{trans_pdf}				4	µs
Symmetry of propagation delay TxD -> BUS [1]	t_{trans_sym}	t_{trans_pdr} - t_{trans_pdf}	-2		2	µs
Propagation delay BUS -> RxD [1] [2]	t_{rec_pdr} t_{trec_pdf}				6	µs
Symmetry of propagation delay BUS -> RxD [1]	t_{rec_sym}	t_{rec_pdr} - t_{rec_pdf}	-2		2	µs
Debouncing time TxD [1]	t_{deb}		0.6	1.0	1.5	µs
Debouncing time EN [1]	t_{deb}		200			ns
Wake-up-debouncing BUS	$t_{debWake}$		25	45	90	µs

[1] See timing diagram
[2] See test circuit for dynamic characteristics on page 12 and 13

Timing Diagram

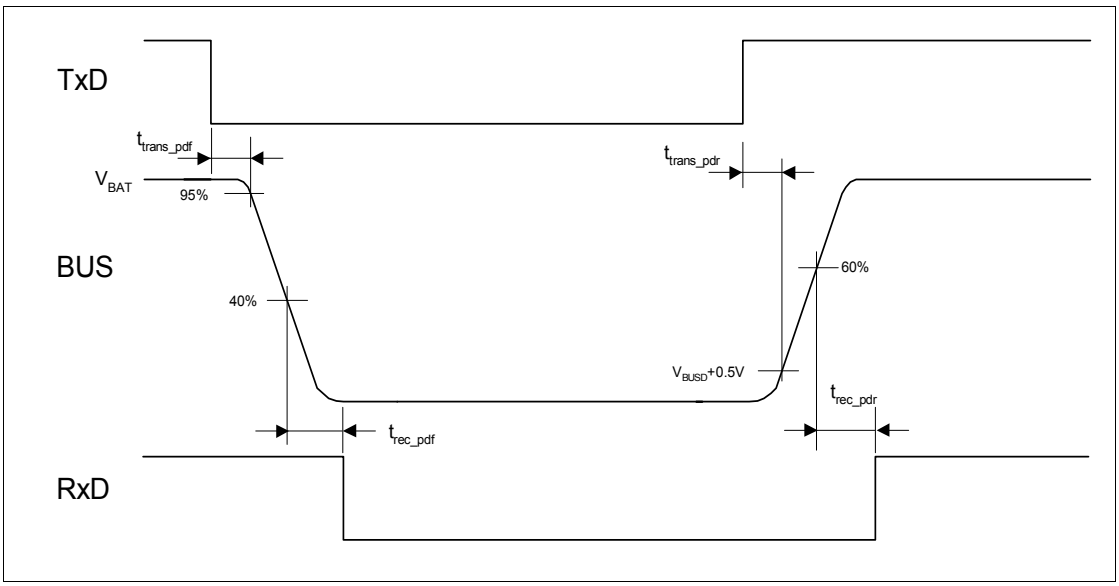


Figure 8 - Timing Diagram

Test Circuit for Dynamic and Static Characteristics

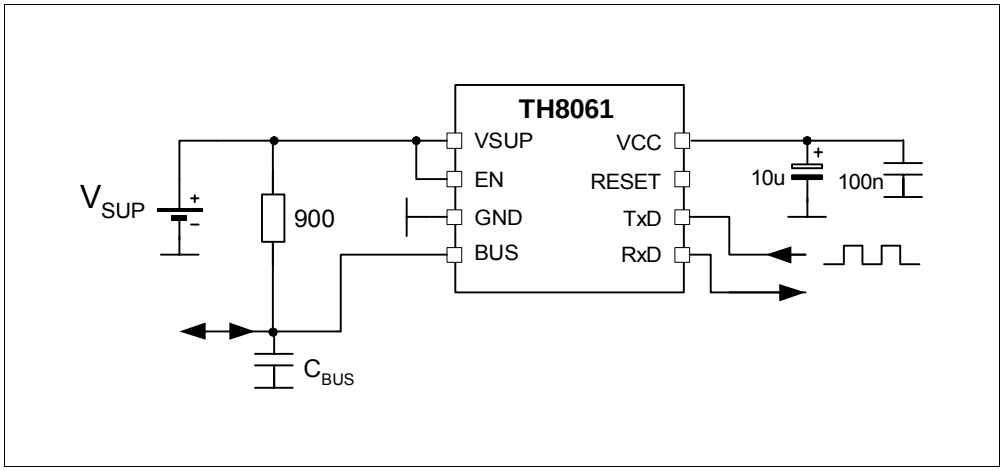


Figure 9 - Test Circuit for Delay Time and Slope Control

Test Circuit for Dynamic and Static Characteristics (continued)

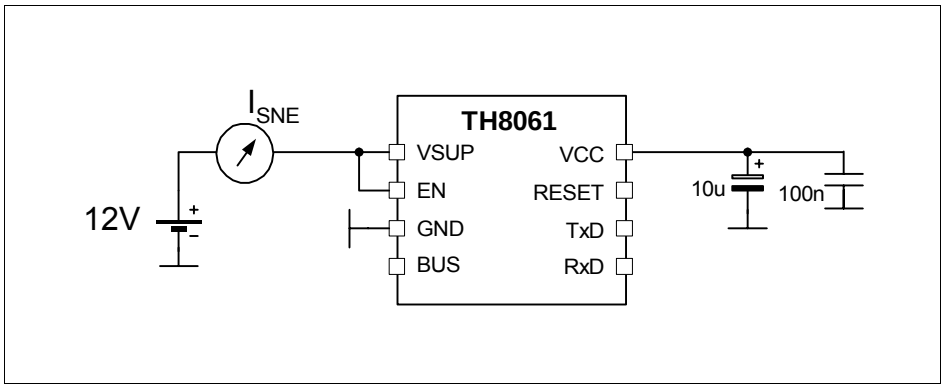


Figure 10 - Test Circuit for Supply Current I_{SNE}

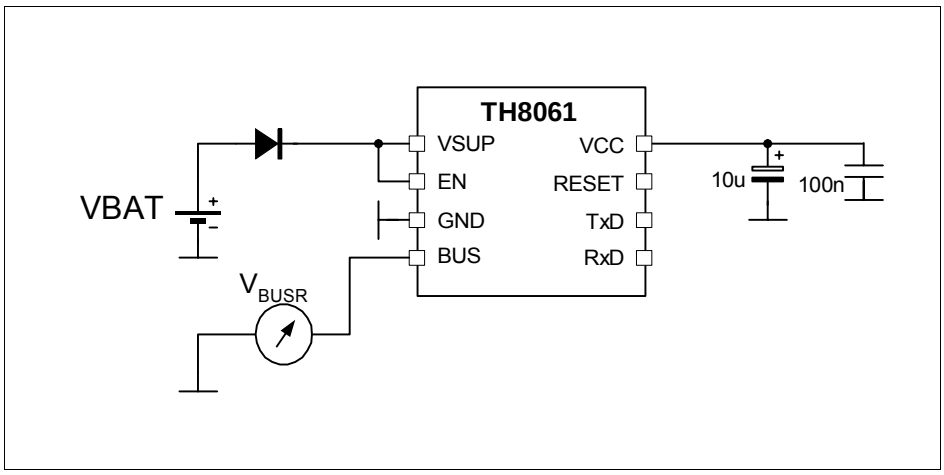


Figure 11 - Test Circuit for Bus Voltage "recessiv" V_{BUSR}

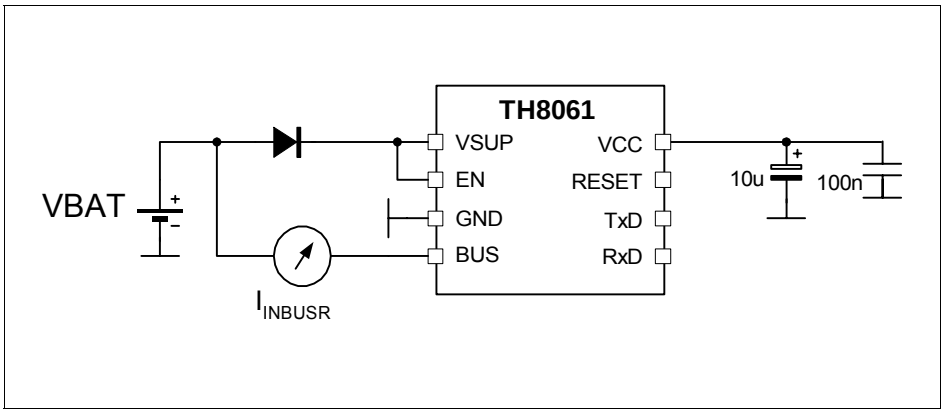
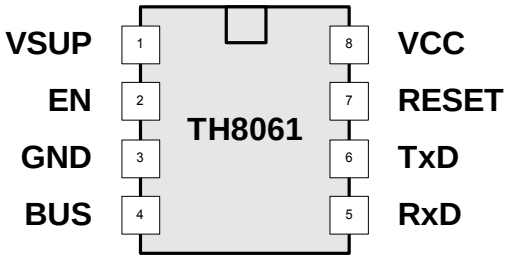


Figure 12 - Test Circuit for Bus Current "recessiv" I_{BUSR}

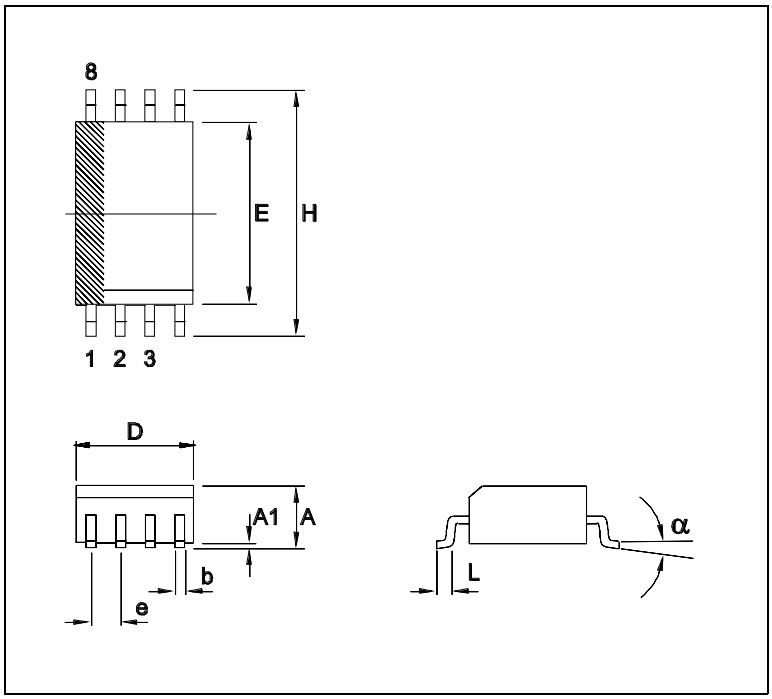
Pin Description



Pin	Name	I/O	Function
1	VSUP		Supply voltage
2	EN	I	Enable Input voltage regulator, HV-pull-down-Input, High-active
3	GND		Ground
4	BUS	I/O	Bi-directional bus line
5	RxD	O	Receive Output, 5V-push-pull
6	TxD	I	5V-Transmit Input, pull-up-Input
7	RESET	O	5V-output reset, active low
8	VCC	O	Regulator output 5V/50mA

Mechanical Specifications

SOIC8 Package Dimensions



Small Outline Integrated Circiut (SOIC), SOIC 8, 150 mil

All Dimension in mm, coplanarity < 0.1 mm									
	D	**E**	**H**	**A**	**A1**	**e**	**b**	**L**	**α**
min	4.8	3.80	5.80	1.35	0.10	1.27	0.33	0.40	0°
max	5.00	4.00	6.20	1.75	0.25		0.51	1.27	8°
All Dimension in inch, coplanarity < 0.004”									
min	0.189	0.150	0.228	0.053	0.004	0.050	0.013	0.016	0°
max	0.197	0.157	0.244	0.069	0.010		0.020	0.050	8°

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