TH8065

Voltage Regulator with LIN Transceiver and Watchdog

Features

- Compatible to LIN Specification 2.0 and SAE J2602
- Operating voltage V_S = 6 ... 18 V
- Low standby current consumption of typ. 15 µA in sleep mode
  - "noload" current < 200µA
- Linear low drop voltage regulator 5V/70mA ±2%
  - Output current limitation
- LIN-Bus Transceiver
  - Compatible to ISO9141 functions
  - Baud rate up to 20 kBaud
  - Slew rate control for best EME behavior
  - Low slew mode for optimized SAE J2602 transmission
  - High EMI immunity
  - High signal symmetry for using in RC – based slave nodes up to 2% clock tolerance
  - Current limitation
- Wake-up via LIN bus traffic
- Reset output (default 8ms/4.65V)
  - Reset time adjustable to 4ms, 15ms and 30ms during IC final test
- Analogue Watchdog with programmable time constant via external capacity
- Over temperature shutdown
- Automotive temperature range of –40°C to 125°C
- CMOS compatible interface to microcontroller
- Load dump protected (40V)
- Small SOIC14 package with fused lead frame for low Rth value

Ordering Information

Part No.	Temperature Range	Package	Version	POR time
TH8065 KDC AA	K (-40 to 125 °C)	DC (SOIC14NB)	A	A (8ms)
On Request				
TH8065 KDC AB	K (-40 to 125 °C)	DC (SOIC14NB)	A	B (4ms)
TH8065 KDC AC	K (-40 to 125 °C)	DC (SOIC14NB)	A	C (30ms)
TH8065 KDC AD	K (-40 to 125 °C)	DC (SOIC14NB)	A	D (15ms)

General Description

The TH8065 consists of a low-drop voltage regulator 5V/70mA combined with a Reset/Watchdog unit and a LIN bus transceiver. The LIN transceiver is suitable for LIN bus systems conform to LIN specification revision 2.0 and SAE J2602.
The combination of voltage regulator and bus transceiver makes it possible to develop simple, but powerful and cheap slave nodes in LIN Bus systems.

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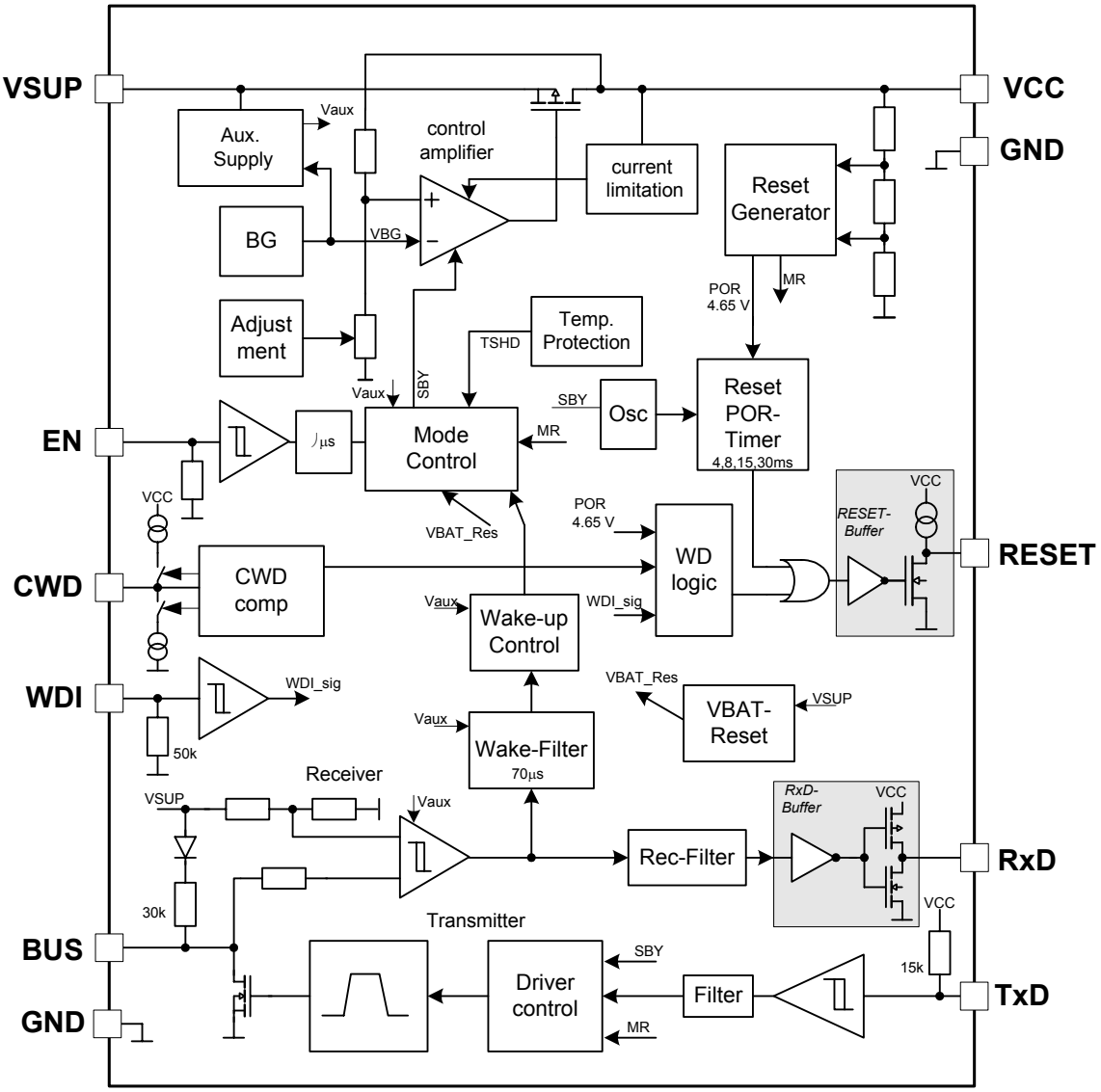


Figure 1 - Block diagram

2. Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.
The absolute maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Correct operating of the device cannot be guaranteed if any of these limits are exceeded.

2.1 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{SUP}	6	18	V
Output voltage	V_{CC}	4.85	5.15	V
Operating ambient temperature	T_A	-40	+125	°C
Junction temperature	T_J		+150	°C

2.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at VSUP	V_{SUP}		-1.0	18	V
		T ≤ 300 s	-	30	
		T ≤ 500 ms	-	40	
Input voltage at pin BUS	V_{BUS}		-24	30	V
		T ≤ 500 ms	-	40	
Difference VSUP-VCC	V_{SUP}-V_{CC}		-0.3	40	V
Input voltage at pin EN	V_{INEN}		-0.3	V_{SUP}+0.3	V
Input voltage at pin TxD, RxD, RESET, WDI, CWD	V_{IN}		-0.3	V_{CC}+0.3	V
Input current at pin EN, TxD, RxD, RESET, WDI, CWD	I_{IN}		-25	25	mA
Input current for short circuit of pin VSUP and VCC	I_{INSH}		-500	500	mA
ESD Capability on pin BUS, VBAT, GND	ESD_{BUSHB}	Human body Model, 100pF via 1.5kΩ	-4	4	kV
ESD Capability on pin TxD, RxD, EN, RESET, WDI, CWD, VCC	ESD_{BUSHB}	Human body Model, 100pF via 1.5kΩ	-2	2	kV
Power dissipation	P_0		Internal limited [1]		
Thermal resistance from junction to ambient (SOIC14fused) [2]	R_{THJA}			70	K/W
Junction temperature [3]	T_J			150	°C
Storage temperature	T_{STG}		-55	150	°C

[1] See chapter 4.1 Safe Operating Area
[2] SOIC14 with fused lead frame and an active copper area of >150sqmm
[3] See chapter 3.5 Overtemperature Shutdown

2.3 Static Characteristics

Unless otherwise specified all values in the following tables are valid for V_{SUP} = 6 to 18V and T_{AMB} = -40 to 125°C. All voltages are referenced to ground (GND), positive currents flow into the IC.

2.3.1. Voltage Regulator and Reset Unit

Parameter	Symbol	Condition	Min	Typ	Max	Unit	T[1]
VSUP							
Operating voltage	V_{SUP}		6	12	18	V	B
Supply current, VCC „noload“ [2]	I_{Snl}	$V_{EN} = V_{SUP}$ = 13V, C_{WD}=1nF, BUS: 1k to VSUP, Pins TxD, RxD, WDI and RESET open, EN = V_{CC}		200	300	µA	A
Supply current, „sleep mode“	I_{Ssleep}	V_{SUP} = 13V, V_{EN} = 0V, BUS: 1k to VSUP		15	30	µA	A
V_{SUP} under voltage reset “off” threshold	V_{SUVR_OFF}	V_{SUP} ramp up	3.2	3.7	4.2	V	A
V_{SUP} under voltage reset “on” threshold	V_{SUVR_ON}	V_{SUP} ramp down	2.7	3.1	3.5	V	A
V_{SUP} under voltage reset hysteresis	V_{SUVR_HYS}		0.2			V	A
VCC							
Output voltage VCC	V_{CCn}	6V ≤ V_{SUP} ≤ 18V 1mA ≤ I_{LOAD} ≤ 70mA T_A = 25°C T_A = -40°C to 125°C	4.90 4.85	5.0	5.10 5.15	V	A
	V_{CCh}	18V ≤ V_{SUP} ≤ 40V I_{LOAD} = 10mA	4.80		5.25	V	A
Drop-out voltage [3]	V_{D10}	I_{VCC} = 10mA		75	120	mV	A
	V_{D30}	I_{VCC} = 30mA		220	350	mV	A
	V_{D70}	I_{VCC} = 70mA		500	800	mV	A
Line regulation	V_{LNR}	6V ≤ V_{SUP} ≤ 18V			20	mV	A
Load regulation	V_{LDR10}	I_{LOAD} = 1mA → 10mA			50	mV	A
	V_{LDR30}	I_{LOAD} = 1mA → 30mA			90	mV	A
	V_{LDR70}	I_{LOAD} = 1mA → 70mA			150	mV	A
Output current limitation	I_{VCC_max}	V_{SUP} > 0V	80	130	200	mA	A
Ripple Rejection on VSUP	PSRR	V_{SUP} = 12V, f_i = 120Hz, V_{iP-P} = 1V, I_{LOAD} = 10mA		t.b.d		dB	

Parameter	Symbol	Condition	Min	Typ	Max	Unit	T[1]
Reset threshold - POR	$V_{RES(ON)}$	VCC ramp up, t > t_{rr}	4.4	4.6	4.8	V	A
Reset threshold – low voltage reset	$V_{RES(OFF)}$	VCC ramp down, t > t_{rr}	4.4	4.6	4.8	V	A
Vres Hysteresis $V_{RESHYS} = \lvert V_{RES(ON)} - V_{RES(OFF)} \rvert$	V_{RESHYS}				150	mV	A
Master reset threshold	V_{MRES}		3.0	3.15	3.3	V	D
Enable Input EN							
Input voltage low	V_{ENL}		-0.3		0.8	V	A
Input voltage high	V_{ENH}		2.0		V_{SUP} +0.3	V	A
Hysteresis	V_{ENHYS}		50		300	mV	A
Pull-down resistor EN low	R_{pdENL}	$0V \leq V_{EN} \leq 0.8V$	14	25	35	kΩ	A
Pull-down current EN high	I_{pdENH}	$V_{EN} \geq V_{ENL}$	0.5	2	10	µA	A
Output RESET							
Output voltage low	V_{OL1_RESET}	I_{OUT} = 1 mA, $V_{SUP} \geq 6$ V			0.8	V	A
Pull-up current	I_{pu}		-500	-375	-250	µA	A
Input CWD							
Input threshold low	V_{CWDL}		0.076	0.08	0.084	V_{CC}	A
Input threshold high	V_{CWDH}		0.342	0.36	0.378	V_{CC}	A
Pull up current (charge current)	I_{CWD_pu}	V_{IN} = 1V	7.6	13.9	20.2	µA	A
Pull down current (discharge current)	I_{CWD_pd}	V_{IN} = 1V	0.76	1.39	2.02	µA	A
Input WDI							
Pull down resistor	R_{pd_WDI}	$V_{IN} = V_{CC}$	35	50	73	kΩ	A
Input voltage low	V_{IL_WDI}				0.3	V_{CC}	A
Input voltage high	V_{IH_WDI}		0.7			V_{CC}	A
Thermal Protection							
Thermal shutdown	T_{JSHD}		155		180	°C	D
Thermal recovery	T_{JREC}		126			°C	D

[1] A = 100% serial test, B = Operating parameter, C = Only used for data characterization (cpk), D = Value guaranteed by design

[2] No active watchdog reset

[3] The nominal V_{CC} voltage is measured at V_{SUP} =12V. If the V_{CC} voltage is 100mV below its nominal value then the voltage drop is $V_D = V_{SUP} - V_{CC}$.

2.3.2. LIN Bus Interface

Parameter	Symbol	Condition	Min	Typ	Max	Unit	T[1]
General							
Pull up current BUS (recessive)	$I_{INBUSpu}$	V_{BUS} = 18 V, V_{SUP} = 6V			20	µA	A
Pull up resistor BUS	R_{BUSpu}	V_{SUP} = 12V, V_{BUS} = 0V	20	30	47	kΩ	A
Reverse current BUS (recessive)	$-I_{INBUSrev}$	V_{SUP} = 12V, V_{BUS} = 0V	-1			mA	A
Reverse current BUS (loss of battery)	I_{INBUS_lob}	V_{SUP} = 0V, 0V ≤ V_{BUS} ≤ 18V			20	µA	A
Reverse current BUS (loss of ground)	I_{INBUS_log}	V_{SUP}= 12V, 0V ≤ V_{BUS} ≤ 18V	-1		1	mA	A
Receiver							
Receive threshold	V_{thr_rec}, V_{thr_dom}	7.0 V ≤ V_{SUP} ≤ 18 V	0.4		0.6	V_{SUP}	A
Centre point of receive threshold $V_{thr\_cnt} = (V_{thr\_rec}+V_{thr\_dom})/2$	V_{thr_cnt}		0.475	0.5	0.525		A
Hysteresis of receive threshold $V_{thr\_hys} = V_{thr\_rec}-V_{thr\_dom}$	V_{thr_hys}			0.15	0.175		A
Transmitter							
Output voltage BUS (dominant)	V_{BUSdom_1}	I_{BUS} = 40mA			1.2	V	A
Current limitation BUS	I_{LIM}	V_{BUS} = V_{SUP}, TxD = 0V	41	120	200	mA	A
Input TxD							
Pull-up resistor	R_{pu_TxD}	V_{IN} = 0V	9.5	15	21	kΩ	A
Input voltage low TxD	V_{IL}				0.3	V_{CC}	A
Input voltage high TxD	V_{IH}		0.7			V_{CC}	A
Output RxD							
Output voltage Low RxD	V_{OL}	I_{OUT} = 1 mA			0.8	V	A
Output voltage High RxD	V_{OH}	I_{OUT} = -1 mA	V_{CC} - 0.8			V	A

[1] A = 100% serial test, B = Operating parameter, C = only used for data characterization (cpk), D = Value guaranteed by design

2.4 Dynamic Characteristics

6V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C, unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit	T[1]
RESET and Watchdog							
Reset time	t_{Res}	V_{SUP} = 12V,Vers. "A"	5.6	8	10.4	ms	A
		V_{SUP} = 12V,Vers. "B"	2.8	4	5.2	ms	A
		V_{SUP} = 12V,Vers. "C"	21	30	39	ms	A
		V_{SUP} = 12V,Vers. "D"	10.5	15	19.5	ms	A
Reset rising time	t_{rr}	V_{SUP} = 12V	3.0	6.5	12	µs	A
Discharge time CWD-capacity	t_{fCWD}	C_{WD} = 10nF, ΔV_{CWD} = 1V			5	µs	C
Watchdog period	t_{WD_per}	C_{WD} = 1nF ±1%	0.63	1.1	1.54	ms	A
Watchdog reset time	t_{WD_R}	C_{WD} = 1 nF ±1%	60	100	140	µs	A
Wake-up and Mode Select							
Wake up time	t_{wake_BUS}		30	70	150	µs	A
Debouncing time EN	t_{deb_EN}		2	6	15	µs	D
Propagation delay EN to sleep mode	$t_{pd\_EN\_sleep}$	EN = High to Low			400	µs	A
Propagation delay EN to normal mode	$t_{pd\_EN\_norm}$	EN = Low to High			400	µs	A
Setup time TxD to EN for low slew mode	$t_{set\_TxD\_LS}$	TxD = Low before EN = L/H	5			µs	B
Hold time TxD after EN for low slew mode	$t_{hold\_TxD\_LS}$	TxD = Low after EN = L/H	20			µs	B
General LIN Parameter							
Slew rate rising edge BUS	dV/dT_{rise}	Normal Mode BUS-Load: 1kOhm/1nF	0.8	1.5	2.5	V/µs	C
Slew rate falling edge BUS	dV/dT_{fall}		-2.5	-1.5	-0.8	V/µs	C
Slew rate rising edge BUS	dV/dT_{rise}	Low Slew Mode BUS-Load: 1kOhm/1nF	0.3	0.8	1.3	V/µs	C
Slew rate falling edge BUS	dV/dT_{fall}		-1.3	-0.8	-0.3	V/µs	C
Receiver debouncing time	t_{deb_BUS}		1.5	2.8	4.0	µs	C
Receiver propagation delay BUS->RxD	t_{dr_RxD} t_{df_RxD}	$C_{L(RXD)}$ = 50 pF			6	µs	A
Symmetry propagation delay BUS->RxD	t_{dsym_RxD}	t_{dr_RXD} - t_{df_RXD}	-2		2	µs	A
Internal capacity	C_{BUS}	Pulse at BUS via 10kOhm with 0/10 V; VSUP = open		25	35	pF	D

Parameter	Symbol	Condition	Min	Typ	Max	Unit	T[1]
LIN transceiver parameter according to LIN Physical Layer Spec. rev. 2.0, table 3.4 (20kbit/s)							
Conditions: Normal slew mode; V_{SUP} =7.0V to 18V; BUS loads: 1kΩ/1nF; 660Ω/6.8nF; 500Ω/10nF TxD signal: t_{Bit} = 50µs, $t_{wH} = T_{wL} = t_{Bit}$; $t_{rise} = t_{fall}$ < 100ns							
Minimal recessive bit time [2]	$t_{rec(min)}$		40	50	58	µs	
Maximum recessive bit time [2]	$t_{rec(max)}$		40	50	58	µs	
Duty cycle 1	D_1	$D_1 = t_{rec(min)} / (2*t_{Bit})$	0.396				A
Duty cycle 2	D_2	$D_2 = t_{rec(max)} / (2*t_{Bit})$			0.581		A
LIN transceiver parameter according to LIN Physical Layer Spec. rev. 2.0, table 3.4 (10.4kbit/s)							
Conditions: Low slew mode; V_{SUP} =7.0V to 18V; BUS loads: 1kΩ/1nF; 660Ω/6.8nF; 500Ω/10nF TxD signal: t_{Bit} = 96µs, $t_{wH} = T_{wL} = t_{Bit}$; $t_{rise} = t_{fall}$ < 100ns							
Minimal recessive bit time [2]	$t_{rec(min)}$		80	96	113	µs	
Maximum recessive bit time [2]	$t_{rec(max)}$		80	96	113	µs	
Duty cycle 1	D_1	$D_1 = t_{rec(min)} / (2*t_{Bit})$	0.417				A
Duty cycle 2	D_2	$D_2 = t_{rec(max)} / (2*t_{Bit})$			0.590		A
LIN transceiver parameter according to SAE J2602 (10.4kbit/s)							
Conditions: Low slew mode; V_{SUP} =7.0V to 18V; BUS loads: 1kΩ/1nF;660Ω/6.8nF;500Ω/10nF TxD signal: t_{Bit} = 96µs, $t_{wH} = T_{wL} = t_{Bit}$; $t_{rise} = t_{fall}$ < 100ns							
Minimal recessive delay TxD -> BUS [2]	$t_{x\_rec\_min}$				48	µs	
Maximum recessive delay TxD -> BUS [2]	$t_{x\_rec\_max}$				48	µs	
Minimal dominant delay TxD -> BUS [2]	$t_{x\_dom\_min}$				48	µs	
Maximum dominant delay TxD -> BUS [2]	$t_{x\_dom\_max}$				48	µs	
Maximum rec. to dom. delay	$T_{r\_d\_max}$	$t_{x\_rec\_max} - t_{x\_dom\_min}$			15.9	µs	A
Maximum dom. to rec. delay	$T_{d\_r\_max}$	$t_{x\_dom\_max} - t_{x\_rec\_min}$			17.2	µs	A

[1] A = 100% serial test, B = Operating parameter, C = only used for data characterization (cpk), D = Value guaranteed by design
[2] See chapter 2.5 Timing Diagrams

2.5 Timing Diagrams

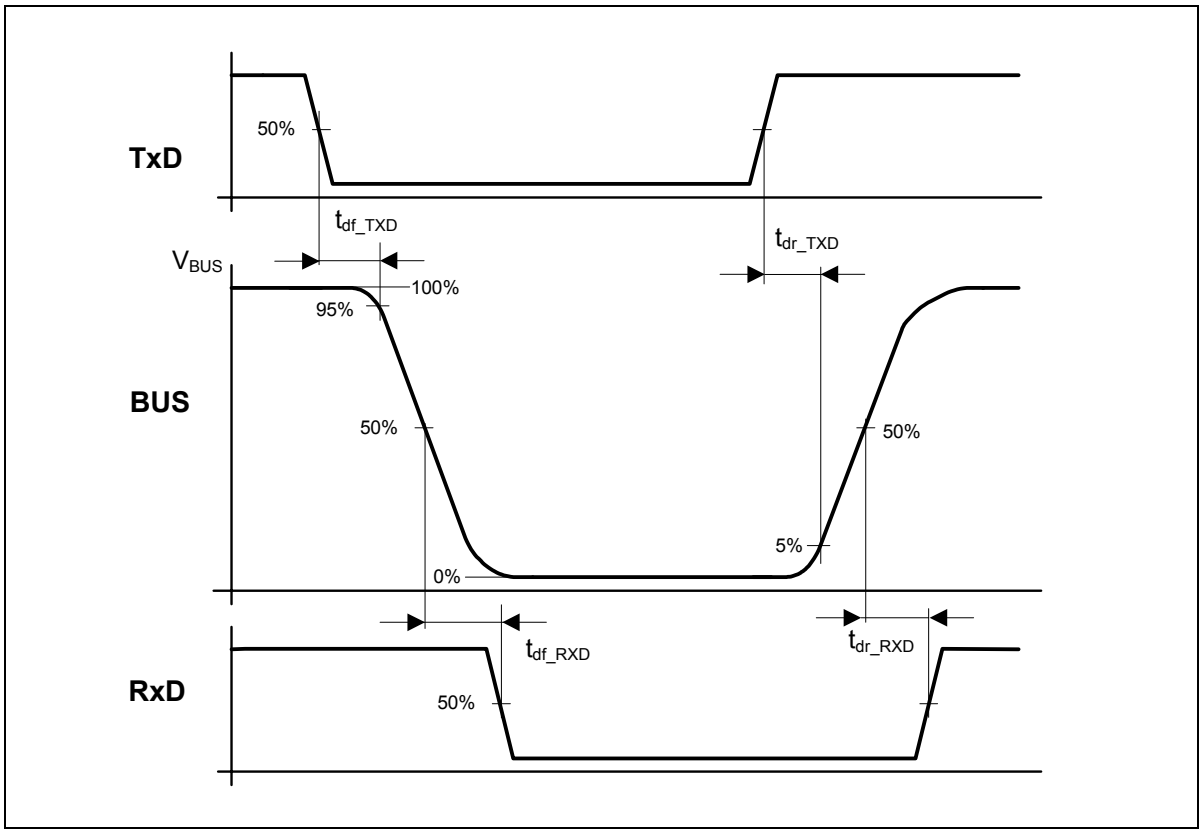


Figure 2 - Timing diagram for propagation delays

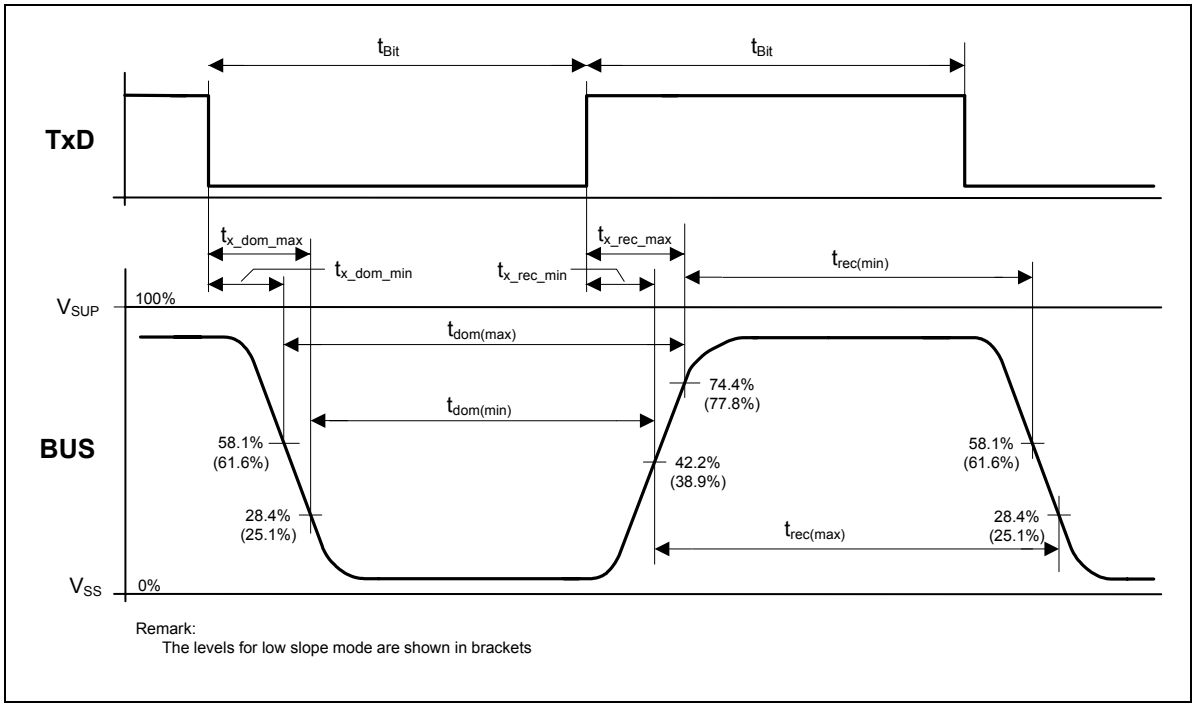


Figure 3 - Timing diagram for duty cycle acc. to LIN 2.0 and J2602

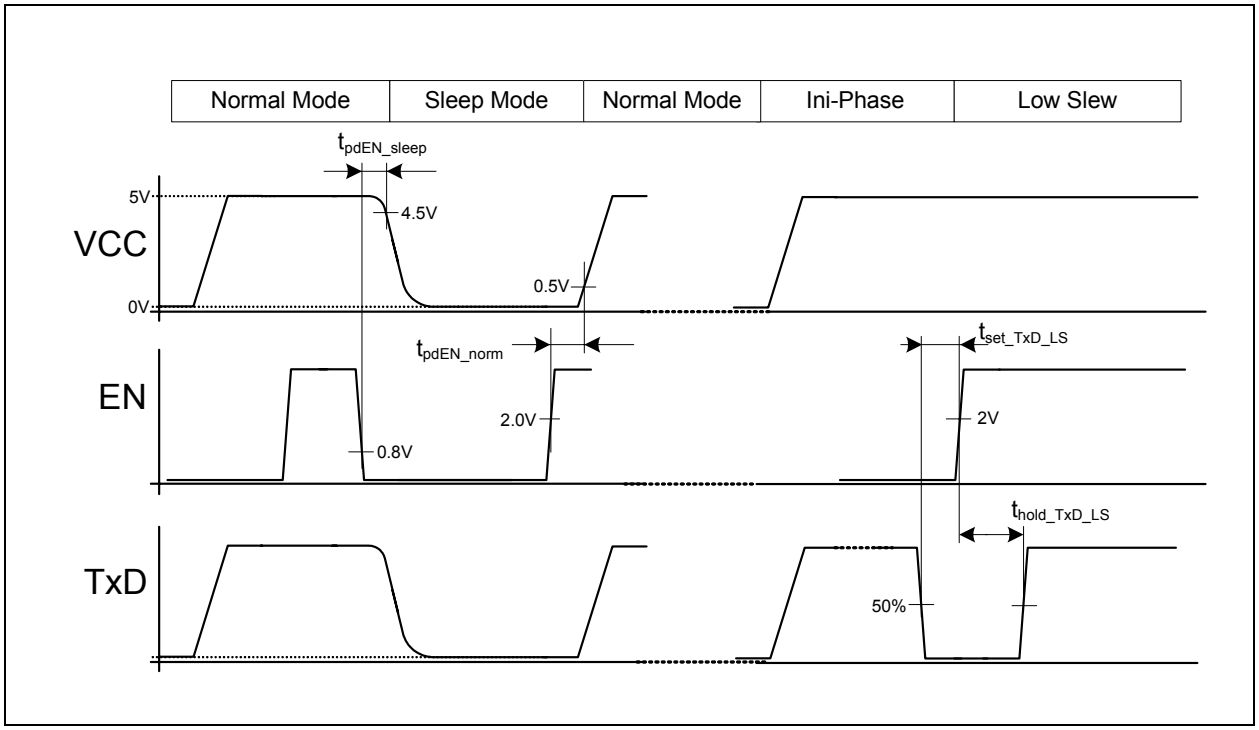


Figure 4 - Timing Diagram for EN mode selection

3. Functional Description

The TH8065 consists of a low drop voltage regulator 5V/70mA and a LIN bus transceiver, which is a bi-directional bus interface for data transfer between LIN bus and the LIN protocol controller.
Additionally integrated is a RESET unit with a power-on-reset delay of 8ms (optional 4,15 or 30ms).
and a programmable watchdog time which will be defined by an external capacity.

3.1 Operating Modes

The TH8065 provides three main operating modes “normal”, “sleep” and “low slew” and the intermediate states “Ini-state” and “thermal shutdown”. The main modes are fixed states defined by basic actions (VSUP start, EN or wake-up). The intermediate states are soft states. They aren’t defined by logical actions but by changes of voltage (VSUP, VCC) or junction temperature.

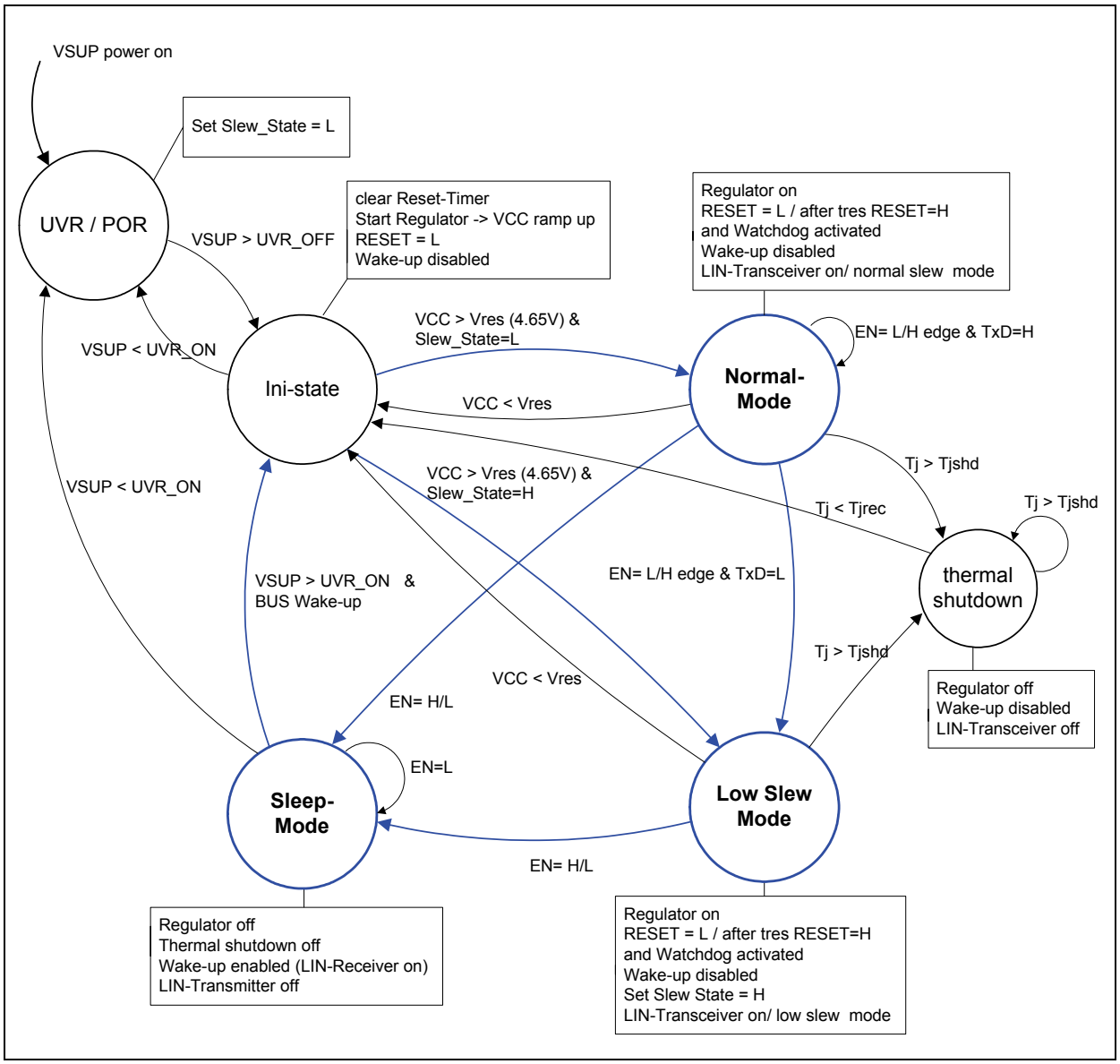


Figure 5 - State diagram of operating modes

Normal Mode

This mode is the base mode. The bus transceiver is able to send with a max baud rate of 20kbit/s.
The whole TH8065 is active. Switching to normal mode can be done via the following actions:

- Start of V_{SUP} or after under voltage reset
- Rising edge at EN (EN=high) and TxD=high (local wake-up)
- Activity on the LIN bus (remote wake-up)

Sleep Mode

Sleep mode is most current saving. With a falling edge on EN (EN=low) the TH8065 is switched from normal mode into sleep mode. The voltage regulator and the reset/watchdog unit will be switched off and the LIN transceiver is in recessive state.
Switching into sleep mode can be done independently from the current transceiver state. That means if the transmitter is in dominant state this state will be cancelled and it will be switched to recessive state.

Low Slew Mode

In this mode the slew rate is switched from the normal value of typ. 1.6V/µs to a low value of typ. 0.8V/µs. This mode is optimized to send with a maximum baud rate of 10.4kbit/s (SAE J2602). Because of this reduction of the slew rate the EME behaviour is improved especially in the frequency range of 100 kHz to 10MHz.
Switching to this mode is possible with a combination of rising edge on EN together with a low level on TxD.

POR-state

This is the power-on-reset state of the TH8065, while Vsup < V_{SUVR_OFF}. If the prior state was sleep mode, the TH8065 switches via the ini-state to normal mode.

Ini-state

This is an intermediate state, which will pass through after switching on of VSUP or VCC. The TH8065 remains in this state if V_{CC} is below V_{RES} (Reset output = L) and Vsup > V_{SUVR_ON}.

Thermal Shutdown

If the junction temperature T_J is higher than T_{JSHD} (>155°C), the TH8065 will be switched into the thermal shutdown mode. The behaviour within this mode is comparable with the sleep mode except for LIN transceiver operating. The transceiver is completely disabled; no wake-up functionality is available.
If T_J falls below the thermal recovery temperature T_{JREC} (typ. 140°C) the TH8065 will be recover to the previous state (normal, sleep or low slew).

3.2 Initialization

Initialization starts if the power supply is switched on as well as every rising edge on of the TH8065 via the EN pin.

VSUP- Power-ON

If V_{SUP} is switched on the TH8065 starts to normal mode via the POR- and Ini-state. A combination of dynamic POR and under voltage reset circuitry generates a POR signal, which switches the TH8065 into normal mode. This power on behaviour is independent from the status of the EN-pin.

Power-on reset and under-voltage reset operates independent from each other, which secures the independence from the rise time of VSUP. During fast VSUP edges the power-on reset will be active. If the increasing of VSUP is very slow (> 1ms/V) and V_{SUP} > V_{SUVR_OFF} (typ. 3.5V) the under voltage reset unit initializes the voltage regulator.

The effects of both POR circuits at different VSUP slopes will show in Figure 6.

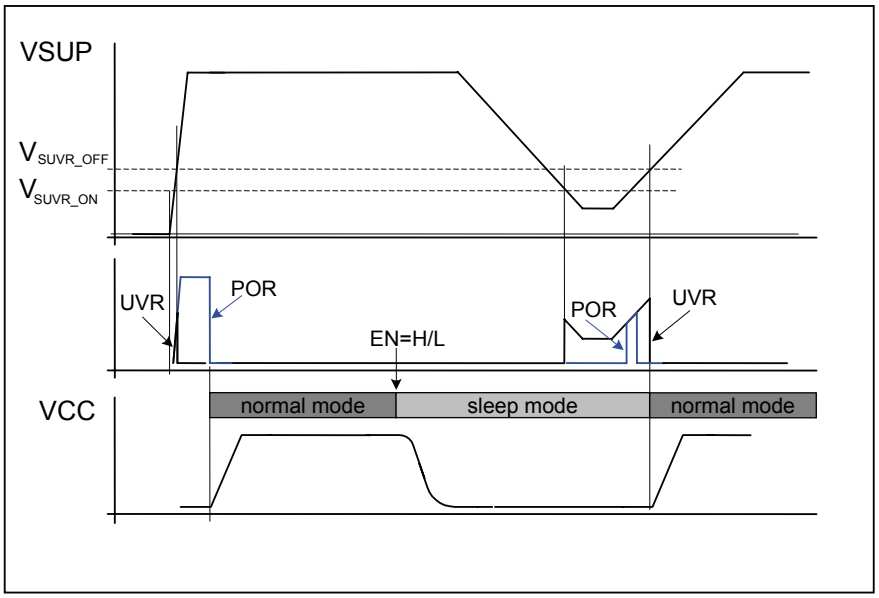


Figure 6 - Operating of power-on and under-voltage reset

After POR the voltage regulator starts and the VCC voltage will be output. If V_{CC}>V_{MRes} the bus interface will be activated. If the V_{CC} voltage level is higher than V_{RES}, the reset time t_{Res} is started. After t_{Res} the RESET output switches from low to high (see Figure 12).
The Initialization procedure operates after POR independent from the EN voltage.

Start of Linear Regulator via Wake-up

The initialization is only being done for the VCC circuitry parts. This procedure begins with leaving the master reset state (V_{CC} > V_{MRes}) and runs in the same manner as the VSUP-Power-On.

3.3 Wake-Up

If the regulator is put into sleep mode it can be woken up with the BUS interface. Every pulse on the BUS (high pulse or low pulse) with a pulse width of min. 70µs switches on the regulator.
The low slew mode has to be selected again if necessary.
After the BUS has woken up the regulator, it can only be switched off with a high level followed by a low level on the EN pin.

3.4 VSUP under voltage reset

The under voltage detection unit inhibits an undefined behaviour of the TH8062 under low voltage condition (VSUP < 4V). If VSUP drops below V_{SUVR_ON} (typ. 3.1V) the under voltage detection becomes active and the IC will be switched to POR state. The following increasing of VSUP above V_{SUVR_OFF} (typ. 3.7V) cancels this POR state and the voltage regulator starts with the initialization sequence.

VSUP under voltage in Normal Mode

Supply Voltages below V_{SUVR_OFF} do not influence the voltage regulator. The output voltage Vcc follows VSUP.

VSUP under voltage in Sleep Mode

No exit from the sleep mode will take place if the VSUP voltage drops down to V_{SUVR_ON} (typ. 3.5V). The under voltage reset becomes active (POR-state) if the voltage drops below 2.7V. As a result of this functioning, the sleep mode is left to the normal mode. If VSUP rises again above V_{SUVR_OFF} (typ. 4.2V) the IC initializes the voltage regulator and continues to work with the normal mode.

The under voltage reset unit secures stable functioning in the under voltage range of VSUP down to GND level. The dynamic Power-On-Reset secures a defined internal state independent from the duration of the VSUP drop, which guarantees a stable restart.

VSUP under voltage in Low Slew Mode

The behaviour of TH8062 at low VSUP voltages is equal to the sleep mode. The low slew mode will be cancelled, if VSUP drops below V_{SUVR_ON} in this mode. The TH8062 enters the normal mode, if VSUP rises again above V_{SUVR_OFF}.

3.5 Overtemperature Shutdown

If the junction temperature is 155°C < T_J < 175°C the over-temperature recognition will be activated and the regulator voltage will be switched off. The V_{CC} voltage drops down, the reset state is entered and the bus-transceiver is switched off (recessive state).
After T_J falls below 140°C the TH8065 will be initialized again (see Figure 12). This initialisation starts independently from the voltage levels on EN and BUS. Within the thermal shutdown mode the transceiver can not switch to the normal mode neither with local nor with remote wake-up.
The operation of the TH8065 is possible between T_{Amax} (125°C) and the switch off temperature, but small parameter differences can appear.
After over-temperature switch-off the IC behaves as described in chapter 3.8 RESET and Watchdog.

3.6 LIN BUS Transceiver

The TH8065 has an integrated bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller.
The transceiver consists of a driver with slew rate control, wave shaping and current limitation and a receiver with high voltage comparator followed by a debouncing unit.

Transmit Mode

During transmission the data at the pin TxD will be transferred to the BUS driver to generate a bus signal. To minimize the electromagnetic emission of the bus line, the BUS driver has an integrated slew rate control and wave shaping unit.
Transmitting will be interrupted in the following cases:

- Sleep mode
- Thermal Shutdown active
- Master Reset (V_{CC} < 3.15V)

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with an active diode This diode prevents the reverse current of V_{BUS} during differential voltage between VSUP and BUS (V_{BUS}>V_{SUP}).
No additional termination resistor is necessary to use the TH8065 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via an external 1kΩ resistor in series with a diode to VBAT.

Receive Mode

The data signals from the BUS pin will be transferred continuously to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit (τ = 2.8µs).

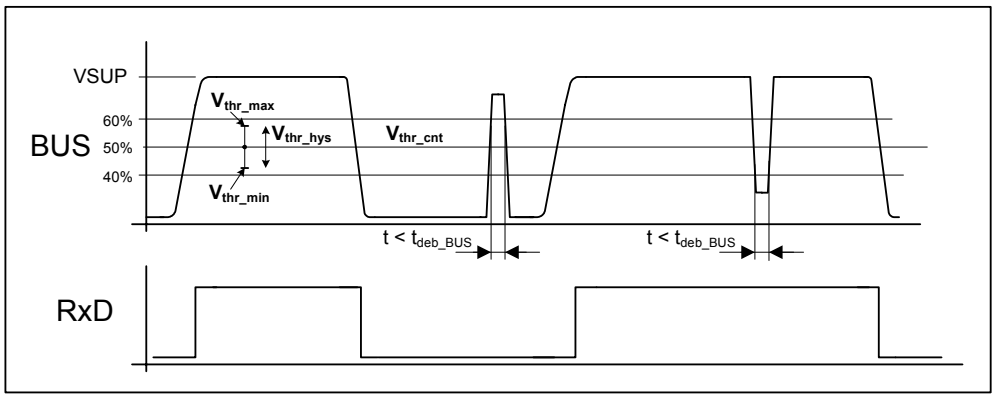


Figure 7 - Receive mode impulse diagram

The receive threshold values V_{thr_max} and V_{thr_min} are symmetrical to the centre voltage of 0.5*V_{SUP} with a hysteresis of 0.150*V_{SUP}. Including all tolerances the LIN specific receive threshold values of 0.4*V_{SUP} and 0.6*V_{SUP} will be securely observed.

Slew Modes and Data rates

The TH8065 is a ***constant slew rate*** transceiver which means that the bus driver works with a mode depended slew rate. In normal mode the slew rate is typical 1.6 V/µs and in low slew mode typical 0.8 V/µs. The lower slew rate in low slew mode associated with a baud rate of 10.4kbit/s improves the EME behaviour. The LIN transceiver of TH8065 is compatible to the physical layer specification according to LIN 2.0 specification for data rates up to 20kbit/s and the SAE specification J2602 for data rates up to 10.4kbit/s.
The constant slew rate principle is very robust against voltage drops and can operate with RC- oscillator systems with a clock tolerance up to ±2% between 2 nodes.

Low Slew Mode

In this mode the slew rate is switched from the normal value of typ. 1.6V/µs to a low value of typ. 0.8V/µs. This mode is optimized to send with a maximum baud rate of 10.4kbit/s (acc. to SAE J2602). Because of this reduction of the slew rate the EME behaviour is improved especially in the frequency range of 100 kHz to 10MHz.

Input TxD

The 5V input TxD controls directly the BUS level:

TxD = low	->	BUS = low (dominant level)
TxD = high	->	BUS = high (recessive level)

The TxD pin has an internal pull up resistor connected to VCC. This guarantees that an open TxD pin generates a recessive BUS level.

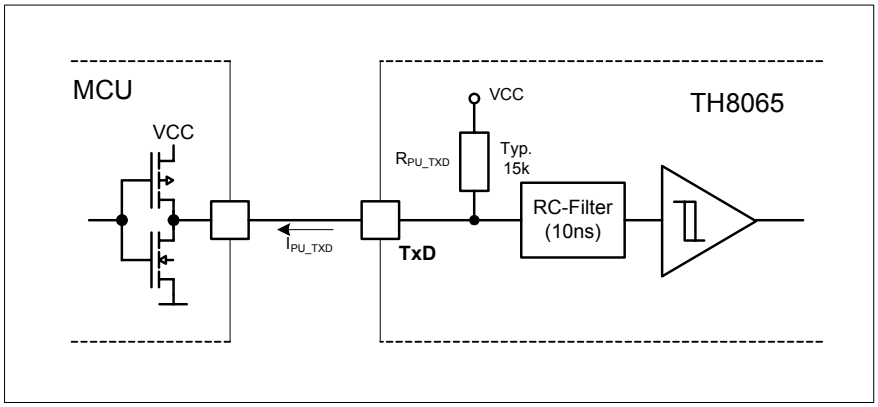


Figure 8 - TxD input circuitry

Output RxD

The received BUS signal will be output to the RxD pin:

BUS < V_{thr_cnt} – 0.5 * V_{thr_hys} -> RxD = low
BUS > V_{thr_cnt} + 0.5 * V_{thr_hys} -> RxD = high

This output is a push-pull driver between VCC and GND with an output current of 1mA.

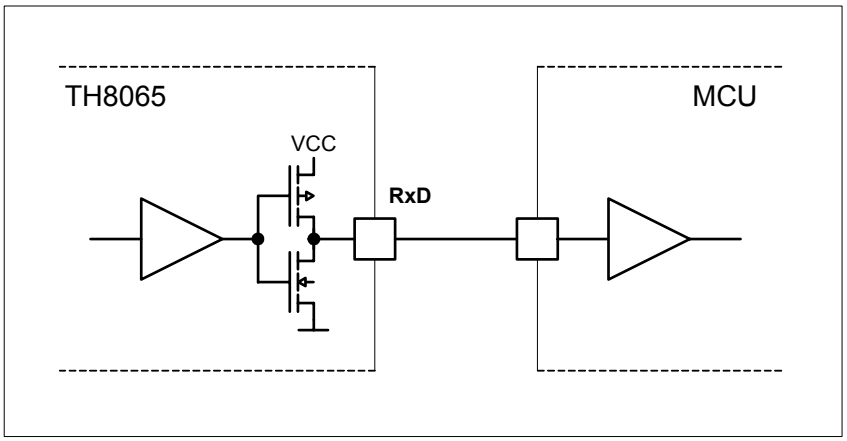


Figure 9 - RxD output circuitry

3.7 Linear Regulator

The TH8065 has an integrated low drop linear regulator with a p-channel-MOSFET as driving transistor. This regulator outputs a voltage of 5V ±3% and a current of ≤70mA within an input voltage range of 6V ≤ V_{SUP} ≤ 18V. The current limitation unit limits the output current for short circuits or overload to 130mA respectively drop-down of the V_{CC} voltage.

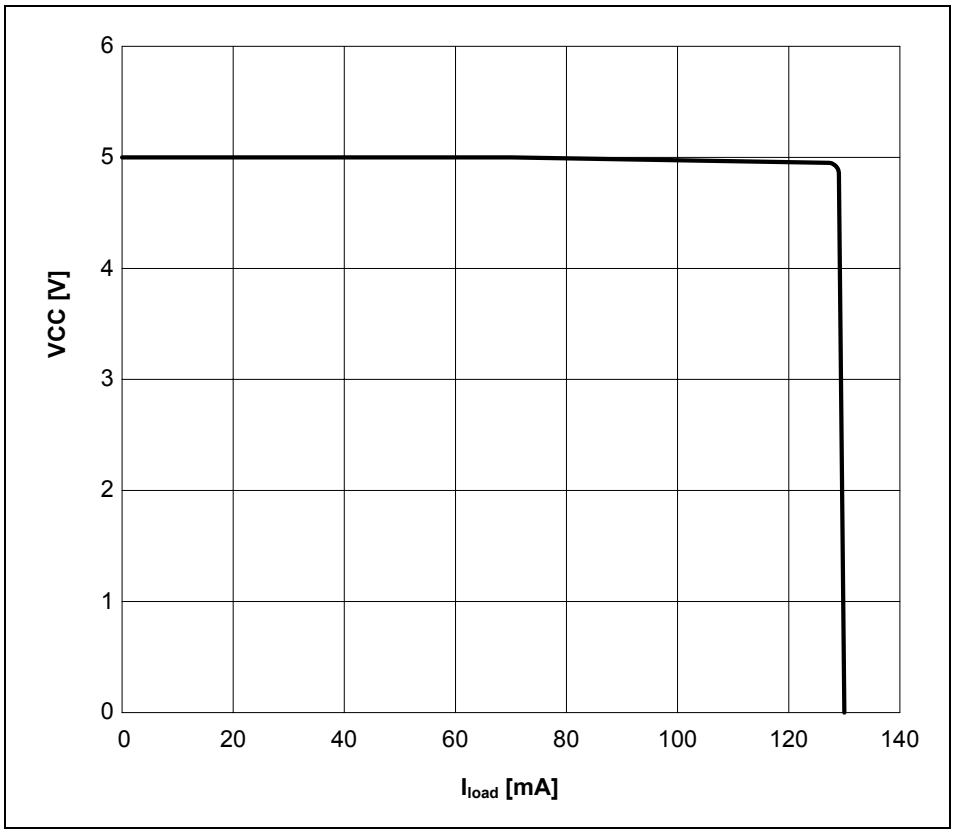


Figure 10 - Characteristic of current limitation VCC = f (I_{VCC})

3.8 RESET and Watchdog

The TH8065 contains a combined reset- and watchdog-unit which secures the correct initialization and generation of the reset signal.

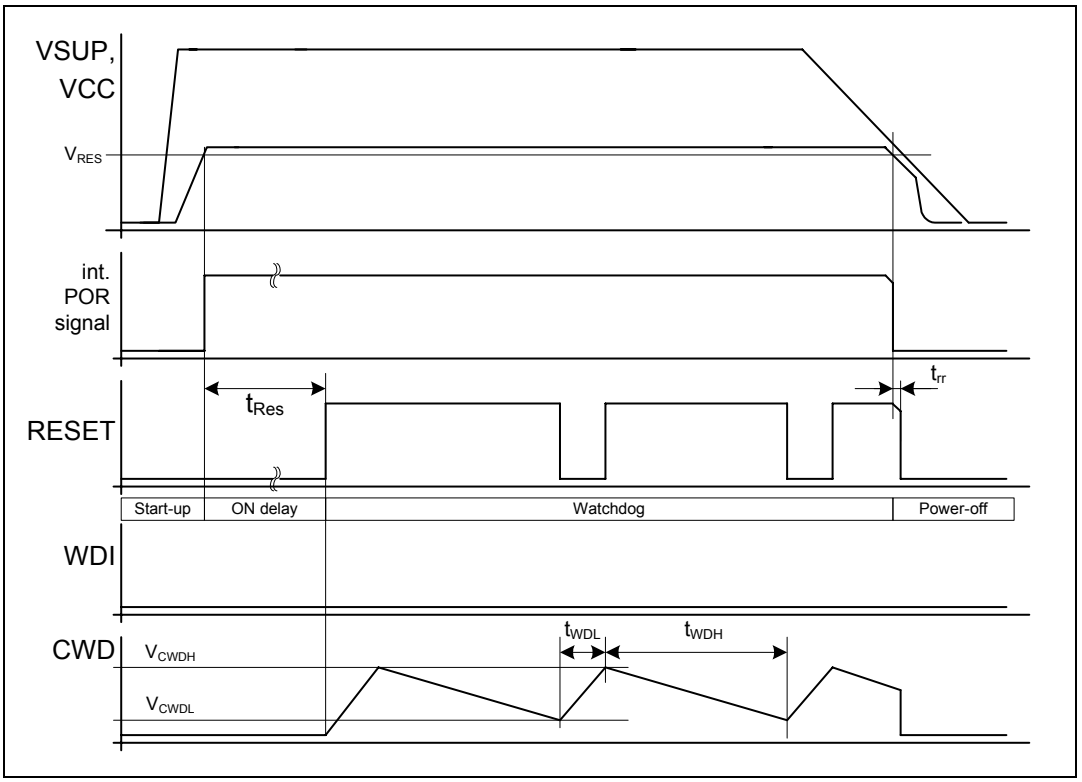


Figure 11 - Reset and Watchdog behaviour

The RESET pin outputs the reset state and the watchdog state of the TH8065. The POR timer will be started if V_{SUP} is switched on and V_{CC}> POR threshold (4.65V). The Watchdog is inactive. After the time t_{Res} the RESET output is switched from low to high and the watchdog becomes active. The charging of the watchdog capacity starts and dependent from the trigger pulse on the WDI input the Reset outputs the status of the watchdog.
The watchdog is only active if $V_{CC} > V_{RES}$. If V_{CC} drops below V_{RES} the watchdog will be switched off and the watchdog capacity will be discharged.

3.8.1. RESET

The RESET unit combines a VCC low voltage detection unit with fixed POR timer This output is switched from low to high if V_{SUP} is switched on and V_{CC}>V_{RES} (4.65V) after the time t_{Res} .
All conditions which cause a drop of the V_{CC} voltage will be detected from the low voltage reset unit which generates a reset signal. The TH8065 will be reinitialized if the V_{CC} voltage rises above the low voltage limit.
If the voltage V_{CC} drops below V_{RES} then the RESET output is switched from high to low after the time t_{rr} has been reached. For this reason short breaks of the V_{CC} voltage and uncontrolled reset generations will be inhibited.
The circuitry of the RESET output driver guarantees, that the reset low level during decreasing of the V_{CC} voltage will be secure kept (see Figure 13).

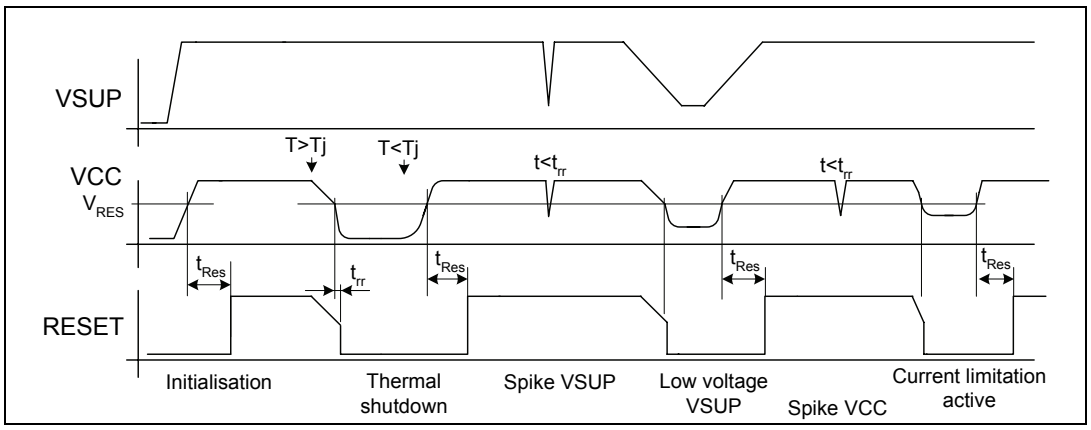


Figure 12 - Reset behaviour

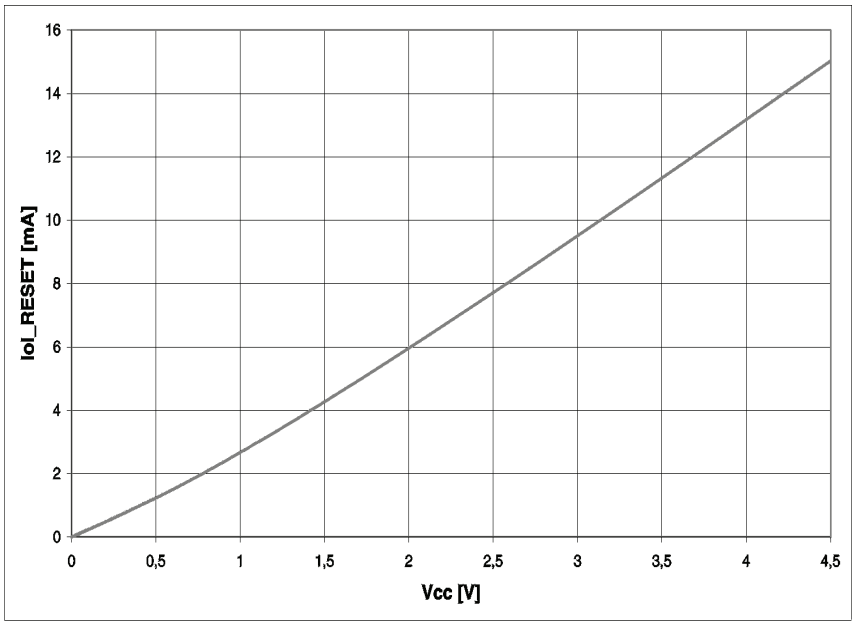


Figure 13 - Output current of reset output vs. VCC voltage

3.8.2. Watchdog

The Watchdog can be used for observation of the connected microcontroller. It has to be triggered via the WDI input and the time is defined via the capacity connected to the CWD input. The watchdog status will be output via the reset pin.
With rising edges on WDI the watchdog time will be reset. If the WDI input isn't triggered the internal circuitry generates low pulses at the RESET pin with a time t_{WD_R} and a period of $t_{WD\text{-}per}$.
The CWD capacitor provides a wide adjustment range for the watchdog time.
With every rising edge on WDI the capacitor C_{WD} will be charged up to the threshold V_{CWDL}. If there is no new trigger pulse on WDI, the following discharging of C_{WD} within the time t_{WDL} will be done up to the lower threshold V_{CWDL}.

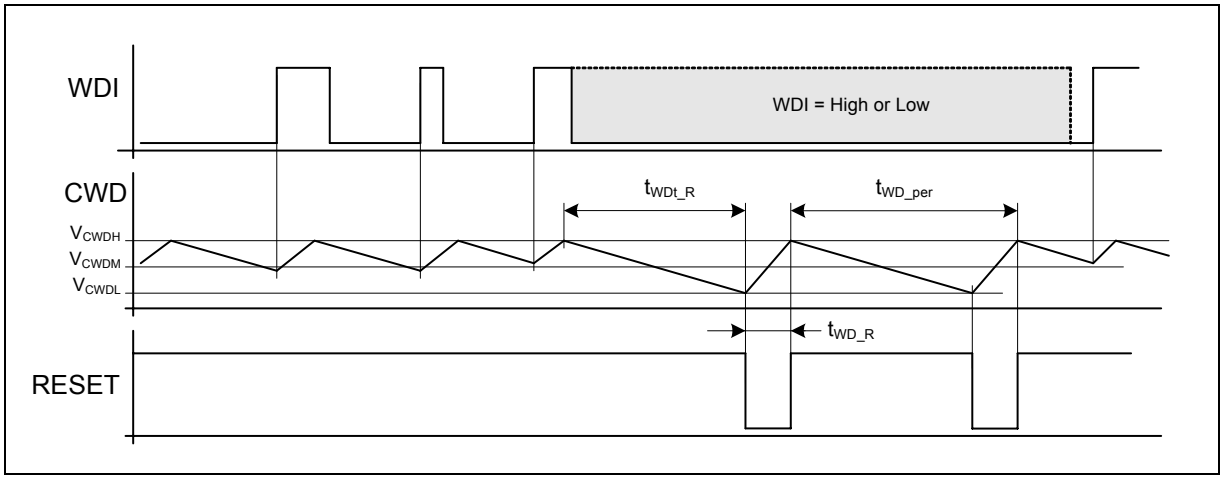


Figure 14 - Watchdog timing

The reset output will be switched from high to low (watchdog reset), if the voltage on pin CWD reaches V_{CWDL}. The reset output stays at low level until the voltage at C_{WD} has reached the level of V_{CWDH}.
The RESET pin generates a periodic signal with low pulse width of t_{WD_R} and a period of t_{WD_per}, if no retrigger of WDI takes place.

Calculation of Watchdog time

Watchdog reset time:

$$t_{WD\_R} = \frac{(V_{CWDH} - V_{CWDL}) * C_{WD}}{I_{CWD\_pu}}$$

Max. watchdog reset trigger time

$$t_{WDt\_R} = \frac{(V_{CWDH} - V_{CWDL}) * C_{WD}}{I_{CWD\_pd}}$$

C_{WD}	Watchdog capacity connected to pin CWD
V_{CWDH}	Upper watchdog threshold
V_{CWDL}	Lower watchdog threshold
I_{CWD_pu}	CWD charge current
I_{CWD_pd}	CWD discharge current

With the valid charge and discharge currents of C_{WD} of the TH8065 is a simple calculation of the capacity values for a defined watchdog trigger time and reset time possible:

$$t_{WDt\_R}[ms] = C_{WD}[nF]$$
$$t_{WD\_R}[ms] = 0.1 * C_{WD}[nF]$$

Example:

$$C_{WD} = 10nF \rightarrow t_{WDt\_R} = 10ms \;\; and \;\; t_{WD\_R} = 1ms$$

Within a timeframe of 10ms the MCU has to reset the watchdog to prevent a reset generation. The complete watchdog period t_{WD_per} = 11ms.

If the watchdog has to be deactivated for e.g. firmware development, the pin CWD has to be directly connected to GND. The reset signal is in this case only determined by the reset thresholds.

3.9 Mode Input EN

The TH8065 is switched into the sleep mode with a falling edge and into normal mode with a rising edge at the EN pin. The normal mode will be kept as long as EN = high.
The deactivation of TH8065 with a falling edge at EN can be done independently from the state of the bus-transceiver.

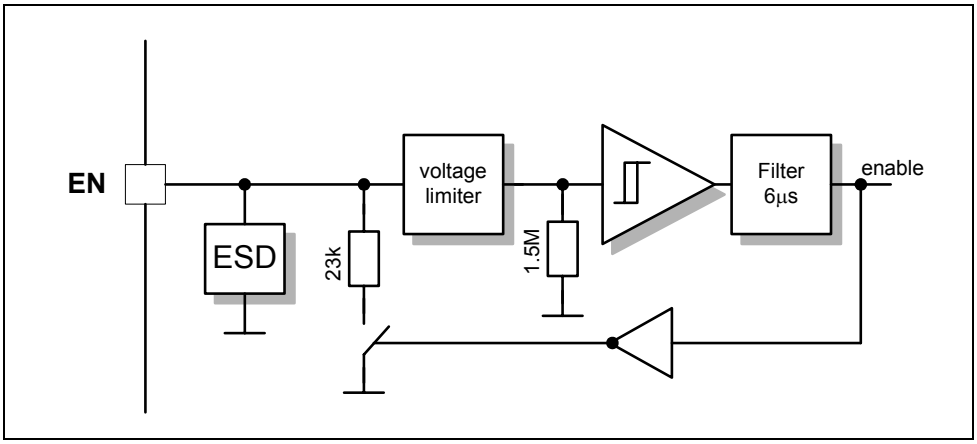


Figure 15 - EN input circuitry

The maximum input voltage is VSUP. The threshold is typ. 1.4V and therefore also 5V and 3.3V CMOS levels can be used as input signal. Figure 15 shows the internal circuitry of the EN pin.
The EN input has an internal pull down resistor of typ. 23k to secure that if this pin is not connected a low level will be generated. An input debouncing filter of 6µs suppresses effectively disturbance couplings via the EN pin
It will use different pull down resistors for normal and sleep mode to minimize the sleep mode current.
The wide input voltage range allows different EN control possibilities. If the EN input is connected to a CMOS output of the MCU, a falling edge switches the TH8065 into sleep mode (the regulator is also switched off). The wake up is only possible via the bus line.

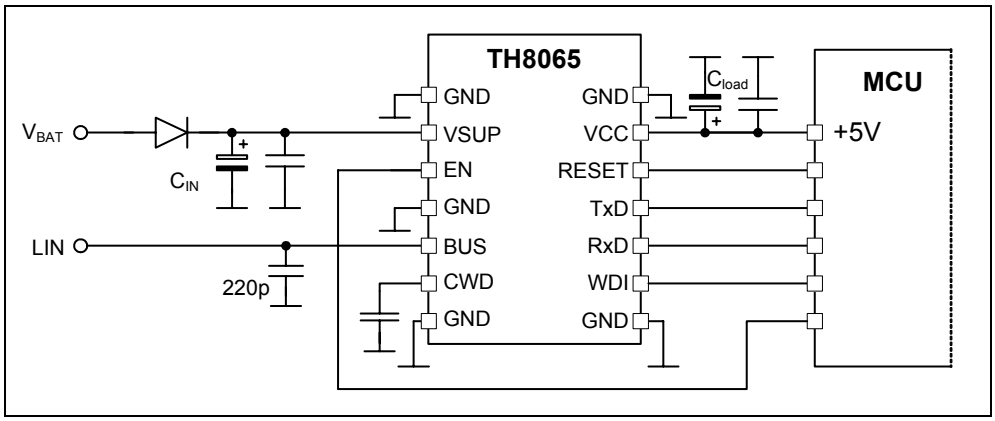


Figure 16 - EN controlled via MCU

If the application doesn't need the wake up capability of the TH8065 a direct connection EN to VSUP is possible. In this case the TH8065 operates in permanent normal mode. Also possible is the external (outside of the module) control of the EN line via a VBAT signal. If this is a direct VBAT signal an external reverse battery protection has to be added to the circuitry.

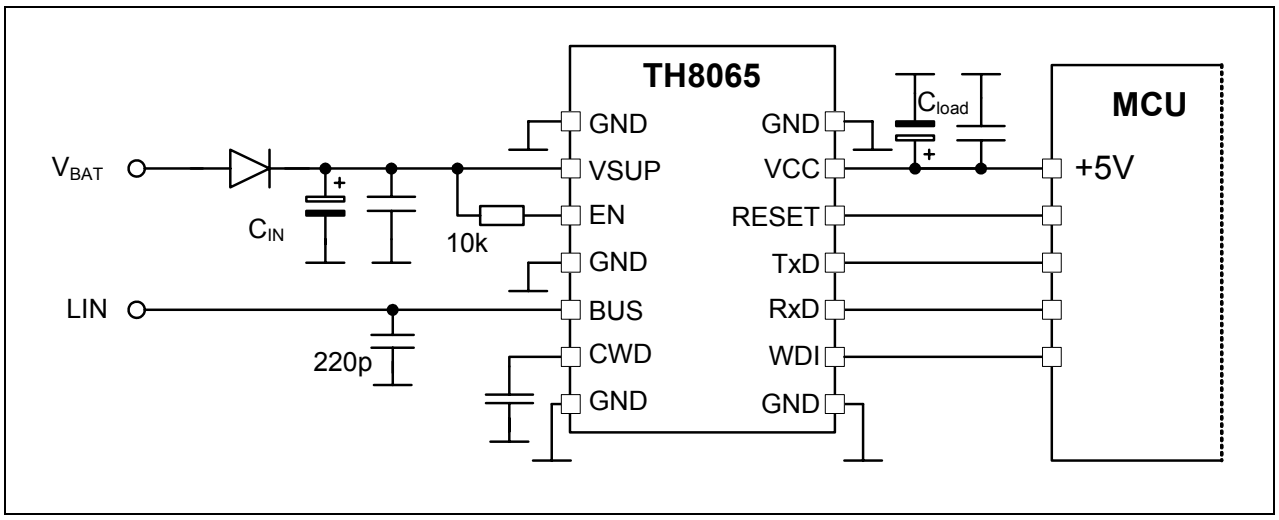


Figure 17 - Permanent normal mode

4. Application Hints

4.1 Safe Operating Area

The maximum power dissipation depends on the thermal resistance of the package and the PCB, the temperature difference between Junction and Ambient as well as the airflow.
The power dissipation can be calculated with:

$$P_D = (V_{SUP} - V_{CC}) * I_{VCC} + P_{D\_TX}$$

The power dissipation of the transmitter P_{D_TX} depends on the transceiver configuration and its parameters as well as on the bus voltage $V_{BUS}=V_{BAT}-V_D$, the resulting termination resistance R_L, the capacitive bus load C_L and the bit rate. Figure 18 shows the dependence of power dissipation of the transmitter as function of V_{SUP}. The conditions for calculation of the power dissipation is R_L=500Ω, C_L=10nF, bit rate=20kbit and duty cycle on TxD of 50%

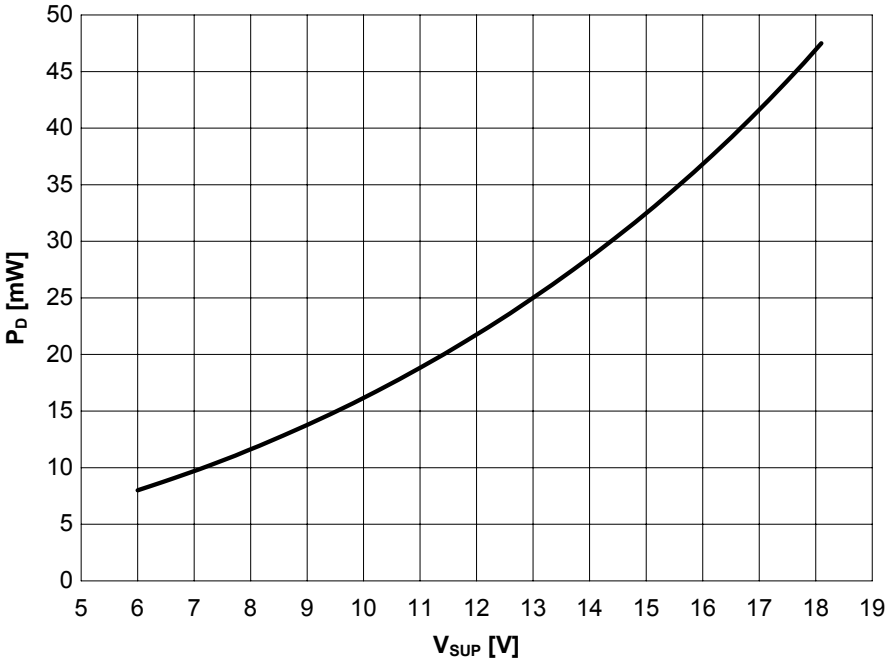


Figure 18 - Power dissipation LIN transceiver @ 20kbit

The permitted package power dissipation can be calculated:

$$P_{Dmax} = \frac{T_j - T_A}{R_{THJ-A}}$$

If we consider that $P_{D\_TX\_max}$= f (V_{SUP}) the max output current I_{VCC} on $V_{CC\ can}$ be calculated:

$$I_{VCCmax} = \frac{\frac{T_j - T_A}{R_{THJ-A}} - P_{D\_TX\_max\ @\ VSUP}}{VSUP - VCC}$$

T_J -T_A is the temperature difference between junction and ambient and R_{th} is the thermal resistance of the package. The thermal energy is transferred via the package and the pins to the ambient. This transfer can be improved with additional ground areas on the PCB as well as ground areas under the IC.

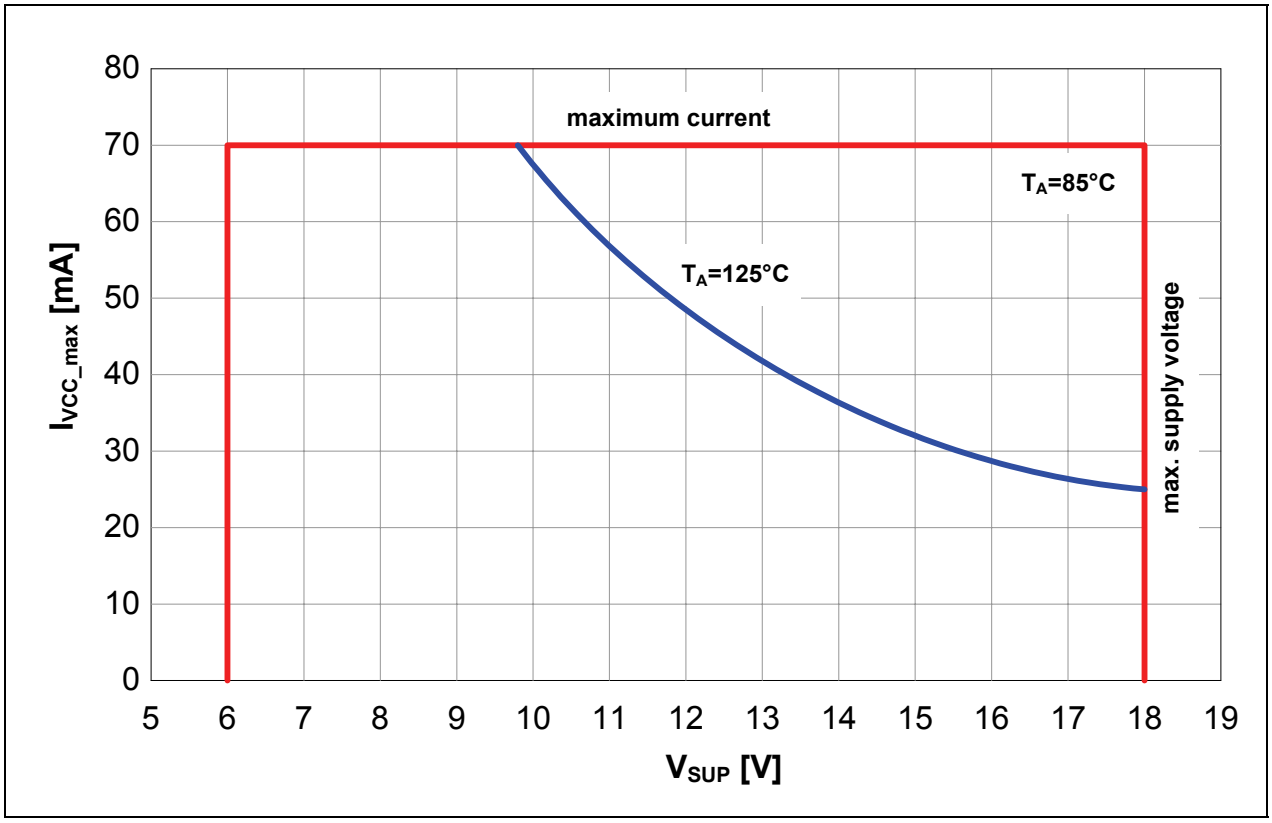


Figure 19 - Save operating area

The linear regulator of the TH8065 operates with input voltages up to 18V and can output a current of 70mA. The maximum power dissipation limits the maximum output current at high input voltages and high ambient temperatures. The output current of 70mA at an ambient temperature of T_A = 125°C is only possible with small voltage differences between V_{SUP} and V_{CC}. See Figure 19 for safe operating areas for different ambient temperatures. The TH8065 is able to output 70mA over the whole voltage range if the max ambient temperature is limited to 85°C.

4.2 Low Dropout Regulator

The voltage regulator of theTH8065 is a low dropout regulator (LDO) with a p-MOSFET as driving transistor. This kind of regulator has a standard pole, generated from the internal frequency compensation and an additional pole, which is dependent from the load and the load capacitance. This additional pole can cause an instable behaviour of the regulator! It is required a zero point to compensate this additional pole. It can be realised via an additional load resistor in series with a load capacitor. It is used for this compensation the equivalent series resistance (ESR) of the load capacitor. Every real capacitor is characterized with an ESR value. With the help of this ESR value an additional zero point is implemented into the amplification loop and therefore the result of the negative phase shift is compensated.
Because of this correlation the regulator has a stable operating area which is defined by the load resistance R_L, the load capacitor C_L and the corresponding ESR value. The load resistance resp. load current is defined by the application itself and therefore the compensation of the pole can only be done via variation of the load capacitance and ESR value.

Input Capacitor on VSUP C_{IN}

An input capacitance is necessary of $C_{IN} \geq 4.7\mu F$. Higher capacitance values improves the line transient response and the supply noise rejection behaviour. The combination of electrolytic capacitor (e.g.100µF) in parallel with a ceramic RF-capacitor (e.g.100nF) archives good disturbance suppressing.
The input capacitor should be placed as close as possible (< 1cm) to the VSUP pin.

Load Capacitor on VCC C_L

The regulator is stabilized by the output capacitor C_L. The TH8065 requires a minimum of 4.7µF capacitor connected to the 5V output to insure stability. This capacitor should maintain its ESR in the stable region of the ESR curve (See Figure 20) over the full operating temperature range of the application. It has to be taken into account that the capacitance value and the ESR of a capacitor changes with temperature. The minimal capacitance value must also be kept within the whole operating temperature range.

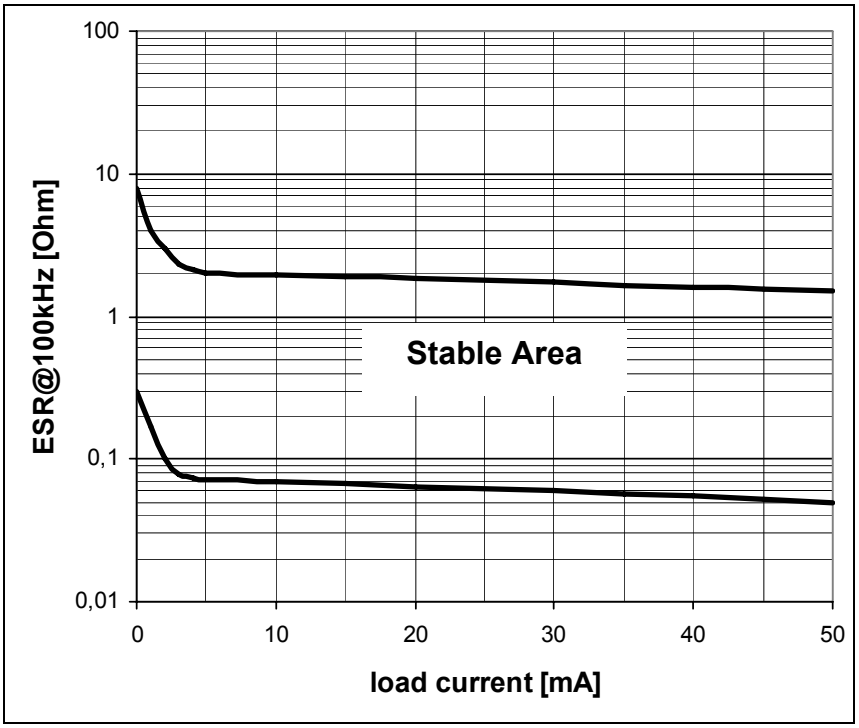


Figure 20 - ESR Curves for 6.8µF ≤ C_L ≤ 100µF and Frequency of 100 kHz

The value and type of the output capacitor can be selected using the diagram shown in Figure 20. The load capacitor should be placed as close as possible (< 1cm) to the VCC pin.

Capacitance Value

The capacitance value of an electrolytic capacitor is dependent from the voltage, temperature and the frequency. The temperature coefficient of the capacitor value is positive, that means that the value increases with increasing of the temperature. The capacitance value decreases with increasing of the frequency. This behaviour of a capacitor can cause that at T_A=-40°C the capacitance value falls below the minimum required capacitance for the regulator. In this case the regulator becomes instable, which means the regulator starts oscillation. The nominal value of the capacitor at T_A=25°C has to be chosen with enough margin under consideration of the capacitor specification. The instable behaviour will be amplified because of the decreasing of the capacitance with this oscillation.

ESR

The equivalent serial resistance is the resistor part of the equivalent circuit diagram of a capacitor. The ESR value is dependent from the temperature and frequency. Normally the specified ESR values for a capacitor is valid at a temperature of T_A=25°C and a frequency of f=100 kHz.
The temperature coefficient is negative, which means with increasing of the temperature the ESR value decreases. In the choice of the capacitance has to be taken into account that the ESR can decrease at T_A=-40°C dramatically that the valid operating area can be left, which causes that the regulator will be instable.

Tantalum Capacitors

This type of capacitor has a low dependence of the capacitance and the ESR from the temperature and is therefore well suited as VCC load capacitor.

Aluminium Capacitors

These capacitors show a strong influence of the capacitance and the ESR from the temperature. This characteristic restrains the usability as load capacitor for the low drop regulator of TH8065.

4.3 Application Circuitry

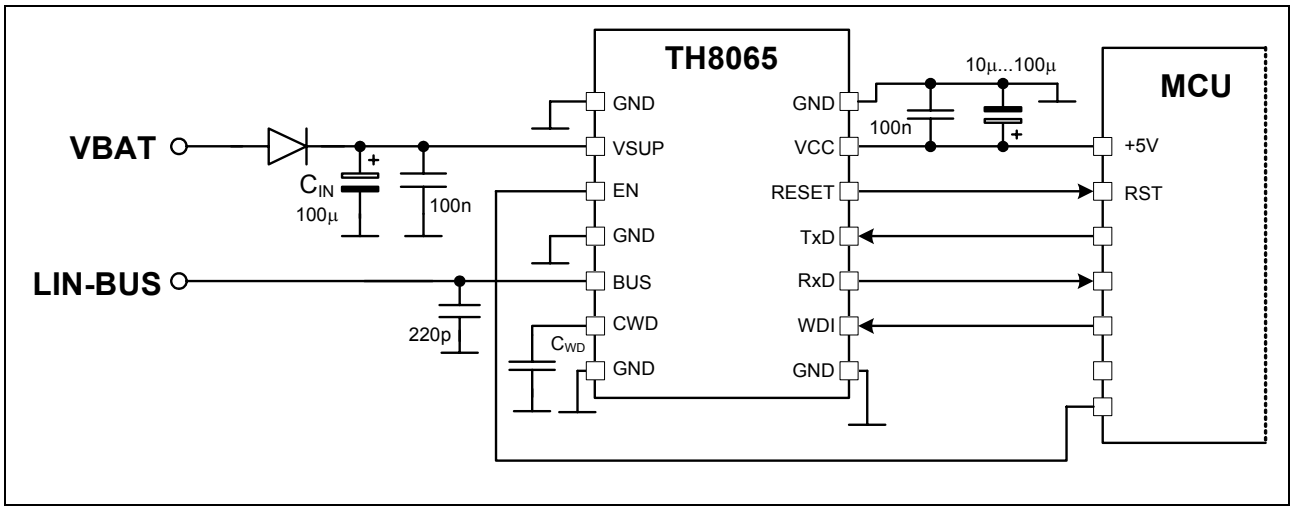


Figure 21 - Application circuit (slave node)

4.4 EMI Supressing

To minimize the influence of EMI on the bus line a 220pF capacitor should be connected directly to the BUS pin (see Figure 21). This EMI-Filter makes sure that the RF injections into the IC from the BUS line have no affect resp. will be limited.
Alternatively to a pure C-filter it is also possible to use LC- or RC-filter. The dimension of C, L or R, L depends on the corner frequency, the maximum LIN bus capacitance (10nF) and the compliance with the DC- and AC LIN bus parameters.

4.5 Connection to Flash-MCU

While programming a flash MCU the TH8065 should be disconnected from the MCU. This can be done via disconnecting the supply voltage from the TH8065 or by switching off with the EN pin. The reverse current supply of the IC via the RxD pin, if the connected MCU pin is used as normal signal input and programming input, must be inhibited via a decoupling diode. In this case the MCU must be supplied via the programming interface.

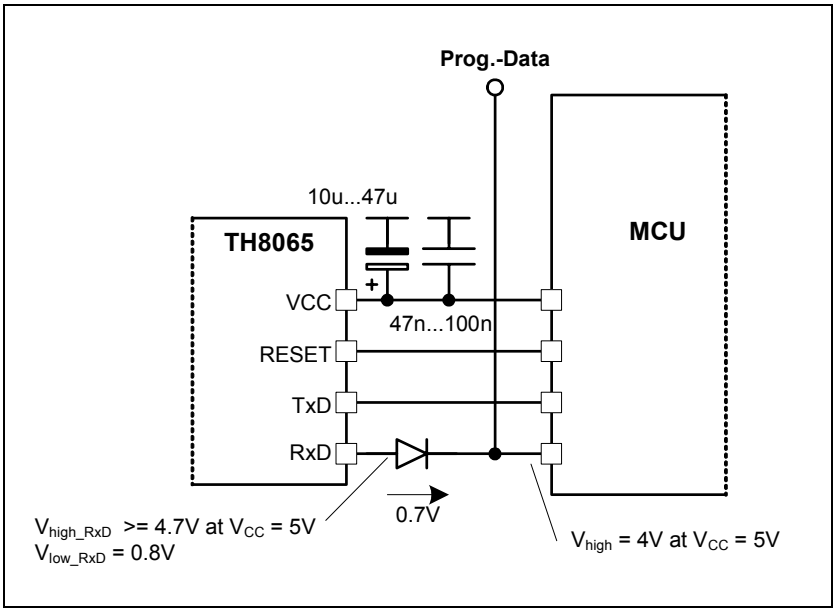


Figure 22 – Example circuitry for connection of RxD to MCU for flash programming

The programming of the Flash is also possible via the LIN pin, if the MCU supports this kind of flash mode.

5. Operating during Disturbance

5.1 Operating without VSUP or GND

The absence of V_{SUP} or GND connection will not influence or disturb the communication between other bus nodes. No reverse supply of the IC can appear if without GND or VSUP connection the BUS pin is on VBAT level.

5.2 Short Circuit BUS against VBAT

The reaction of the IC depends on the send state of the transceiver:

- Recessive LIN bus is blocked, no influence to the TH8065
- Dominant Current limitation, thermal shut down of TH8065 if power dissipation will make an overrun of T_J

5.3 Short Circuit BUS against GND

LIN bus is blocked. No influence on the TH8065.

5.4 Short Circuit TxD against GND

The LIN transceiver is permanently in the dominant state, which means the whole LIN bus. This state can only be detected from the LIN controller. In this case the controller must switch off the LIN node via the EN input of the TH8065. A thermal shut down of TH8065 will appear if the power dissipation will make an overrun of $T_{J.}$

5.5 TxD open

The internal pull-up resistor forces the LIN node to the recessive state. The communication between the other bus-nodes will not be disturbed.

5.6 Short Circuit VCC against GND

The VCC pin is protected via a current limitation. This state is comparable with the behaviour in the sleep mode.

5.7 Overload of VCC

Thermal switch off

The power dissipation is increasing if the load current is between I_{VCC_max} and I_{LVCC}. If the max junction temperature of >155°C is reached, the IC will be switched off. The voltage regulator will also be switched off and a reset signal is forced.

Over current

If the current limitation is active the voltage on VCC drops down. If this voltage under-runs the threshold V_{RES}, a reset will be forced.

5.8 Undervoltage VCC

The reset unit ensures the correct behaviour of the driver during under-voltage. The BUS pin generates the recessive state if $V_{CC} < V_{MRes}$ (3.15V). The inputs EN, WDI and TxD have pull-up or pull-down characteristics. If $V_{CC} \geq V_{MRes}$ the TxD signal is transmitted to the bus. The receive mode is also active.

5.9 Undervoltage VSUP

The combination of dynamic power on reset and low voltage reset guarantees a defined start up behaviour. If the supply voltage VSUP drops below 3V the low voltage detection becomes active. If the VSUP voltage rises again above 3.5V the low voltage reset will be terminated and the 5V voltage regulator will be started.

5.10 Short circuit RxD, RESET against GND or VCC

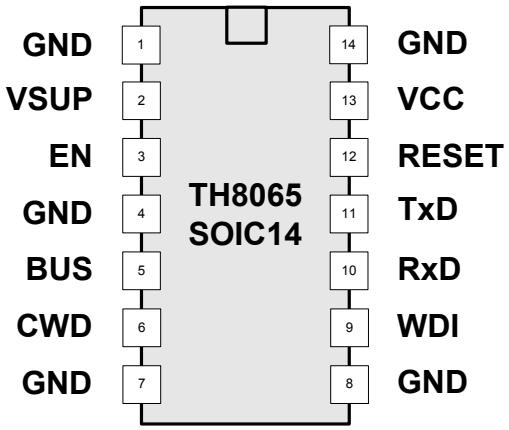
Both outputs are short circuit proof to VCC and ground.

5.11 Short circuit CWD against GND or VCC

The watchdog is deactivated if CWD is short circuit against GND. The reset signal is in this case only determined by the thresholds.

If WDI is short circuit against VCC the reset pin outputs a permanent low level.

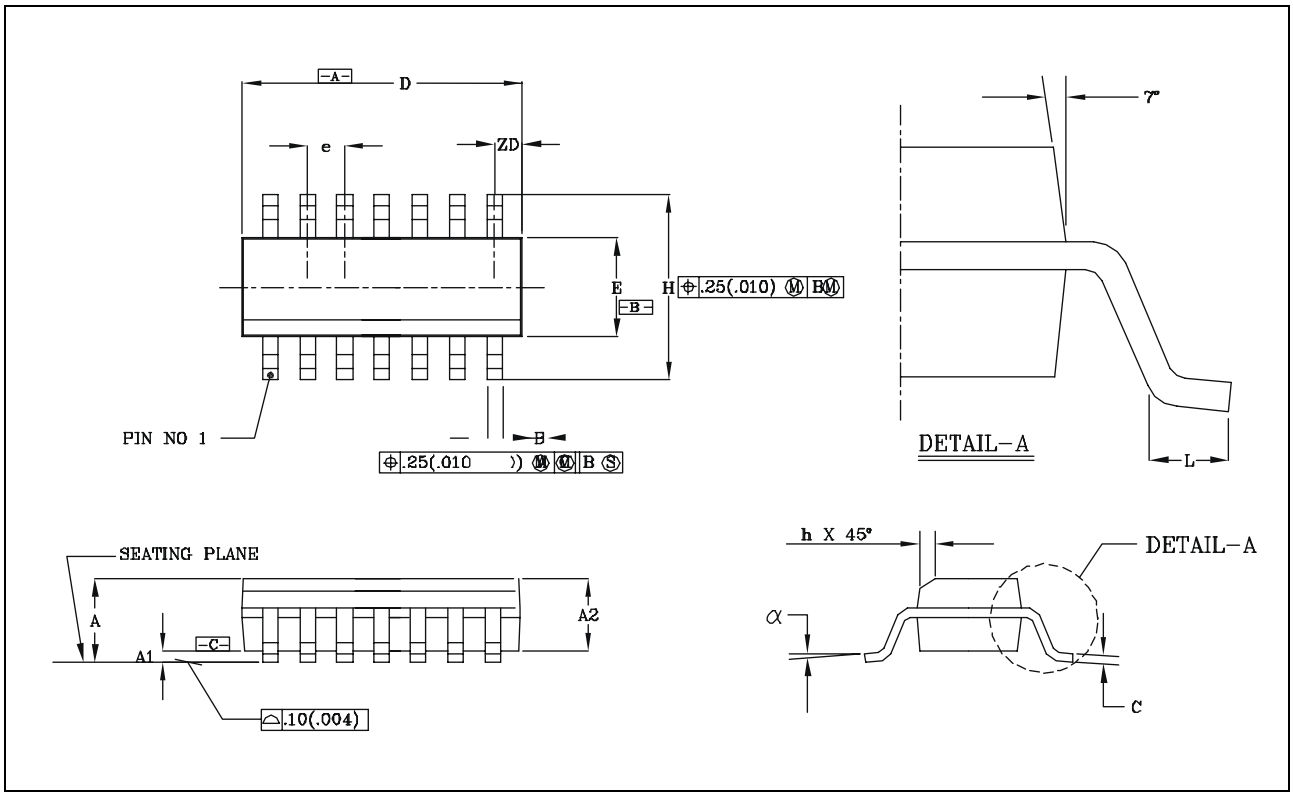
6. PIN Description



Pin	Name	IO-Typ	Description
1	GND	P	Ground
2	VSUP	P	Supply voltage
3	EN	I	Enable input voltage regulator, HV-pull-down-input, High-active
4	GND	P	Ground
5	BUS	I/O	LIN bus line
6	CWD	I/O	Watchdog capacity
7	GND	P	Ground
8	GND	P	Ground
9	WDI	I	Watchdog trigger input, pull down
10	RxD	O	Receive output, 5V-push-pull
11	TxD	I	5V-Transmit input, pull-up-input
12	RESET	O	Reset 5V-output, active low
13	VCC	O	Regulator output 5V/70mA
14	GND	P	Ground

7. Mechanical Specification

SOIC14NB

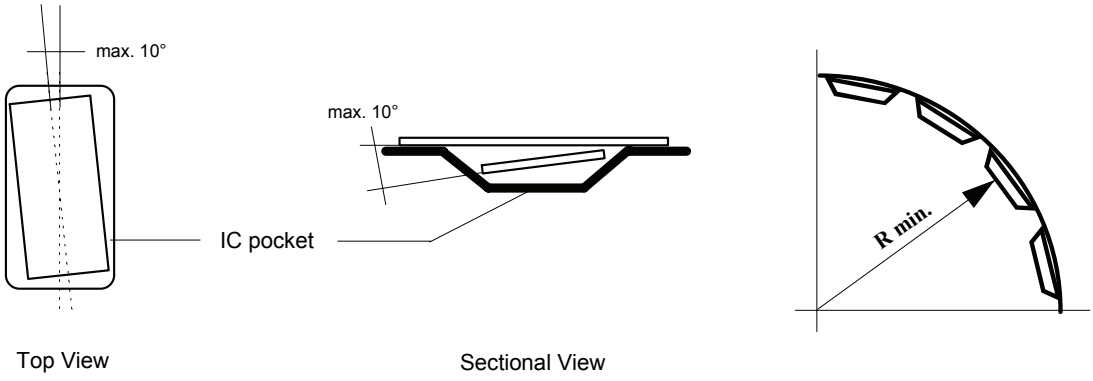


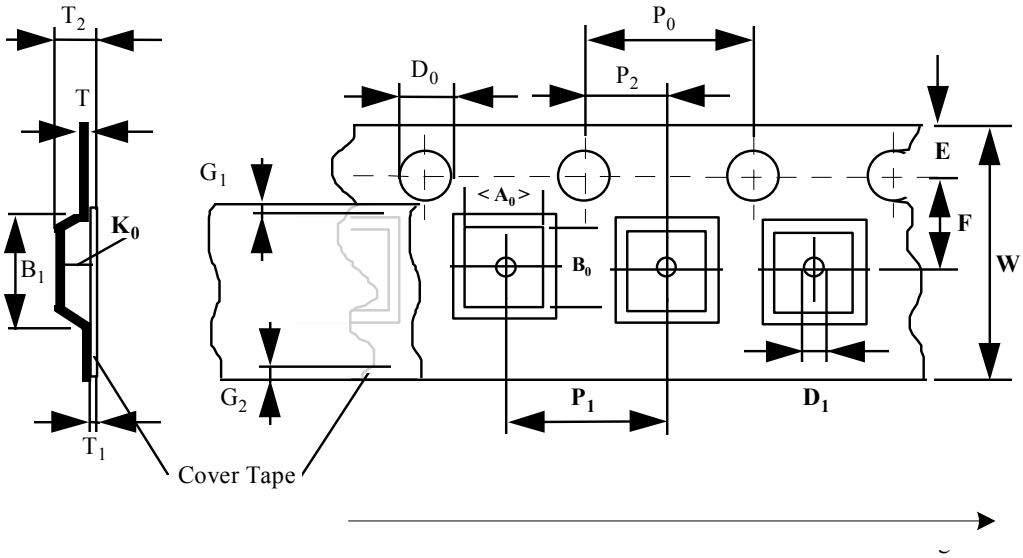
Small Outline Integrated Circiut (SOIC), SOIC 14, 150 mil

	A1	B	C	D	E	e	H	h	L	A	α	ZD	A2
All Dimension in mm, coplanarity < 0.1 mm													
min	0.10	0.36	0.19	8.56	3.81	1.27	5.80	0.25	0.41	1.52	0°	0.51	1.37
max	0.25	0.45	0.25	8.74	3.99		6.20	0.50	1.27	1.72	8°		1.57
All Dimension in inch, coplanarity < 0.004"													
min	0.004	0.014	0.0075	0.337	0.160	0.050	0.228	0.010	0.016	0.060	0°	0.020	0.054
max	0.01	0.018	0.0098	0.344	0.167		0.244	0.020	0.050	0.068	8°		0.062

8. Tape and Reel Specification

8.1 Tape Specification





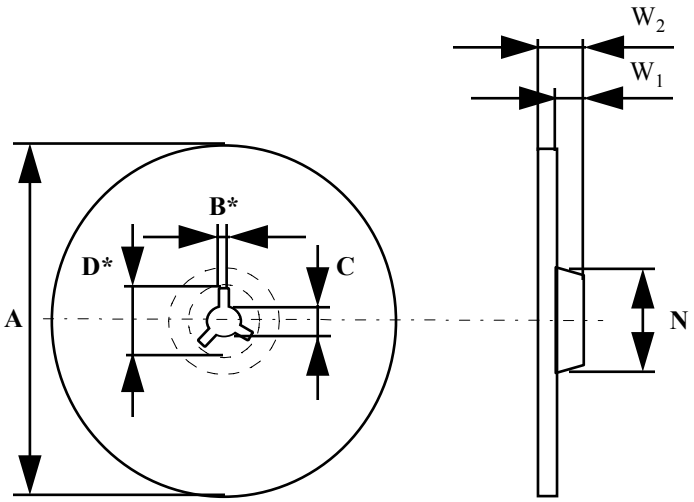
Standard Reel with diameter of 13“

Package	Parts per Reel	Width	Pitch
SOIC14NB	2500	16 mm	8 mm

D_0	E	P_0	P_2	T_{max}	$T_{1\,max}$	$G_{1\,min}$	$G_{2\,min}$	$B_{1\,max}$	$D_{1\,min}$	F	P_1	R_{min}	$T_{2\,max}$	W
1.5 +0.1	1.75 ±0.1	4.0 ±0.1	2.0 ±0.1	0.6	0.1	0.75	0.75	12.1	1.5	7.5 ±0.1	4 - 12 ±0.1	30	8.0	16.0 ±0.3

A_0, B_0, $K_{0\,can}$ be calculated with package specification.
Cover Tape width 13.3 mm.

8.2 Reel Specification



A_{max}	B*	C	D^*_{min}
330	2.0 ±0.5	13.0 +0,5/-0,2	20.2

Width of half reel	N_{min}	W_1	$W_{2\ max}$
8 mm	100,0	8,4	11,1

9. ESD/EMC Remarks

9.1 General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

9.2 ESD-Test

The TH8065 is tested according CDF-AEC-Q100-002 / MIL883-3015.7 (human body model).

9.3 EMC

The test on EMC impacts is done according to ISO 7637-1 for power supply pins and ISO 7637-3 for data- and signal pins.

10. Revision History

Version	Changes	Remark	Date
001		Preliminary Release	Oct. 2004
002	Updated Static Characteristics		April 2005
003	Introduction of variable POR Reset times		May 2006

11. Assembly Information

Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualification of **RoHS** compliant products (RoHS = European directive on the Restriction Of the Use of Certain Hazardous Substances) please visit the quality page on our website:
http://www.melexis.com/quality_leadfree.asp

12. Disclaimer

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.
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