

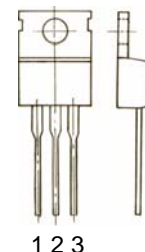
TIP41/41A/41B/41C TRANSISTOR (NPN)

FEATURES

Medium Power Linear Switching Applications

TO-220

1. BASE
2. COLLECTOR
3. EMITTER



MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	TIP41	TIP41A	TIP41B	TIP41C	Units
V_{CB0}	Collector-Base Voltage	40	60	80	100	V
V_{CEO}	Collector-Emitter Voltage	40	60	80	100	V
V_{EBO}	Emitter-Base Voltage	5				V
I_C	Collector Current -Continuous	6				A
P_C	Collector Power Dissipation	2				W
T_J	Junction Temperature	150				$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range	-55to+150				$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{amb}=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	MAX	UNIT	
Collector-base breakdown voltage	TIP41	$I_C=1\text{mA}, I_E=0$	40		V	
	TIP41A		60			
	TIP41B		80			
	TIP41C		100			
Collector-emitter breakdown voltage	TIP41	$I_C=30\text{mA}, I_B=0$	40		V	
	TIP41A		60			
	TIP41B		80			
	TIP41C		100			
Emitter-base breakdown voltage	$V(BR)_{EBO}$	$I_E=1\text{mA}, I_C=0$	5		V	
Collector cut-off current	TIP41	$V_{CB}=40\text{V}, I_E=0$ $V_{CB}=60\text{V}, I_E=0$ $V_{CB}=80\text{V}, I_E=0$ $V_{CB}=100\text{V}, I_E=0$		0.4	mA	
	TIP41A					
	TIP41B					
	TIP41C					
Collector cut-off current	TIP41/41A TIP41B/41C	I_{CEO}	$V_{CE}=30\text{V}, I_B=0$ $V_{CE}=60\text{V}, I_B=0$		0.7	mA
Emitter cut-off current		I_{EBO}	$V_{EB}=5\text{V}, I_C=0$		1	mA
DC current gain		$h_{FE(1)}$	$V_{CE}=4\text{V}, I_C=0.3\text{A}$	30		
		$h_{FE(2)}$	$V_{CE}=4\text{V}, I_C=3\text{A}$	15	75	
Collector-emitter saturation voltage		$V_{CE(sat)}$	$I_C=6\text{A}, I_B=0.6\text{A}$		1.5	V
Base-emitter voltage		$V_{BE(on)}$	$V_{CE}=4\text{V}, I_C=6\text{A}$		2	V
Transition frequency		f_T	$V_{CE}=10\text{V}, I_C=0.5\text{A}$ $f=1\text{MHz}$	3		MHz

Typical Characteristics

TIP41/41A/41B/41C

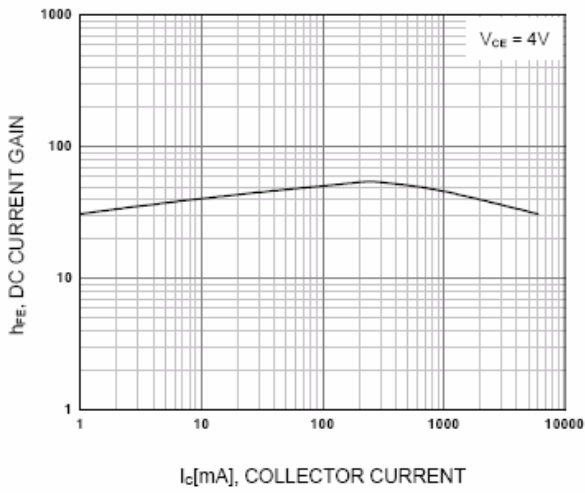


Figure 1. DC current Gain

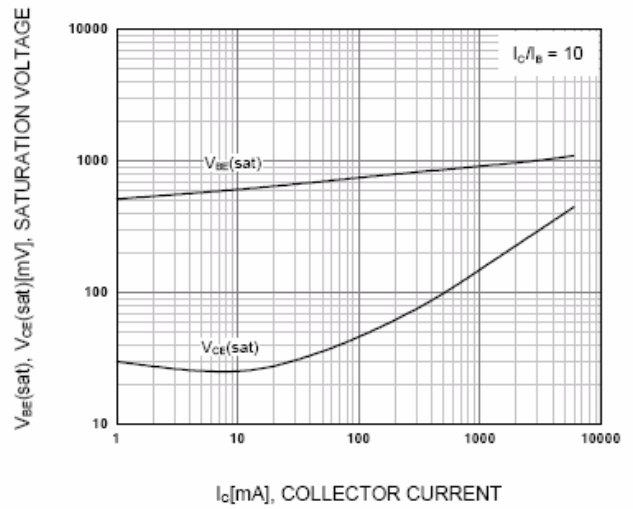


Figure 2. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

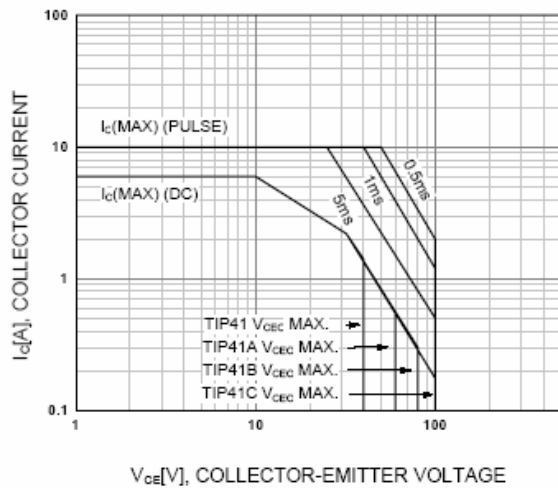


Figure 3. Safe Operating Area

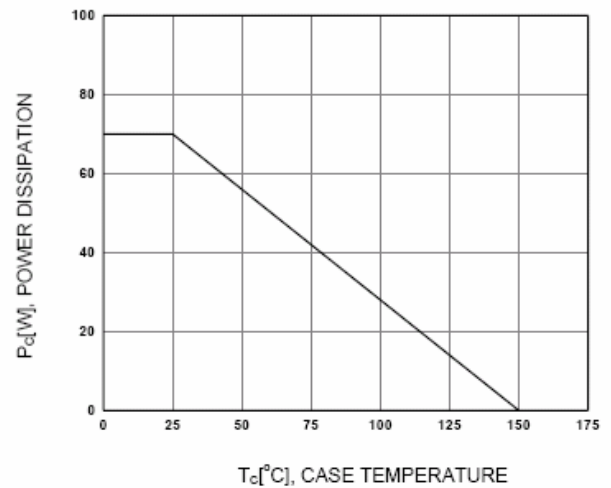


Figure 4. Power Derating