75 Ω VIDEO LINE DRIVER

FEATURES

- **Fixed Gain (6 dB)**
- **Internal 75 Ω Drivers**
- **Very Small Output Capacitor Using SAG Function Pin**
- **Active High ON/OFF Control**
- **Very Low Standby Current (typ. $I_{STBY} \leq 25$ μA)**
- **Very Small SOT23L-8 Package**

APPLICATIONS

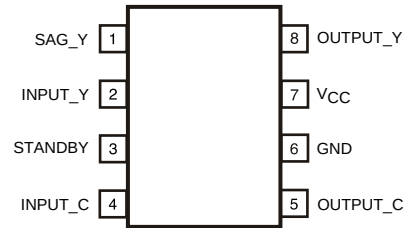
- **Video Equipment**
- **Digital Cameras**
- **CCD Cameras**
- **TV Monitors**
- **Video Tape Recorders**
- **LCD Projectors**

DESCRIPTION

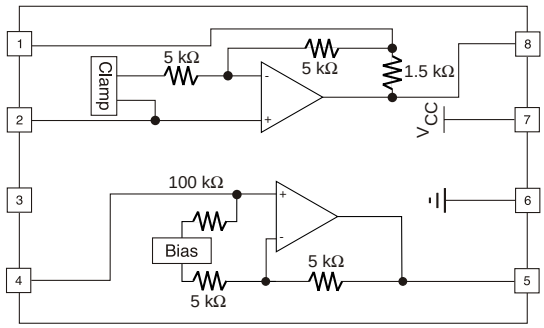
Operating from a single +5 V supply, the TK15407 is a dual video driver IC that takes standard video signals as analog inputs and provides buffered analog outputs for driving 150 Ω loads (series 75 Ω resistor and 75 Ω cable load). Both amplifiers have a fixed gain of 6 dB and can be used in series for 12 dB gain. The luminance (Y) input is clamped at 1.29 V and amplified 6 dB to produce 2 V_{P-P} (typical) into a series 75 Ω resistor and 75 Ω cable load. The internal 1.5 k SAG function resistor provides gain compensation for low frequency signals. The chromanance (C) input is biased at 2.6 V and amplified 6 dB to produce 1.1 V_{P-P} (typical) into a series 75 Ω resistor and 75 Ω cable load. During standby (Pin 3 grounded), the TK15407 consumes only 119 μW of power. Nominal power dissipation (no input) is typically 76 mW. The TK15407 is ideally suited for S-VHS systems.

The TK15407M is available in the very small SOT23L-8 surface mount package.

TK15407



BLOCK DIAGRAM



ORDERING INFORMATION

TK15407M □□

Tape/Reel Code

TAPE/REEL CODE
TL: Tape Left

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 6 V
Operating Voltage Range..... 4.5 to 5.5 V
Power Dissipation (Note 1) ..... 200 mW
Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range .....-25 to +75 °C

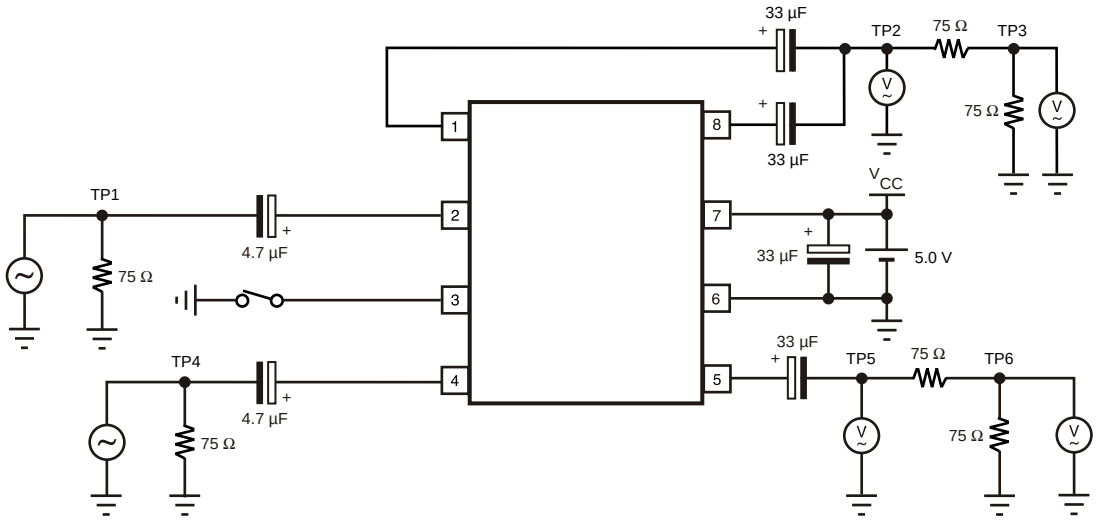
TK15407M ELECTRICAL CHARACTERISTICS

Test conditions: V_{CC} = 5.0 V, V_{IN} = 1.0 V_{P-P}, R_L = 150 Ω, T_A = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Supply Current	No input		15.1	21.0	mA
I_{STBY}	Standby Supply Current	Pin 3 Grounded		23.8	50.0	µA
I_{OS}	Standby Terminal Current	Pin 3 in Standby mode		23.8	50.0	µA
V_{THL}	Threshold Voltage (High to Low)	Pin 3 Operating to Standby mode	GND	0.1	0.3	V
V_{TLH}	Threshold Voltage (Low to High)	Pin 3 Standby to Operating mode	1.8	2.0	V_{CC}	V
V_{CMP}	Clamp Voltage	Pin 2 Y Signal Input terminal	1.10	1.29	1.50	V
V_{BIAS}	Bias Voltage	Pin 4 C Signal Input terminal	2.35	2.66	2.95	V
GVA	Voltage Gain	f_{in} = 1 MHz	5.2	5.7	6.2	dB
DG	Differential Gain (Y Signal)	Staircase signal input	-3.0	+1.3	+3.0	%
DP	Differential Phase (Y Signal)	Staircase signal input	-3.0	0.0	+3.0	deg
fr	Frequency Response	f_{in} = 1 MHz / 5 MHz		-0.3		dB
THD	Total Harmonic Distortion (C Signal)	f_{in} = 1.0 kHz		0.4	1.5	%
$V_{OUT(MAX)}$	Maximum Output Voltage (C Signal)	THD = 10% point	0.9	1.1		Vrms

Note 1: Power dissipation is 200 mW in free air. Derate at 1.6 mW/°C for operation above 25°C.

TEST CIRCUIT



MEASUREMENT METHOD

1. Supply Current (I_{CC})
The Pin 7 current is measured with no input signal and the Standby Pin (Pin 3) open.

2. Standby Supply Current (I_{STBY})
The Pin 7 current is measured when the Standby Pin (Pin 3) is connected to ground.

3. Standby Terminal Current (I_{OS})
The Pin 3 current is measured when Pin 3 is connected to ground.

4. Threshold Voltage (High to Low) (V_{THL})
The Pin 3 voltage is measured at the point which changes the device from operating mode into standby mode.

5. Threshold Voltage (Low to High) (V_{TLH})
The Pin 3 voltage is measured at the point which changes the device from standby mode into operating mode.

6. Clamp Voltage (V_{CMP})
The DC voltage at Pin 2 is measured with no input signal.

7. Bias Voltage (V_{BIAS})
The DC voltage at Pin 4 is measured with no input signal.

8. Voltage Gain (GVA)
The voltage gain equation is as follows:
$GVA = 20 \log_{10} V2/V1$
Where V1 is the input voltage at TP1 (TP4) and V2 is the measured voltage at TP2 (TP5).

9. Differential Gain (DG)
The differential gain is measured at TP3 when a staircase waveform of 10 steps is applied to TP1.

MEASUREMENT METHOD (CONT.)

10. Differential Phase (DP)
The differential phase is measured at TP3 when a staircase waveform of 10 steps is applied to TP1.

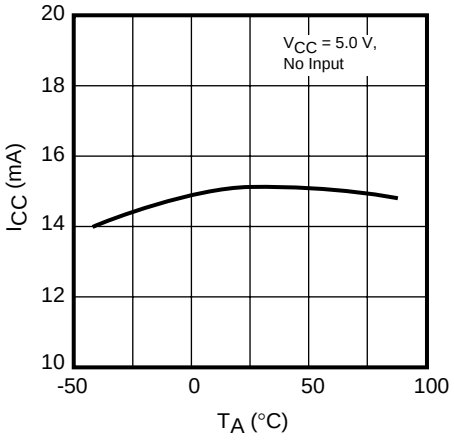
11. Frequency Response (fr)
The frequency response equation is as follows:
$fr = 20 \log_{10} V2/V1$
Where V1 is the measured TP3 (TP6) voltage when the TP1 (TP4) input frequency is set to 1 MHz and V2 is the measured TP3 (TP6) voltage when the TP1 (TP4) input frequency is set to 5 MHz.

12. Total Harmonic Distortion (THD)
The TP6 signal is measured when a 1 kHz 1 V_{P-P} input signal is applied to TP4.

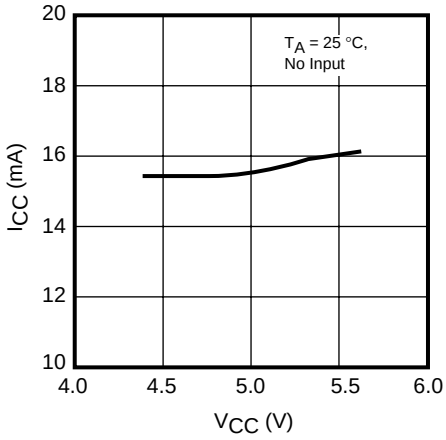
13. Maximum Output Voltage ($V_{OUT(MAX)}$)
A 1 kHz input signal is applied to TP4 and the amplitude is slowly increased. The output voltage at TP5 is measured at the point the THD reaches 10%.

TYPICAL PERFORMANCE CHARACTERISTICS

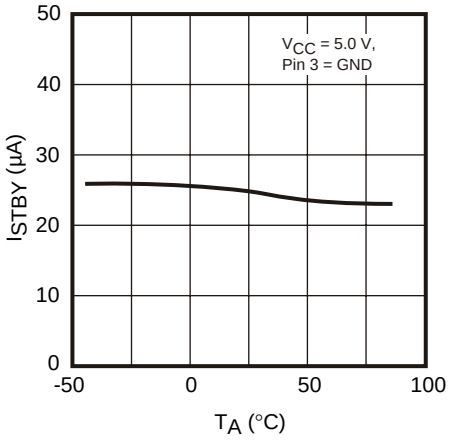
SUPPLY CURRENT vs. TEMPERATURE



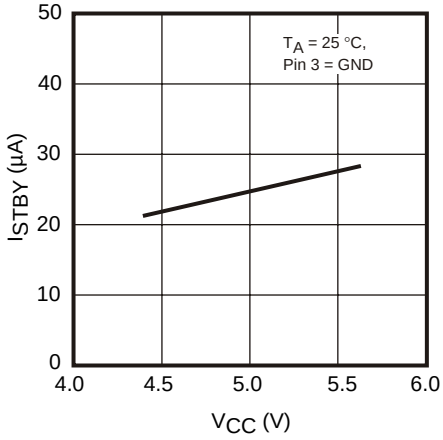
SUPPLY CURRENT vs. SUPPLY VOLTAGE



STANDBY SUPPLY CURRENT vs. TEMPERATURE

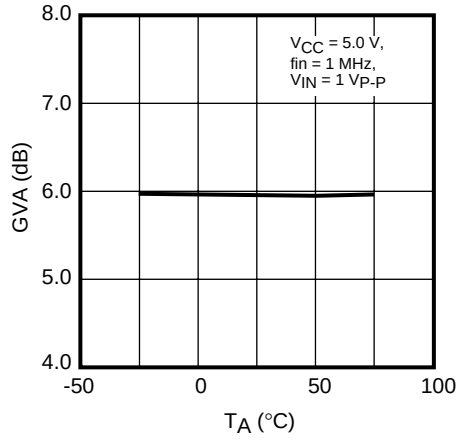


STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

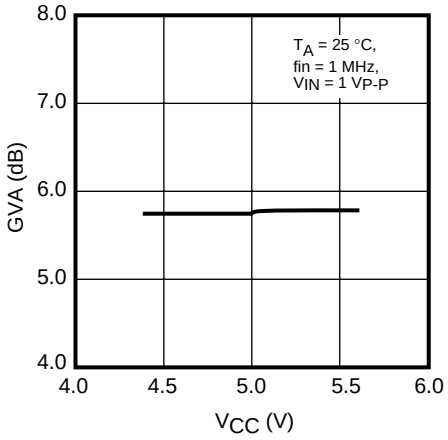


TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

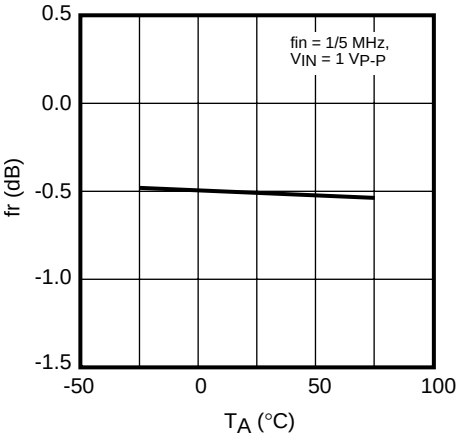
VOLTAGE GAIN vs. TEMPERATURE



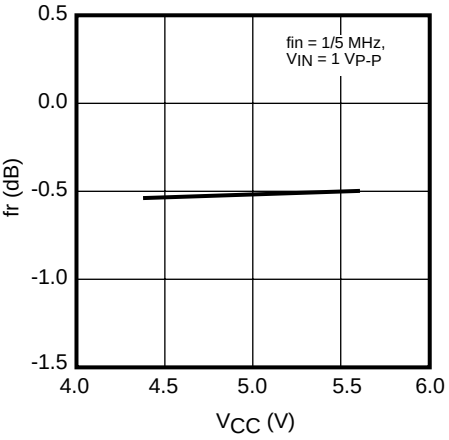
VOLTAGE GAIN vs. SUPPLY VOLTAGE



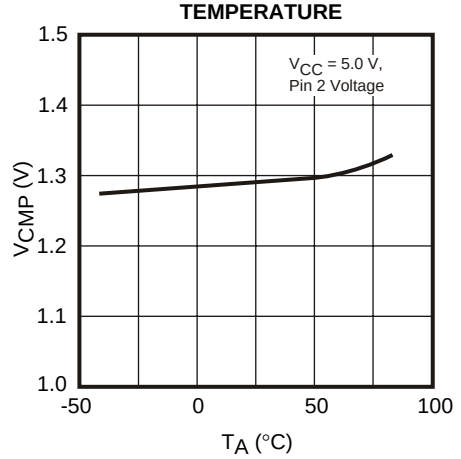
FREQUENCY RESPONSE vs. TEMPERATURE



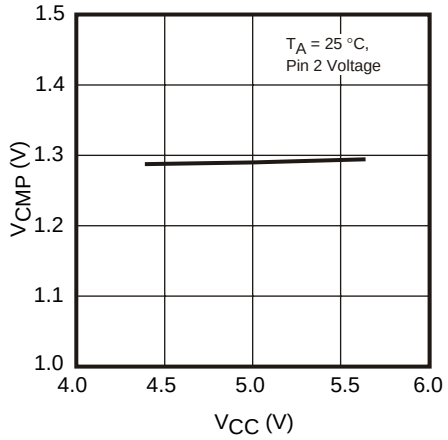
FREQUENCY RESPONSE vs. SUPPLY VOLTAGE



CLAMP VOLTAGE vs. TEMPERATURE

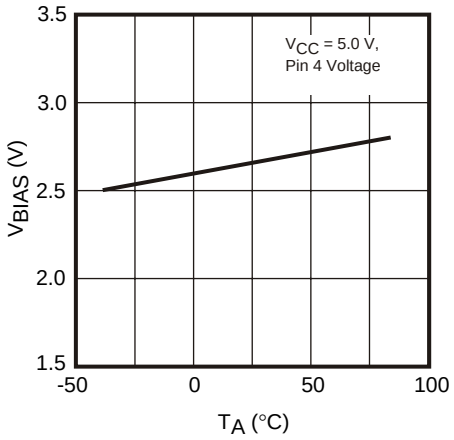


CLAMP VOLTAGE vs. SUPPLY VOLTAGE

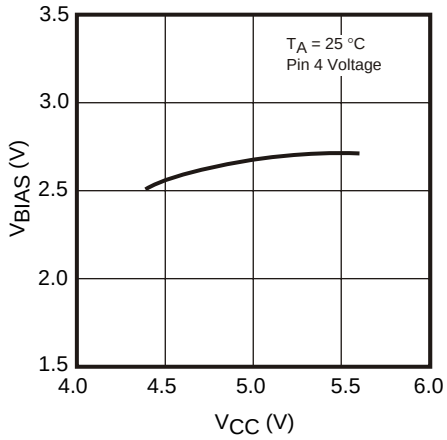


TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

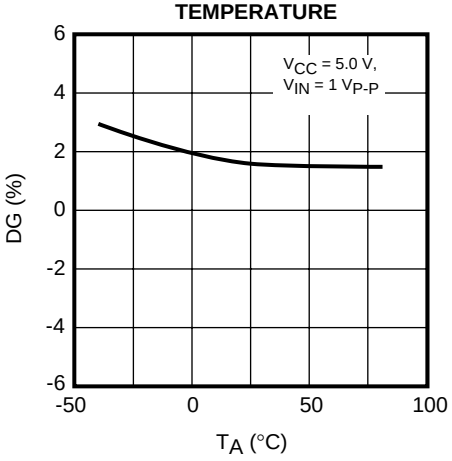
BIAS VOLTAGE vs. TEMPERATURE



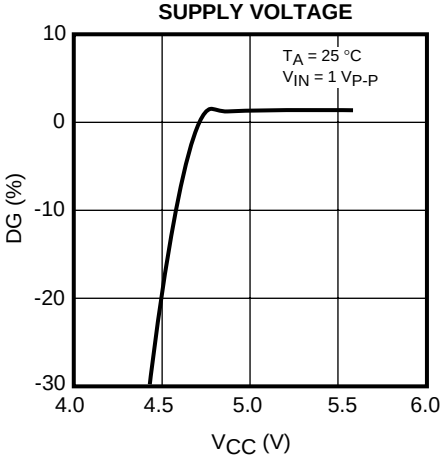
BIAS VOLTAGE vs. SUPPLY VOLTAGE



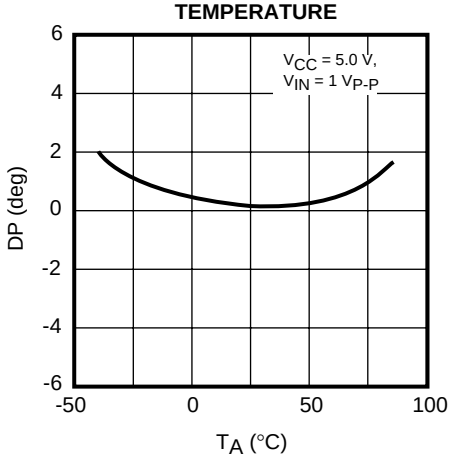
DIFFERENTIAL GAIN vs. TEMPERATURE



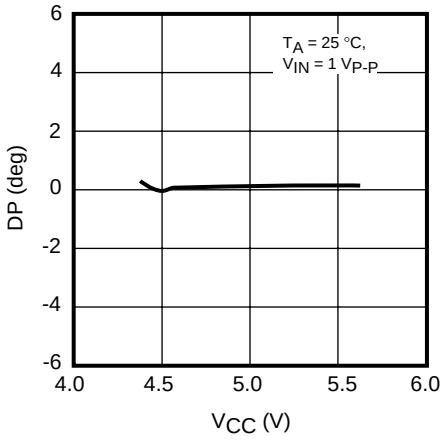
DIFFERENTIAL GAIN vs. SUPPLY VOLTAGE



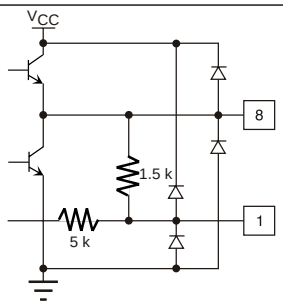
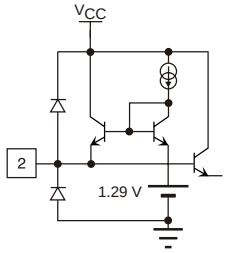
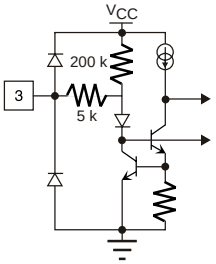
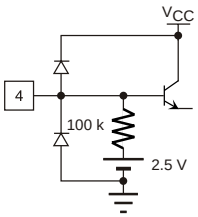
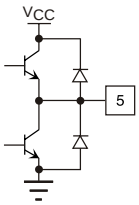
DIFFERENTIAL PHASE vs. TEMPERATURE



DIFFERENTIAL PHASE vs. SUPPLY VOLTAGE

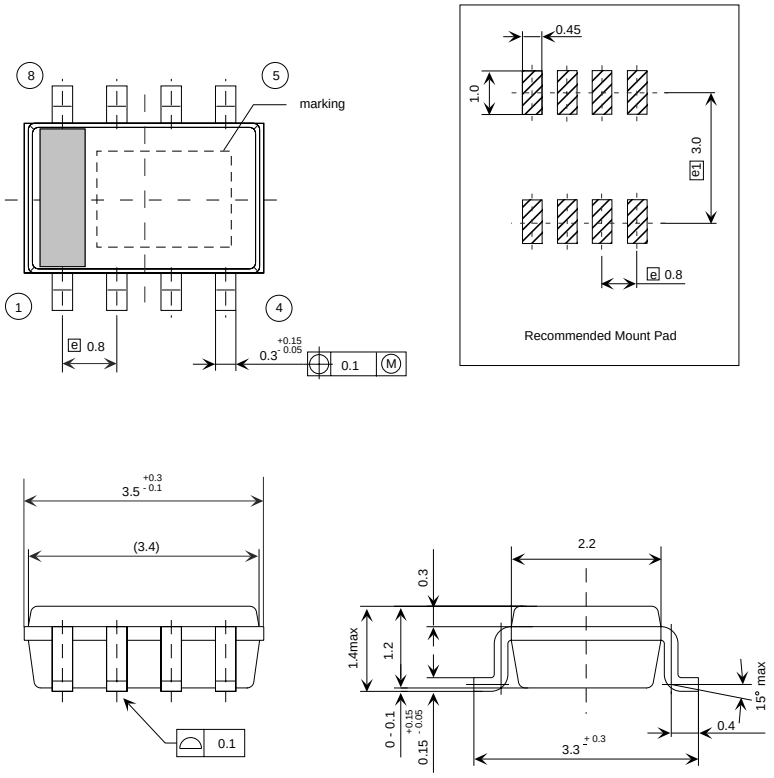


PIN FUNCTION DESCRIPTIONS

TERMINAL			INTERNAL EQUIVALENT CIRCUIT	DESCRIPTION
PIN NO.	SYMBOL	VOLTAGE		
8 1	OUTPUT_Y SAG_Y	1.6 V 1.4 V		Pin 8: Luminance Output terminal. The Luminance output is available to drive 75 Ω + 75 Ω load. Pin 1: SAG terminal
2	INPUT_Y	1.3 V		Luminance Input terminal. The luminance input signal is clamped at 1.29 V.
3	STANDBY	2.1 V		Standby Logic terminal. The device is in the standby mode when Pin 3 is connected to Low. The device is in the operating mode when Pin 3 is connected to High or Open.
4	INPUT_C	2.6 V		Chromanance Input terminal. The chromanance input signal is biased by a 100 kΩ Bias Resistance.
5	OUTPUT_C	2.8 V		Chromanance Output terminal. The chromanance output is available to drive 75 Ω + 75 Ω load.
6	GND	GND		GND terminal.
7	V_{CC}	V_{CC}		Power Supply terminal.

PACKAGE OUTLINE

SOT23L-8



Dimensions are shown in millimeters
Tolerance: x.x = ± 0.2 mm (unless otherwise specified)

Marking Information

	Marking
TK15407	407

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