Dual XAUI Transceiver

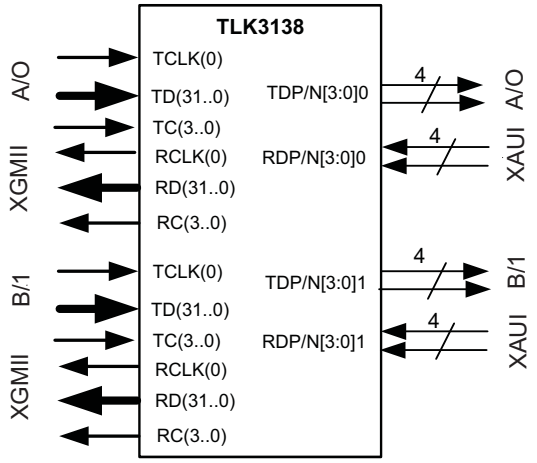
FEATURES

- **Eight Channel 3.125 Gbps Transceiver**
- **Contains Two Complete IEEE P802.3ae-2002 10 Gbps Ethernet XGXS(1) (XAUI) Compliant Cores**
- **XAUI (Serial side) Channel Redundancy Mode Support: Fast Switching from Primary to Secondary XAUI/Channel with Provisionable Error Character or Local Fault Code Insertion at Switch Time**
- **XGMII (Parallel side) Channel Redundancy Mode Support: Fast Switching from Primary to Secondary XGMII/Channel with Provisionable Error Character or Local Fault Code Insertion at Switch Time**
- **Serial Side Transmit Pre-emphasis and Receive Adaptive Equalization to Allow Extended Backplane Reach**
- **Selectable Full Duplex Serial Side Retimer Mode**
- **Full Datapath Loopback Capability (Serial/Parallel Side)**
- **Support PRBS 2^7-1 and 2^{23}-1 Generate/Verify. Support Standard Defined CJPAT, CRPAT, High Frequency, Low Frequency, and Mixed Frequency Testing**
- **XGMII: HSTL Class 1 I/O with On-chip 50-Ω Termination on Inputs/Outputs (1.5-V Power Supply)**
- **XGMII: Support Receive (Output) Aligned/Centered Timing Modes, and Transmit (Input) Source Centered Mode**
- **Supports Jumbo Packet (9600 byte maximum) Operation**
- **Align Character Skew Support of 30 bit Times at Chip Pins**
- **Dual MDIO: IEEE 802.3ae Clause 45 Compliant Management Data Input / Output Interface (1.2-V and 2.5-V I/O)**
- **1.2-V Core, 1.5-V HSTL I/O Supply, and 2.5-V LVCMOS and Bias Supply**
- **JTAG: IEEE 1149.1 Test Interface**
- **±200 ppm Clock Tolerance in XAUI Transmit and Receive Datapaths**
- **Diagnostic LED Output Interface**
- **130-nm CMOS Technology**
- **Package: PBGA 484, 23×23mm, 484 ball, 1mm Pitch**
- **2.42 W Typical Power Dissipation (Dual XAUI Mode, Input HSTL Termination Disabled)**
- **Commercial Ambient Operating Temp (0°C to 70°C)**

(1) XGMII Extender Sublayer

APPLICATIONS

- **10 Gigabit Ethernet Servers and Routers**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The TLK3138 is an eight channel serial transceiver. It is compliant with the 10Gbps Ethernet XAUI specification. The TLK3138 provides 10 Gbps high-speed bi-directional point-to-point data transmission. The primary application of this device is in backplanes and front panel connections requiring dual/redundant 10Gbps connections over controlled impedance media of approximately 50Ω. The transmission media can be printed circuit board (PCB) traces, copper cables or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling into the lines.

The TLK3138 performs the parallel-to-serial, serial-to-parallel conversion, and clock extraction functions for a physical layer interface. The TLK3138 provides two complete XGXS/PCS functions defined in Clause 47/48 of the IEEE P802.3ae 10Gbps Ethernet standard. The serial transmitter is implemented using differential Current Mode Logic (CML) with integrated termination resistors.

The TLK3138 can be configured as a dual XAUI transceiver. TLK3138 supports two 32-bit data path, 4-bit control, 10 Gigabit Media Independent Interfaces (XGMII) to the protocol device(s). Figure 1 shows an example system block diagram for TLK3138 used to provide the 10Gbps Ethernet Physical Coding Sublayer to Coarse Wave-length Division Multiplexed optical transceiver or parallel optics.

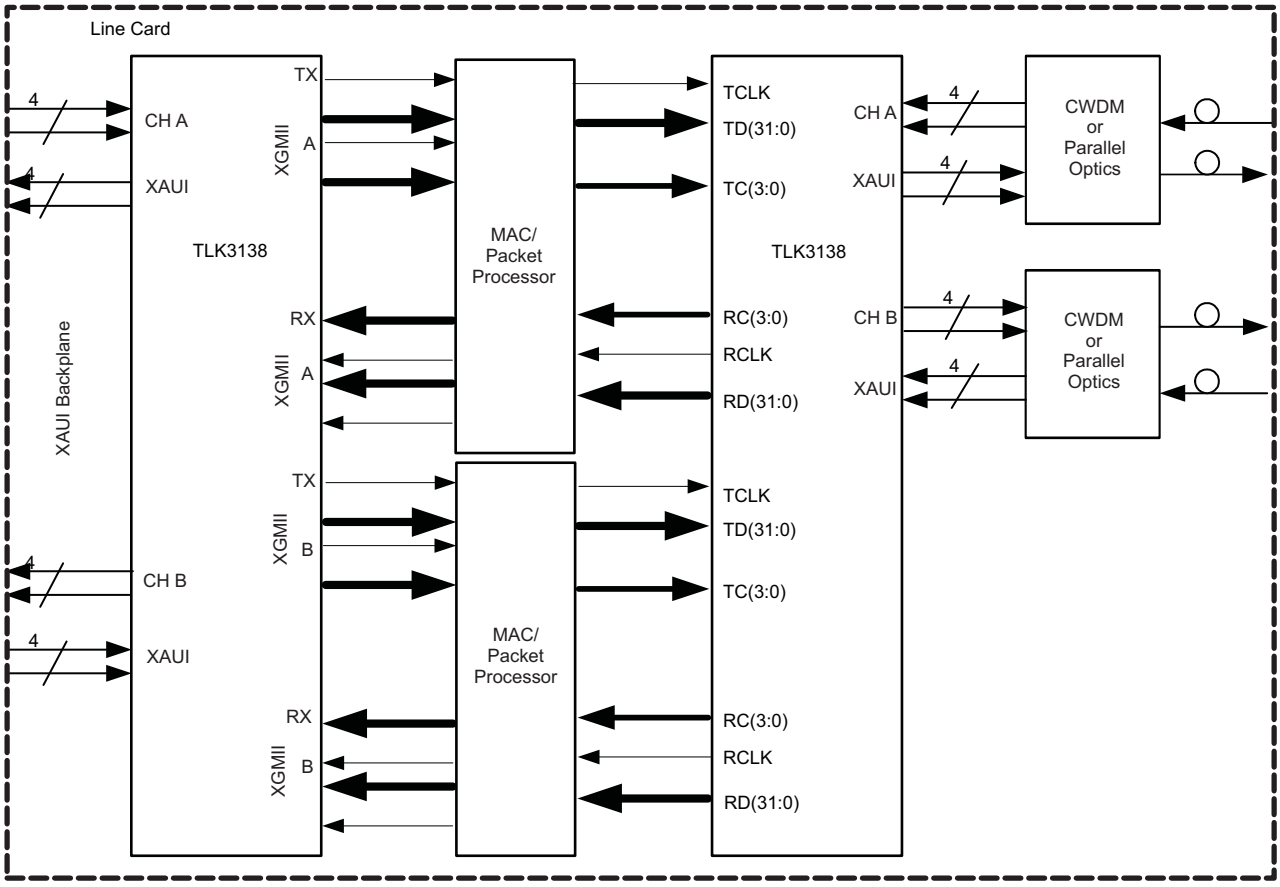


Figure 1. System Block Diagram – PCS

Figure 2 shows an example system block diagram for TLK3138 used to provide the system backplane interconnect.

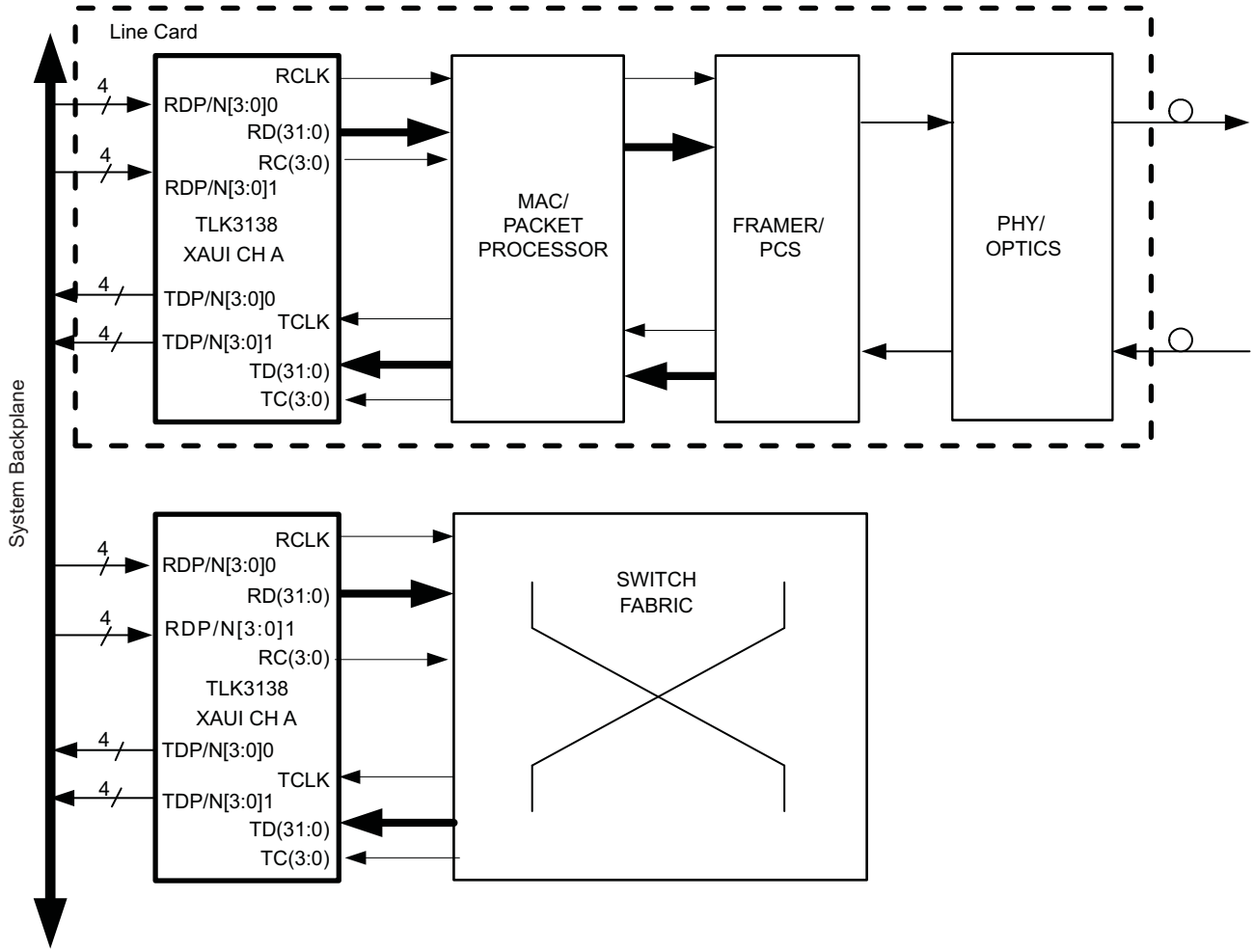


Figure 2. System Block Diagram – XAUI Backplane

Figure 3 shows the TLK3138 in a Dual XAUI Application:

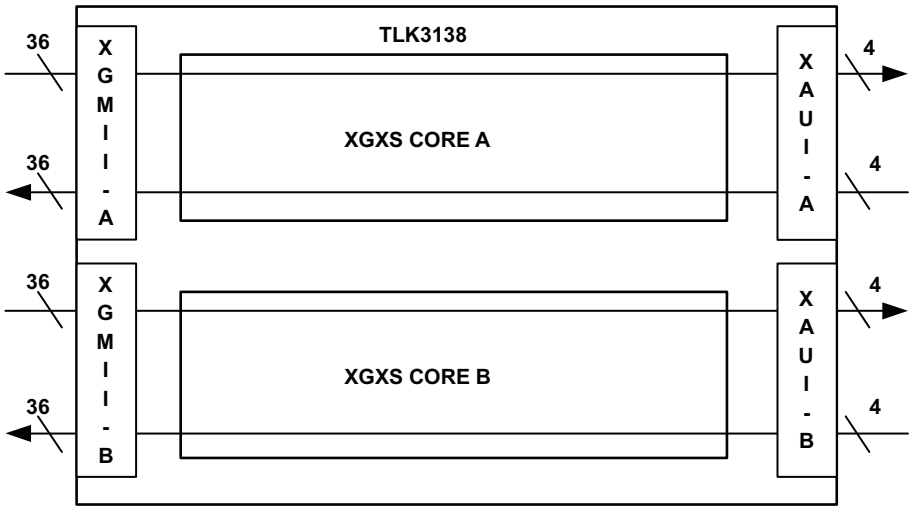


Figure 3. DUAL XAUI Application

Figure 4 shows the TLK3138 in a XAUI Retimer Application

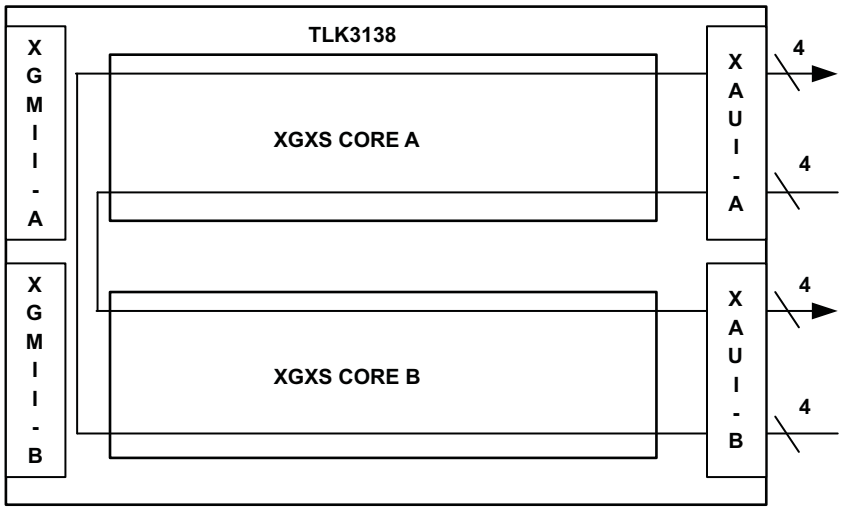


Figure 4. XAUI Retimer Application

Figure 5 shows the TLK3138 in a Redundant XAUI Application.

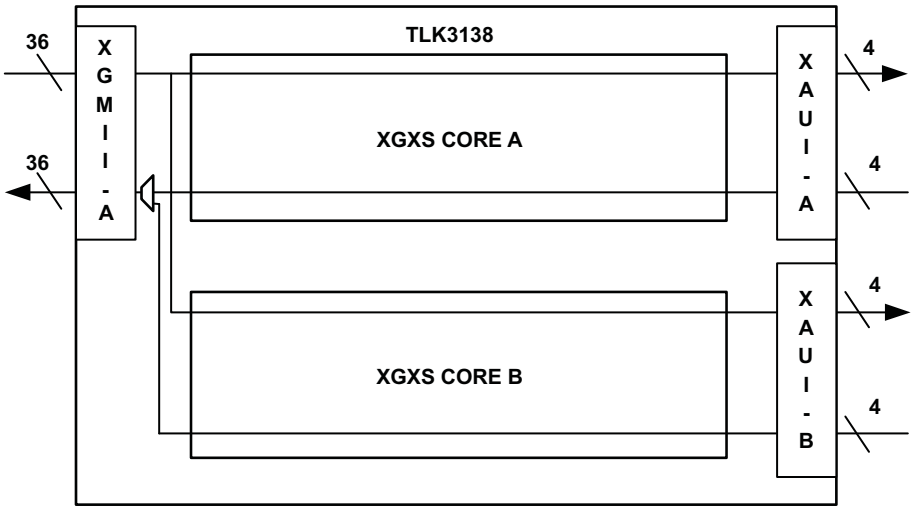


Figure 5. Redundant XAUI Application

Figure 6 shows the TLK3138 in a Redundant XAUI Application.

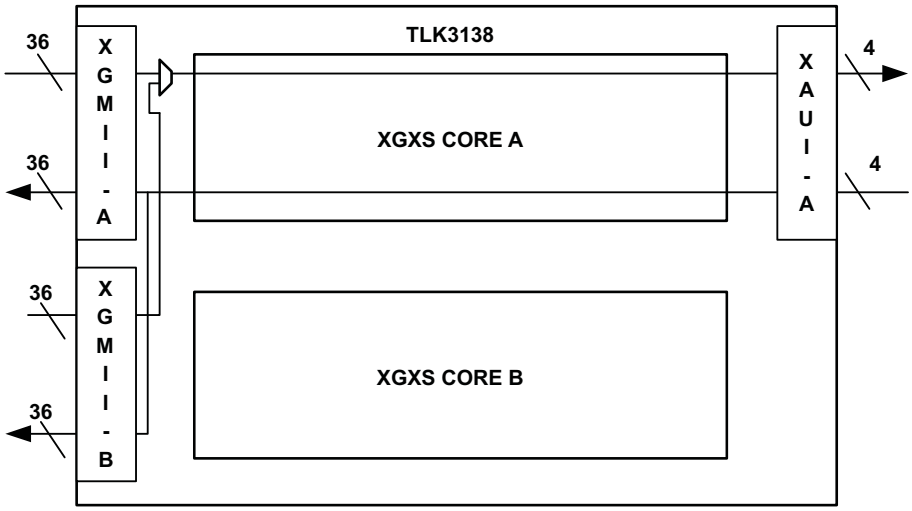


Figure 6. Redundant XGMII Application

Figure 7 shows the TLK3138 in a XAUI Loopback Application.

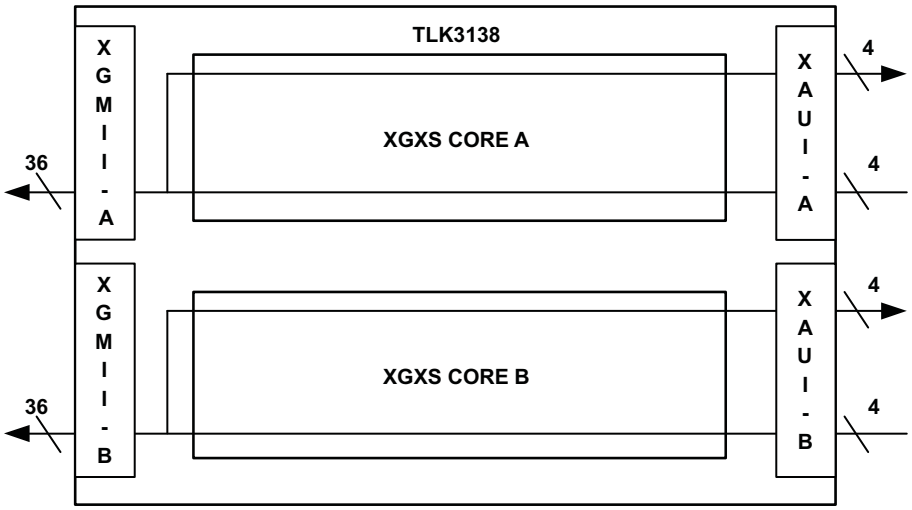


Figure 7. XAUI Loopback Application

Figure 8 shows the TLK3138 in a XGMII Loopback application.

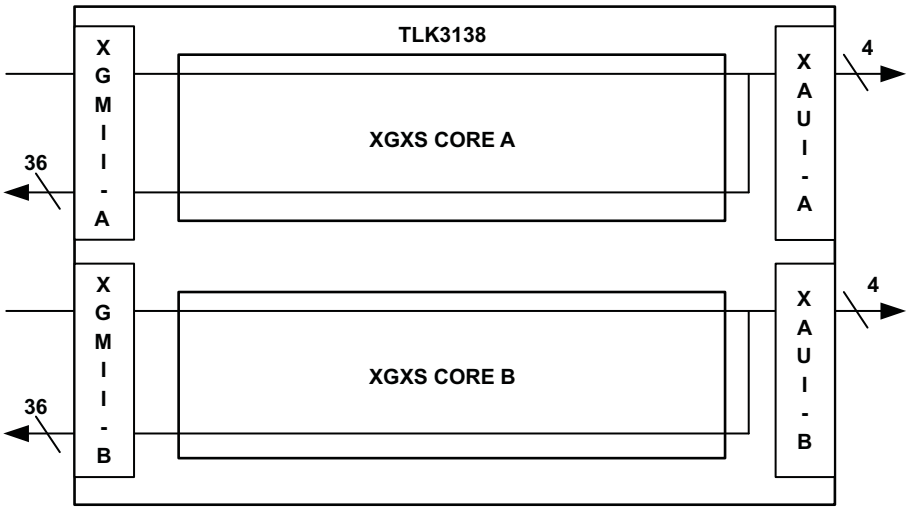


Figure 8. XGMII Loopback Application

It is possible to select non-conflicting modes of operation based on the following bits:

XAUI_RETIME (See Register Bit 4/5. 32907.2 for definition)

REDUNDANT_XAUI (See Register Bit 4/5.32907.6 for definition)

REDUNDANT_XGMII (See Register Bit 4/5.32907.7 for definition)

XGMII_LOOPBACK (See Register Bit 4/5.32792. 0 for definition (1 bit for each XGXS Core))

XAUI_LOOPBACK (See Register Bit 4/5.32792. 1 for definition (1 bit for each XGXS Core))

The TLK3138 supports the IEEE 802.3 defined Management Data Input/Output (MDIO) Interface to allow ease in configuration and status monitoring of the link. The bi-directional data pin (MDIO) should be externally pulled up to 1.2V or 2.5V per the standard for both MDIO0 and MDIO1.

The TLK3138 supports the IEEE 1149.1 defined JTAG test port for ease in board manufacturing test. It also supports a comprehensive series of built-in tests for self-test purposes including PRBS generation and verification, CRPAT, CJPAT, Mixed/High/Low Frequency testing.

The TLK3138 operates with a 1.2V core voltage supply, a 1.5V HSTL I/O voltage supply and a 2.5V bias supply.

The TLK3138 is packaged in a 23×23mm, 484-ball, 1mm ball pitch Plastic Ball Grid Array (PBGA) package and is characterized for operation from 0°C to 70°C Ambient, 115°C Junction, and 5% power supply variation unless noted otherwise. Note that the junction temperature must be kept below 115°C to meet TI C035 process reliability.

BLOCK DIAGRAMS

Figure 9 provides a high level description of the TLK3138 block diagram.

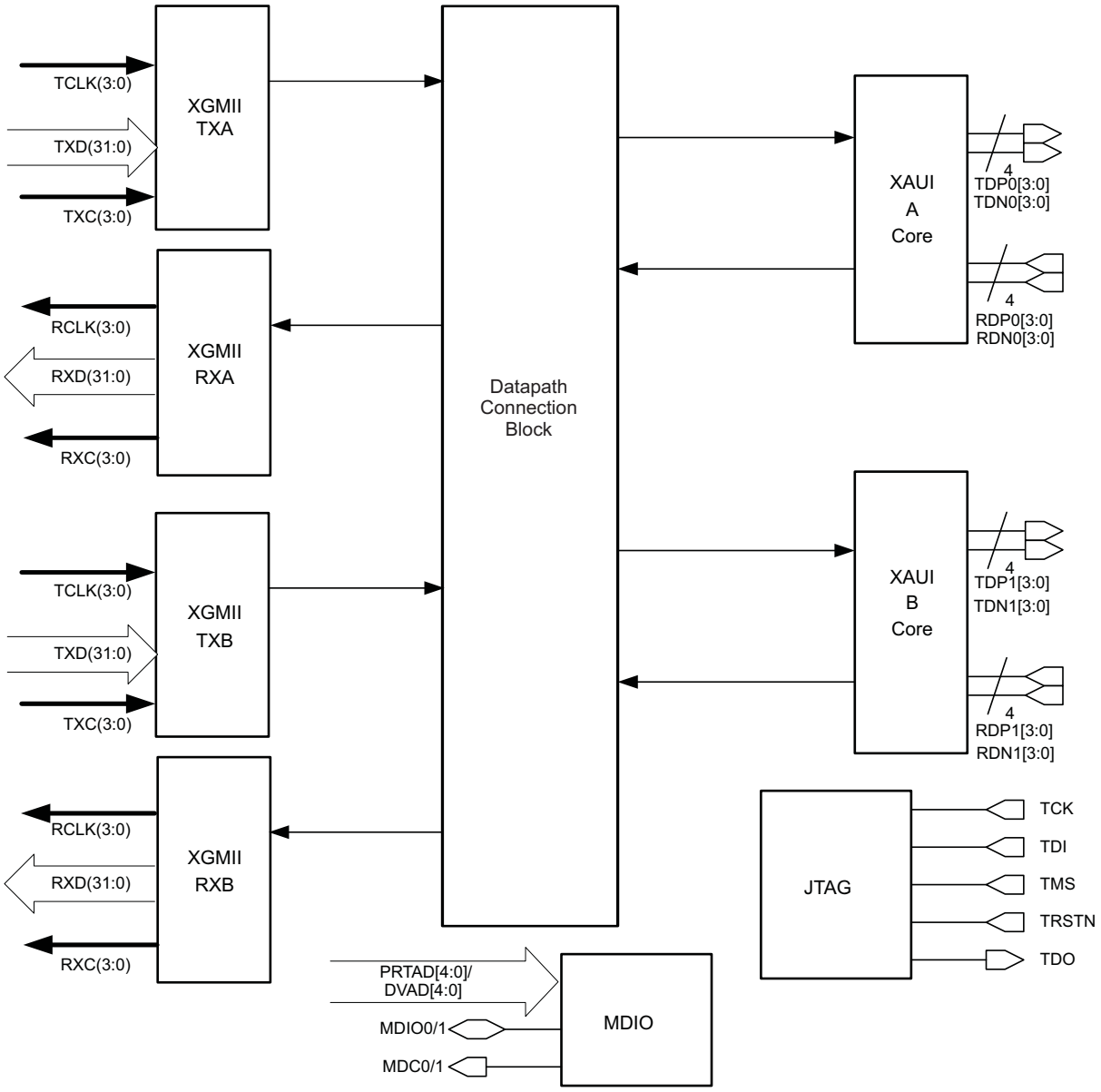


Figure 9. TLK3138 Block Diagram

Figure 10 is a more detailed block diagram description of XAUI core.

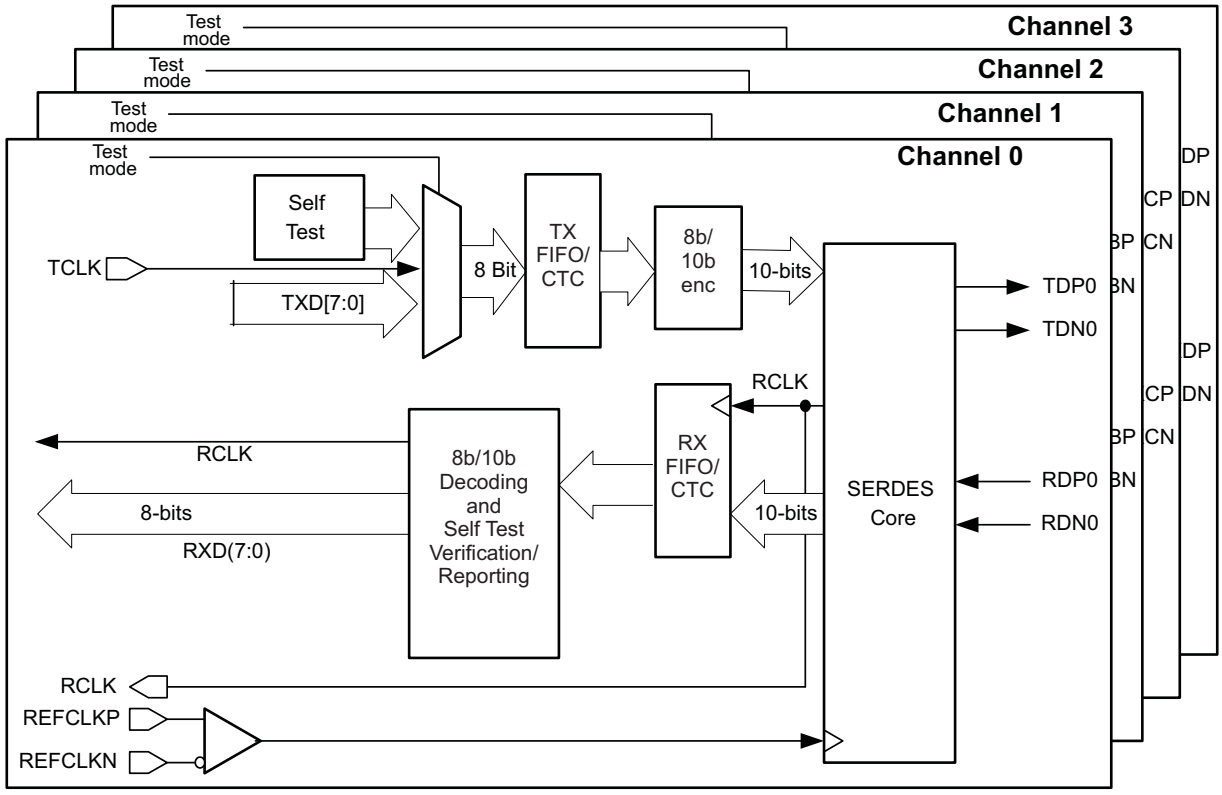


Figure 10. Detailed XAUI Core Block Diagram

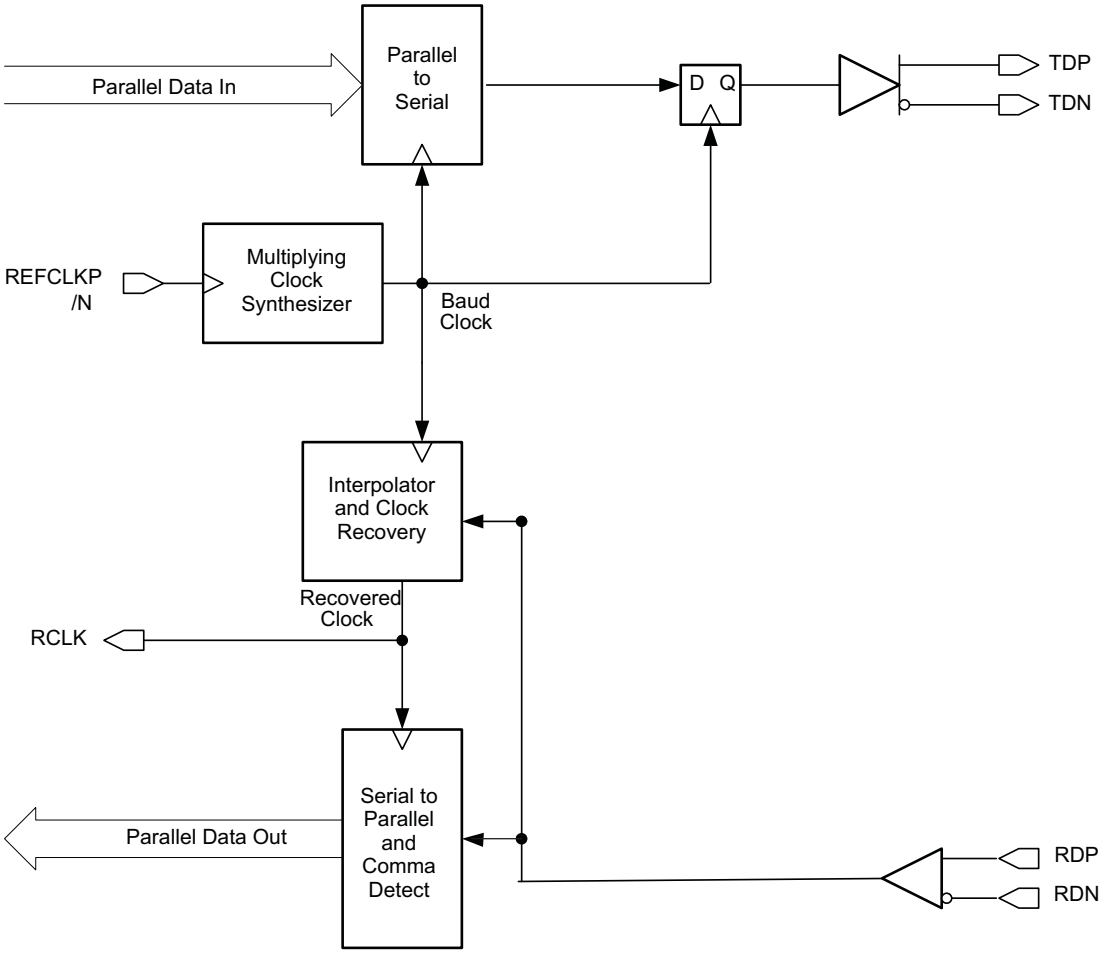


Figure 11. Block Diagram of SERDES Core

DETAILED DESCRIPTION

The TLK3138 has several operational interface modes controlled by register bits A/B and XAUI_RETIME, REDUNDANT_XAUI, and REDUNDANT_XGMII. The major modes of application are discussed below.

REDUNDANT XAUI OPERATION

The TLK3138 can operate as a redundant XAUI transceiver.

In Redundant XAUI MODE (4/5.32907.6), only the A side XGMII interface is active, and both serial interfaces XAUI A and XAUI B are active. It is possible for B side XGMII to receive B side serial data, but the transmit XGMII B interface is ignored. The transmit datapath either duplicates the transmit XGMII data to both serial side data streams, or if the IDLE mode is selected, send only valid A/K/R (idle) sequences on the deselected side. The receive datapath selects one of the two aggregated input serial streams controlled by the A_B (4/5.32907.3) register bit.

While communication is occurring on the primary selected channel, the secondary channel is fully functional capable of transmitting and receiving data. All registers are accessible and valid. The only difference between the primary and secondary channels is the primary channel is routed to the A side XGMII receive bus.

A completely active secondary channel allows transition from primary to secondary channels within a few clock cycles. During the transition, the data on each byte of the bus is 0xFE (code violation), which is the ERROR indication, or local fault indication (based on a provisioned register value).

DETAILED DESCRIPTION (continued)

REDUNDANT XGMII OPERATION

The TLK3138 can operate as a redundant XGMII transceiver.

In Redundant XGMII MODE (4/5.32907.7), only the A side Serial interface is active, and both Parallel interfaces XGMII A and XGMII B are active. It is possible for B side XAUI to transmit B side parallel data, but the receive XAUI B interface is processed but not used. The receive datapath either duplicates the receive XAUI data to both parallel side data streams, or if the IDLE mode is selected, send only valid (idle) sequences on the deselected side. The transmit datapath selects one of the two aggregated input parallel streams controlled by the A_B (4/5.32907.3) register bit.

While communication is occurring on the primary selected channel, the secondary channel is fully functional capable of transmitting data (if desired). All B side transmit related registers are accessible and valid.

During the transition, the data on each byte of the bus is 0xFE (code violation), which is the ERROR indication, or local fault indication (based on a provisioned register value).

RETIMER OPERATION

The TLK3138 can operate as a full duplex serial side re-timer. All the functions of transceiver operations are performed except for the XGMII input interfaces, and optionally the XGMII output interfaces. The recovered data on each XAUI channel is de-serialized, de-skewed, aligned to the reference clock, and re-serialized. In the re-timer mode inputs from the XGMII inputs are ignored. XGMII outputs can provisionally be left on to snoop received data, or turned off to save power.

Note that when RETIM is high, the serial side A receive data is routed out to the serial side B transmit serial lines. Similarly, the serial side B receive data is routed out to the serial side A transmit serial lines.

If A/B is toggled when in re-timer monitor mode, the data on each byte of the XGMII receive output bus (if not in 3-state) is 0xFE (code violation) for several XGMII clock cycles, or local fault (based on the provisioned register value).

PARALLEL CLOCKING MODES

The TLK3138 supports source-centered timing and source-aligned timing on the XGMII receive output bus. The source-centered timing supported is the timing defined in P802.3ae Clause 46, with the RX_CLK centered within the receive output data bit timing, as shown in Figure 12. Also shown is source-aligned timing.

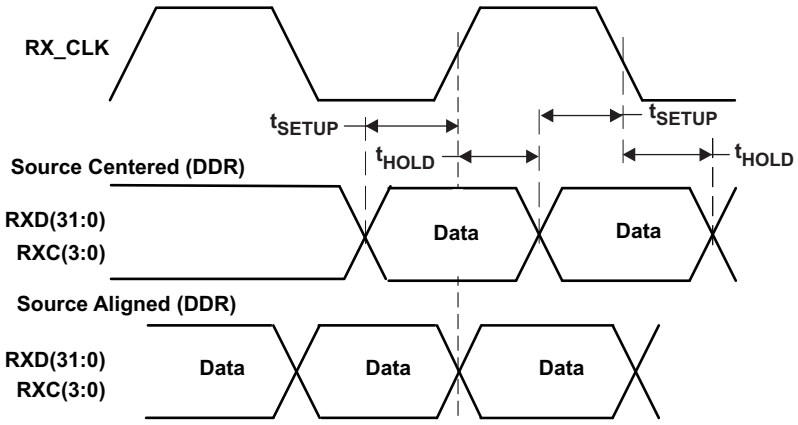


Figure 12. Receive Interface Timing – Source Centered/Aligned

On the transmit data path, the data is sampled on the rising edge and falling edge of TCLK as shown in Figure 13.

DETAILED DESCRIPTION (continued)

In the receive datapath A FIFO, placed on the output of the serial to parallel conversion logic for each serial link, compensates for channel skew, clock phase and frequency tolerance differences between the recovered clocks for each serial links and the receive output clock, RX_CLK. This FIFO has a total depth of sixteen ten bit entries, giving 30 bit time deskew (channel to channel skew) alignment capability in standard mode. See HSTL Output Switching Characteristics (DDR) table in the Electrical Characteristics section for more details on XGMII timing.

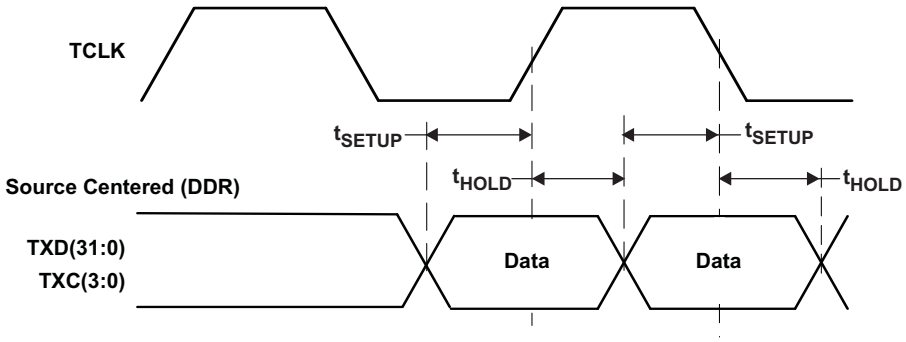


Figure 13. Transmit Interface Timing

PARALLEL INTERFACE DATA

Data placed on the XGMII transmit input bus is latched and then phase aligned to the internal version of the transmit reference clock, 8b/10b encoded, serialized, then transmitted sequentially beginning with the LSB of the encoded data byte over the differential high speed serial transmit pins.

The XGMII receive data bus outputs four bytes on RXD(31:0). Control character (K-characters) reporting for each byte is done by asserting the corresponding control pin, RXC(3:0). When RXC is asserted, the 8 bits of data corresponding to the control pin is to be interpreted as a K-character. If an error is uncovered in decoding the data, the control pin is asserted and 0xFE is output for the corresponding byte.

TRANSMISSION LATENCY

For each channel, the data transmission latency of the TLK3138 is defined as the delay from the rising or falling edge of the selected transmit clock when valid data is on the transmit data pins to the serial transmission of bit 0, as shown in Figure 14. The maximum transmit latency ($T_{LATENCY}$) is 650 bit times; the standard allows a combined latency (TX + RX) of 2048 bit times.

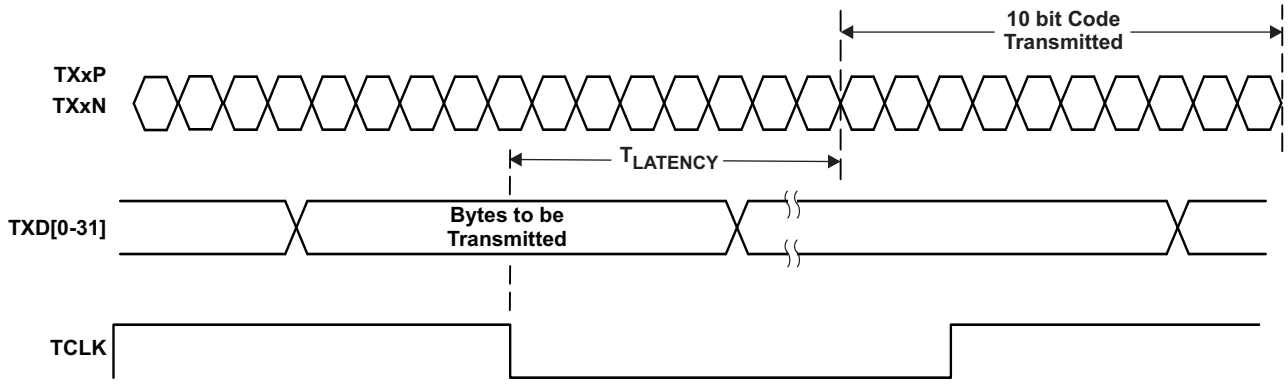


Figure 14. Transmission Latency

DETAILED DESCRIPTION (continued)

CHANNEL CLOCK TO SERIAL TRANSMIT CLOCK SYNCHRONIZATION

In XAUI mode, the TLK3138 allows ±200 ppm difference between the serdes transmit reference on the XAUI side, versus the input TCLK on the XGMII side. There exists a FIFO capable of CTC operations, and has a depth of 32 locations (32 bits wide per location).

The reference clock and the transmit data clock(s) may be from a common source, but the design allows for up to ±200 ppm of frequency difference should the application require it.

DATA RECEPTION LATENCY

For each serial link, the serial-to-parallel data latency is the time from when the first bit arrives at the serial receiver input until it is output in the aligned parallel word on the XGMII, as shown in Figure 15. The maximum receive latency ($R_{LATENCY}$) is 950 bit times using standard alignment mode; the standard allows a combined latency (TX + RX) of 2048 bit times.

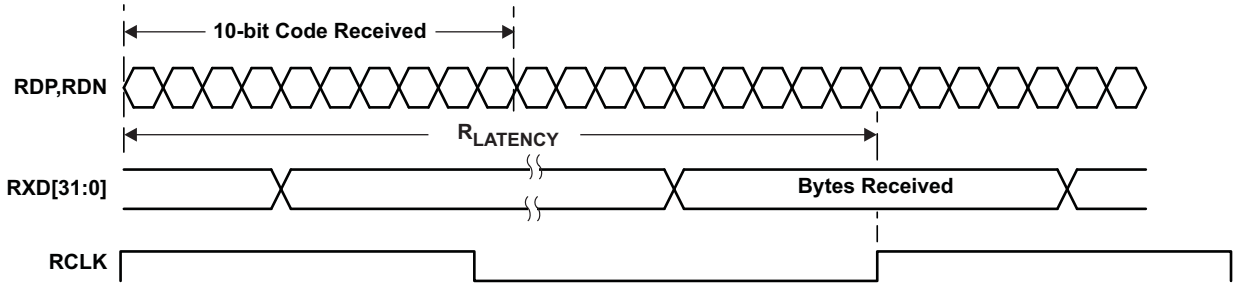


Figure 15. Receiver Latency

8B/10B ENCODER

All true serial interfaces require a method of encoding to insure sufficient transition density for the receiving PLL to acquire and maintain lock. The encoding scheme also maintains the signal DC balance by keeping the number of ones and zeros are balanced which allows for AC coupled data transmission. The TLK3138 uses the 8B/10B encoding algorithm that is used by 10Gbps and 1Gbps Ethernet and Fibre Channel standards. This provides good transition density for clock recovery and improves error checking. The 8B/10B encoder/decoder function is enabled for all serial links. The TLK3138 internally encodes and decodes the data such that the user reads and writes actual 8-bit data on each channel. The encoder and decoder functions can optionally be enabled or disabled on a per channel basis.

The 8B/10B encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transition density. This transmission code includes D Characters, used for transmitting data, and K Characters, used for transmitting protocol information. Each K or D character code word can also have both a positive and a negative disparity version. The disparity of a code word is selected by the encoder to balance the running disparity of the serialized data stream.

The generation of K-characters to be transmitted on each channel is controlled by transmit control pins, TXC(3:0). When the control pin is asserted along with the 8 bits of data, an 8B/10B K-character is transmitted. Similarly, reception of K-characters is reported by the receive control pins, RXC(3:0). When receive control pin is asserted, the corresponding byte on the receive data bus should be interpreted as a K-character. The TLK3138 transmits and receives all of the twelve valid K-characters as defined in Table 1.

DETAILED DESCRIPTION (continued)

Table 1. Valid K-Codes

K-CODE	TXC(3:0) or RXC(3:0)	DATA BUS BYTES (RXD[x: x-7] or TXD[x: x-7])	ENCODED K-CODE		K-code Description
			NEGATIVE RUNNING DISPARITY	POSITIVE RUNNING DISPARITY	
00 through FF	0	DDD DDDDD	dddddd dddd	dddddd dddd	Normal data
K28.0	1	000 11100	001111 0100	110000 1011	IdleO/busy
K28.1	1	001 11100	001111 1001	110000 0110	IdleE/busy
K28.2	1	010 11100	001111 0101	110000 1010	
K28.3	1	011 11100	001111 0011	110000 1100	Channel Alignment Pre-curser
K28.4	1	100 11100	001111 0010	110000 1101	
K28.5	1	101 11100	001111 1010	110000 0101	IdleE/not-busy
K28.6	1	110 11100	001111 0110	110000 1001	
K28.7	1	111 11100	001111 1000	110000 0111	Code Violation or Parity Error
K23.7	1	111 10111	111010 1000	000101 0111	IdleO/not-busy
K27.7	1	111 11011	110110 1000	001001 0111	SOP(S)
K29.7	1	111 11101	101110 1000	010001 0111	EOP(T)
K30.7	1	111 11110	011110 100	100001 0111	

Table 2 provides additional transmit data control coding and descriptions that have been incorporated into 10 Gigabits per second Ethernet. Data patterns put on XGMII transmit data bus other than those defined in Table 2 when the transmit control pin is asserted results in an invalid K-character being transmitted which results in an code error at the receiver.

Table 2. Valid XGMII Channel Encodings

DATA BUS (TXD[x: x-7] or RXD[x: x-7])	TXC(3:0) or RXC(3:0)	DESCRIPTION
00 through FF	0	Normal Data Transmission
00 through 06	1	Reserved
07	1	Idle
08 through 9B	1	Reserved
9C	1	Sequence (only valid in Channel A)
9D through FA	1	Reserved
FB	1	Start (only valid in Channel A)
FC	1	Reserved
FD	1	Terminate
FE	1	Transmit error propagation
FF	1	Reserved

COMMA DETECT AND 8B/10B DECODING

When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to be able to recognize the byte boundary again. Generally this is accomplished through the use of a synchronization pattern. This is a unique a pattern of 1s and 0s that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8B/10B encoding contains a character called the comma (b'0011111' or b'1100000') which is used by the comma detect circuit to align the received serial data back to its original byte boundary. The channel synchronization block detects the K28.5 comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It then converts the data back into 8-bit data. It is important to note that the comma can be either a (b'0011111') or the inverse (b'1100000') depending on the running disparity. The TLK3138 decoder detects both patterns.

The reception of K-characters is reported by the assertion of receive control pin, RXC(3:0) for the corresponding byte on the XGMII receive bus. When a code word error or running disparity error is detected in the decoded data received on a serial link, the receive control pin is asserted and an 0xFE is placed on the receive data bus for that channel, as shown in Table 3.

Table 3. Receive Data Controls

EVENT	RECEIVE DATA BUS RXD[x: 7-x]	RXC(3:0)
Normal Data	XX	0
Normal K-character	Valid K-code	1
Code word error or running disparity error	FE	1

Channel Initialization and Synchronization

The TLK3138 has a synchronization state machine which is responsible for handling link initialization and synchronization for each channel. The initialization and synchronization state diagram is provided in Figure 16. The status of any channel can be monitored by reading MDIO register 4/5.24.3:0.

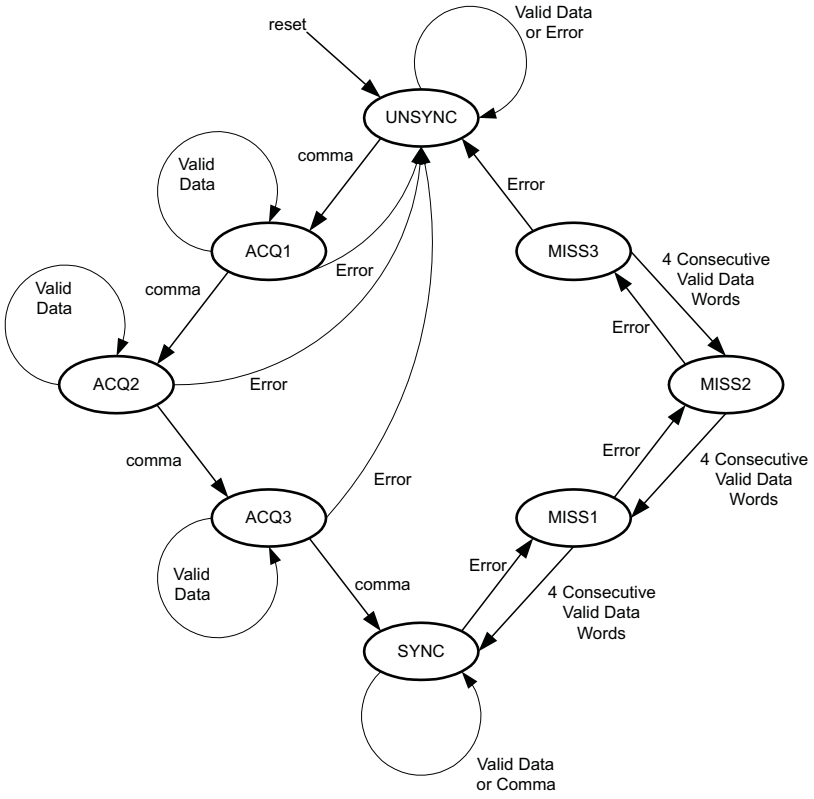


Figure 16. Channel Synchronization State Machine

CHANNEL STATE DESCRIPTIONS

UNSYNC – This is the initial state for each channel upon device power up or reset. In this state, the TLK3138 has the comma detect circuit active and makes code word alignment adjustments based on the position of a comma in the incoming data stream. While in this state the TLK3138 sets the Lane Sync bit to '0' for the particular channel in MDIO register bits 4/5.24.3:0, indicating the lane is not synchronized.(1) The channel state transitions to the ACQ1 state upon the detection of a comma.

(1) The Lane Sync Bit = '0' bit from any/or all channels causes a local fault to be output on the receive data bus.

ACQ1 – During this state the comma detect circuit is active but code word re-alignment is disabled. The TLK3138 remains in this state until either a comma is detected in the same code word alignment position as found in state UNSYNC or a decode error is encountered. While in this state, the Lane Sync bit for the particular channel remains de-asserted, indicating the lane is not synchronized.(2) A decode or running disparity error returns the channel state to UNSYNC. A detected comma causes the channel state to transition to ACQ2.

ACQ2 – During this state, the comma detect circuit is active but code word re-alignment is disabled. The TLK3138 remains in this state until either a comma is detected in the same code word alignment position as found in state UNSYNC or a decode error is encountered. While in this state, the Lane Sync bit for the particular channel remains de-asserted, indicating the lane is not synchronized.(2) A decode or running disparity error returns the channel state to UNSYNC. A detected comma causes the channel state to transition to ACQ3.

ACQ3 –During this state the comma detect circuit is active but code word re-alignment is disabled. The TLK3138 remains in this state until either a comma is detected or a decode error encountered. While in this state, the Lane Sync bit for the particular channel remains de-asserted, indicating the lane is not synchronized.(2) A decode or running disparity error returns the channel state to UNSYNC. A detected comma causes the channel state to transition to SYNC.

SYNC –This is the normal state for receiving data. When in this state, the TLK3138 sets the Lane Sync bit to '1' for the particular channel in the MDIO register bits 4/5.24.3:0 indicating the lane has been synchronized. During this state the comma detect circuit is active but code word re-alignment is disabled. A decode or running disparity error causes the channel state to transition to MISS1.

MISS1 – When entering this state an internal error counter is cleared. If the next four consecutive codes are decoded without error, the channel state reverts back to SYNC. If a decode or running disparity error is detected, the channel state transitions to MISS2.

MISS2 – When entering this state an internal error counter is cleared. If the next four consecutive codes are decoded without error, the channel state reverts back to MISS1. If a decode or running disparity error is detected, the channel state transitions to MISS3.

MISS3 –When entering this state an internal error counter is cleared. If the next four consecutive codes are decoded without error, the channel state reverts back to MISS1. If a decode or running disparity error is detected, the channel state transitions to UNSYNC.

END OF PACKET ERROR DETECTION

Because of their unique data patterns, /A/ (K28.3), /K/ (K28.5), and /T/ (K29.7) catch running disparity errors that may have propagated undetected from previous codes in a packet. Running disparity errors detected by these control codes at the end of packets cause the previous data codes to be reported as errors (0xFE) to allow the protocol device to reject the packet (see Figure 17).

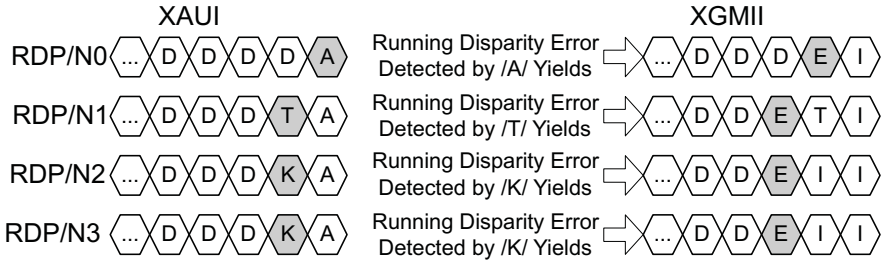


Figure 17. End of Packet Error Detection

(2) The Lane Sync bit = '0' causes a local fault to be output on the receive data bus.

FAULT DETECTION AND REPORTING

The TLK3138 detects and reports local faults as well as forward both local and remote faults as defined in the IEEE P802.3ae 10Gbps Ethernet Standard to aid in fault diagnosis. All faults detected by the TLK3138 are reported as local faults to the upper layer protocols. Once a local fault is detected in the TLK3138, MDIO register bit 4/5.1.7 is set. Fault sequences, sequence ordered sets received by the TLK3138, either on the Transmit Data Bus or on the high speed receiver pins, are forwarded without change to the MDIO registers in the TLK3138. Also, note that the TLK3138 is capable of performing CTC operation where only RF and LF or any Q sequences are transported (not generated) in either the transmit or receive direction in XAUI mode.

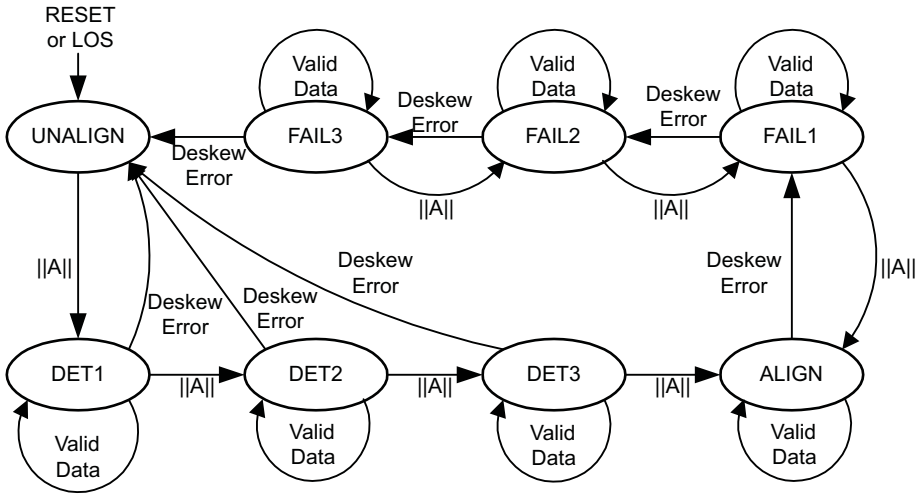
TLK3138 reports a fault by outputting a K28.4 (0x9C) on RXD(7:0), 0x00 on RXD(15:8) and RXD(23:8) and 0x01 for local faults on RXD(31:24). Forwarding of remote faults is handled as a normal transmission. Note that the TLK3138 does not generate a remote fault indication nor any other type of Q.

RECEIVE SYNCHRONIZATION AND SKEW COMPENSATION

In XAUI mode, the TLK3138 has a FIFO enabled on the receive data path coming from each serial link to compensate for channel skew and clock phase and frequency tolerance differences between the recovered clocks for each channel and the receive output clock RX_CLK. This FIFO has a depth of 32 locations (32 bits wide for each location).

The de-skew of the 4 serial links that make up each XAUI channel into a single 32 bit wide column of data is accomplished by alignment of the receive FIFOs on each serial link to a K28.3 control code sent during the inter-packet gap (IPG) between data packets or during initial link synchronization. The K28.3 code (referred to as the *A* or alignment code) is transmitted on the first column following the end of the data packet as shown in Table 2.

The column de-skew state machine is provided in Figure 18. The status of column alignment can be monitored by reading MDIO registers 4/5.24.12 for global alignment.



Note: Deskew Error is at least one column containing an A character, but not all four simultaneously.

Figure 18. Column De-Skew State Machine

COLUMN STATE DESCRIPTIONS

UNALIGN – This is the initial state for the column state machine upon device power up or reset. If any of the channel state machines are set to UNSYNC, the column state is set to UNALIGN. In this state, the column state machine searches for alignment character codes (K28.3 or /A/) on each channel and align the FIFO pointers on each channel to the /A/ character code. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4/5.24.12, indicating the column is not aligned.(3) The column state transitions to the DET1 state upon the detection and alignment of /A/ character codes in all four channels.

DET1 – During this state, the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. The column state machine remains in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels) or a deskew error is detected, the column state machine transitions to state UNALIGN. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4/5.24.12 indicating the column is not aligned.(4) Detection of a complete alignment column causes the column state machine to transition to state DET2.

DET2 – During this state, the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. The column state machine remains in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels) or a deskew error is detected, the column state machine transitions to state UNALIGN. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4/5.24.12 indicating the column is not aligned.(4) Detection of a complete alignment column causes the column state machine to transition to state DET3.

DET3 –During this state, the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. The column state machine remains in this state looking for a column of alignment character codes. If an incomplete alignment column is detected (alignment character codes not found on all channels) or a deskew error is detected, the column state machine transitions to state UNALIGN. While in this state, the Column Alignment Sync bit is set to '0' in MDIO registers 4/5.24.12 indicating the column is not aligned.(4) Detection of a complete alignment column causes the column state machine to transition to state ALIGN.

ALIGN – This is the normal state for receiving data. When in this state, the column state machine sets the Column Alignment Sync bit to '1' in MDIO registers 4/5.24.12 indicating all channels are aligned. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If a deskew error is detected in the correct position within the Inter-Packet Gap, the column state machine transitions to state FAIL1.

FAIL1 – When in this state, the Column Alignment Sync bit is '1' in MDIO registers 4/5.24.12. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If a complete alignment column is not detected in the correct position within the Inter-Packet Gap, the column state machine transitions to state FAIL2.

FAIL2 – When in this state, the Column Alignment Sync bit is '1' in MDIO registers 4/5.24.12. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If a complete alignment column is not detected in the correct position within the Inter-Packet Gap, the column state machine transitions to state FAIL3.

FAIL3 – When in this state, the Column Alignment Sync bit is '1' in MDIO registers 4/5.24.12. During this state the alignment character code detect circuit is active on each channel but the column re-alignment is disabled. If complete alignment column is not detected in the correct position within the Inter-Packet Gap, the column state machine transitions to state UNALIGN.

(3) The XGXS Lane Alignment bit = '0' causes a local fault to be output on the receive data bus.
(4) The XGXS Lane Alignment bit = '0' causes a local fault to be output on the receive data bus.

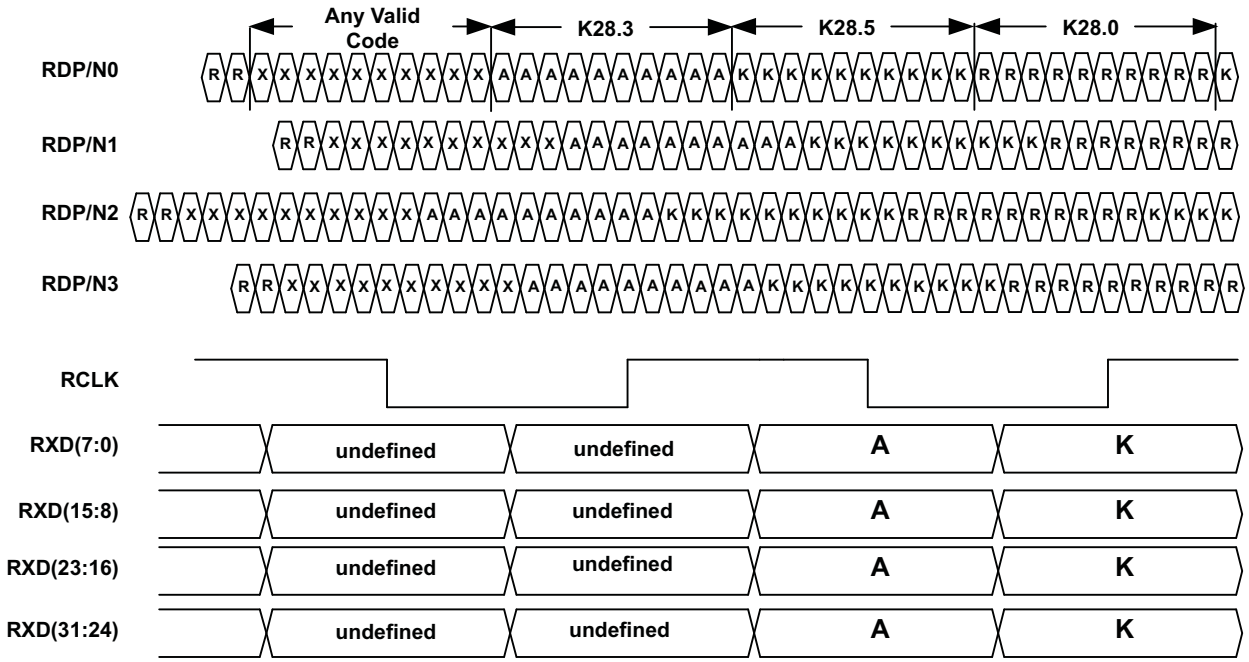


Figure 19. Channel De-Skew Using Alignment Code

INTER-PACKET GAP MANAGEMENT

When in transceiver mode, the TLK3138 replaces the idle codes (see Table 2) during the Inter-Packet Gap (IPG) with the necessary codes to perform all channel alignment, byte alignment, and clock tolerance compensation as defined in IEEE 802.3ae 10Gbps Ethernet Standard. According to the Ethernet Standard, a valid packet must begin on TXD(0:7) of the XGMII. However, due to variable packet sizes, the IPG can begin on any channel. The TLK3138 replaces idle codes latched on the same XGMII clock edge as the end of packet code with /K/ codes (as shown in Figure 20).

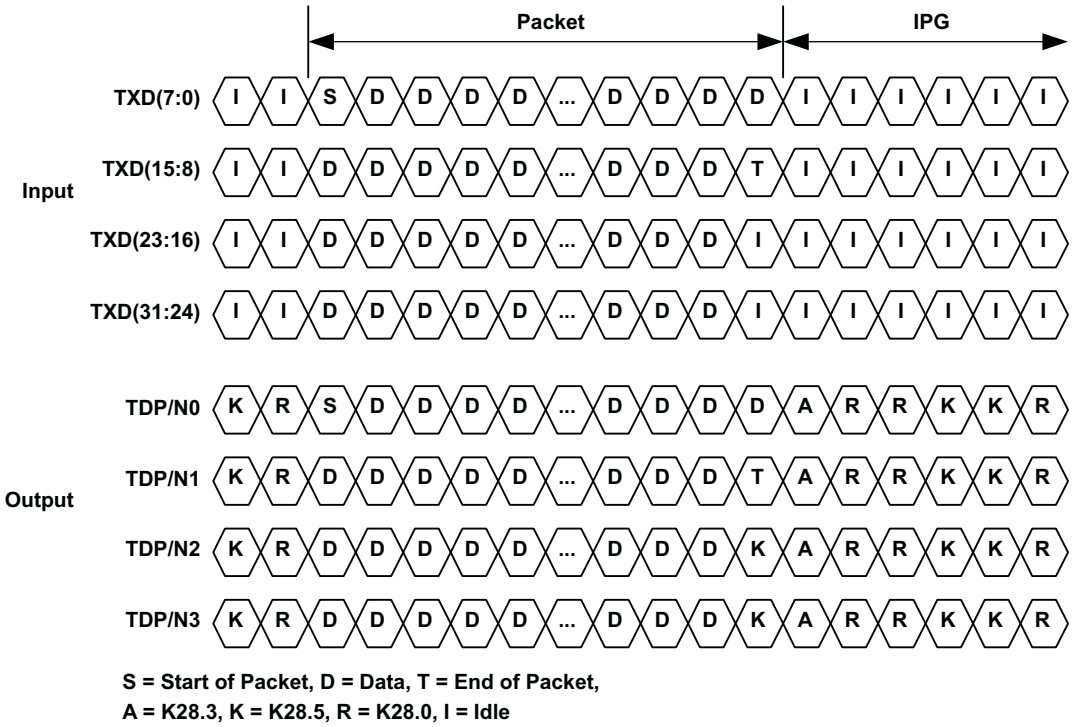


Figure 20. Inter-Packet Gap Management

The subsequent idles in the IPG are replaced by *columns* of channel alignment codes (K28.3), byte alignment codes (K28.5), or clock tolerance compensation codes (K28.0). The state machine which governs the IPG replacement procedure is illustrated in Figure 21, with notation defined in Table 2. Note that any IPG management state transitions to send data if the IPG is terminated.

The repetition of the */A/* pattern on each serial channel allows the FIFOs to remove or add the required phase and frequency difference to align the data from all four serial links of a XAUI channel and allow output of the aligned 32 bit wide data on a single edge of the receive clock, RX_CLK, as shown in Figure 21.

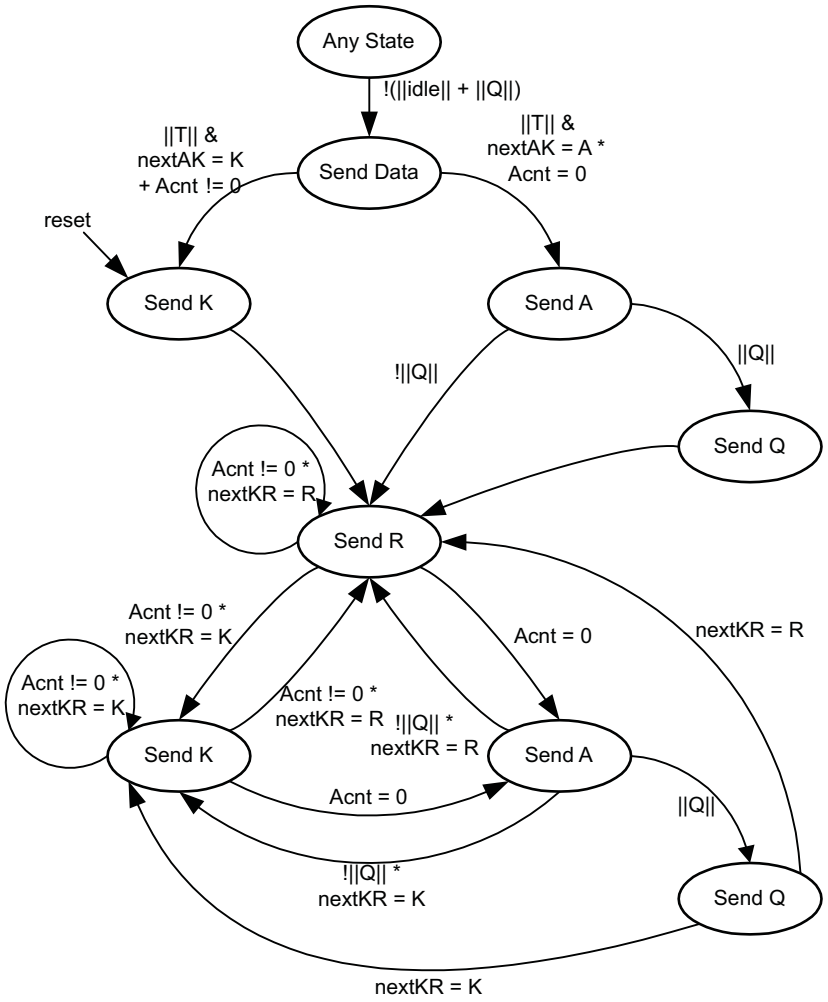


Figure 21. IPG Management State Machine

Table 4. IPG Management State Machine Notation

SYMBOL	DEFINITION
||idle||	XGMII idle. 0x07 on TXD(x:: :x-7),
||Q||	Link status message: K28.4, Dx.y, Dx.y, Dx.y.
nextAK	A Boolean variable. It takes the value K when an A is sent at the beginning of the IPG and the value A when a K is sent at the beginning of the IPG. Its initial value is K.
Acnt	When an A character is sent, variable Acnt is loaded with a random number such that 16 ≤ Acnt ≤ 31. Acnt is decremented each time a column of A characters is generated.
nextKR	A randomly-generated Boolean that can assume the value K or R.
||T||	Terminate Character Column (Terminate Character in Any Lane)

CLOCK TOLERANCE COMPENSATION (CTC)

The XAUI interface is defined to allow for separate clock domains on each side of the link. Though the reference clocks for two devices on a XAUI link have the same specified frequencies, there are slight differences that, if not compensated for, leads to over or under run of the FIFOs on the receive/transmit data path. The TLK3138 provides compensation for these differences in clock frequencies via the insertion or the removal of /R/ characters on all channels, as shown in Figure 22 and Figure 23.

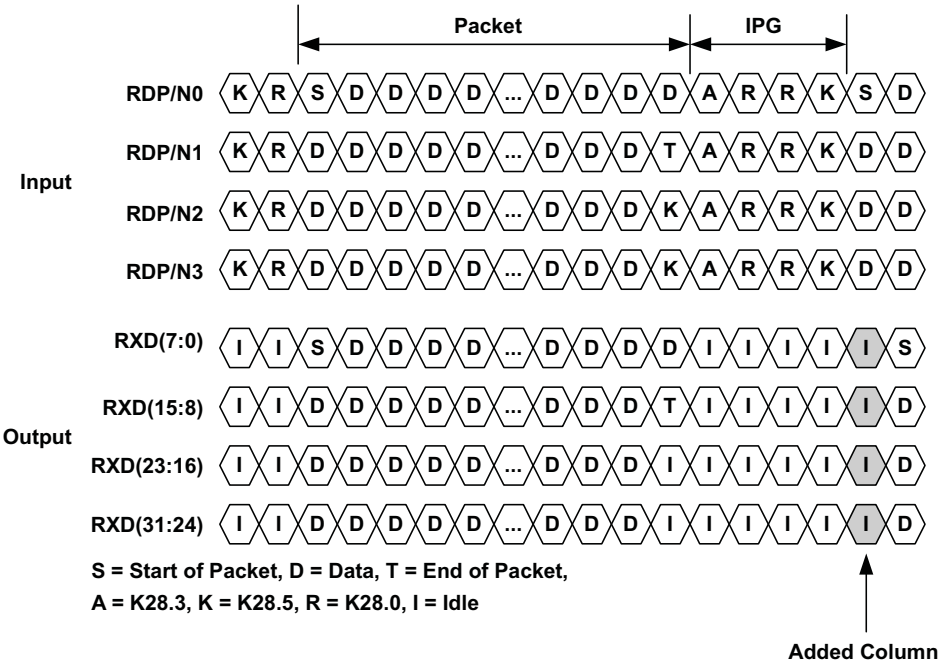


Figure 22. Clock Tolerance Compensation: Add

The /R/ code is disparity neutral, allowing its removal or insertion without affecting the current running disparity of each channel's serial stream.

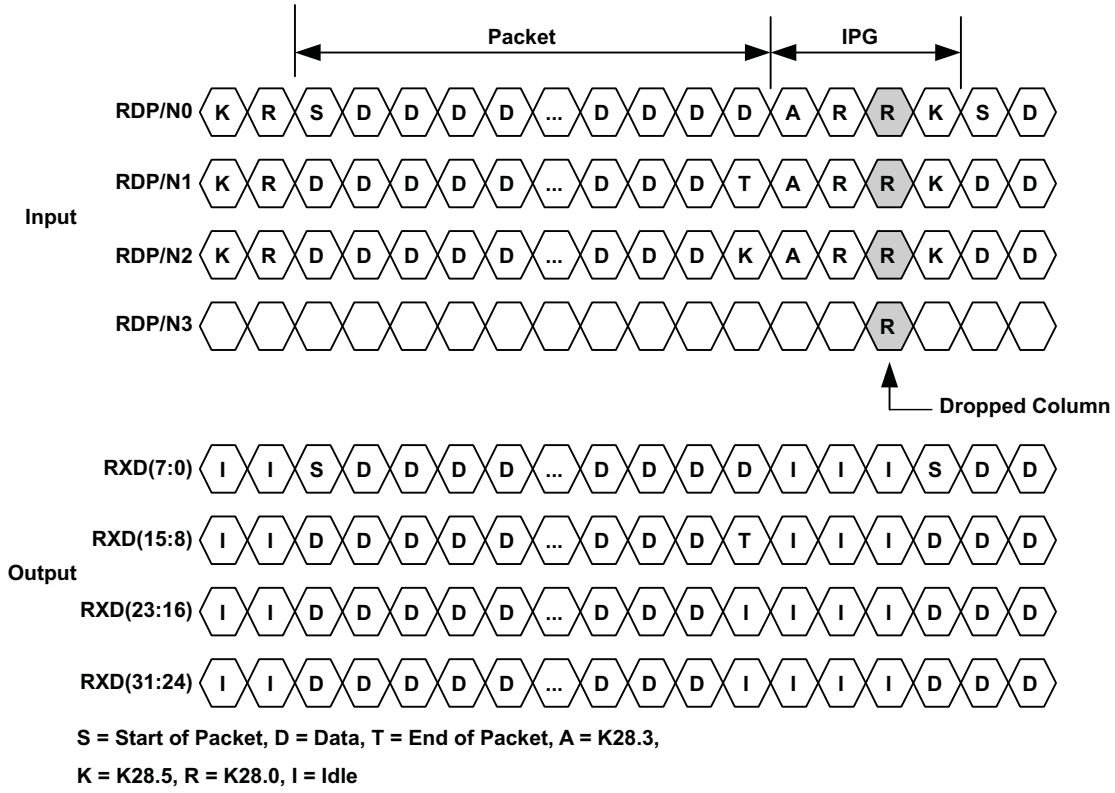


Figure 23. Clock Tolerance Compensation: Drop

PARALLEL TO SERIAL

The parallel-to-serial shift register on each channel takes in data and converts it to a serial stream. The shift register is clocked by the internally generated bit clock, which is 10 times the reference clock (REFCLKP/REFCLKN) frequency. The least significant bit (LSB) for each channel is transmitted first.

SERIAL TO PARALLEL

For each channel, serial data is received on the RDPx/RDNx pins. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within ±200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. If enabled, the 10-bit wide parallel data is then fed into 8b/10b decoders.

HIGH SPEED CML OUTPUT

The high speed data output driver is implemented using Current Mode Logic (CML) with integrated pull up resistors requires no external components. The line can be directly coupled or AC coupled. Under many circumstances, AC couple is desirable.

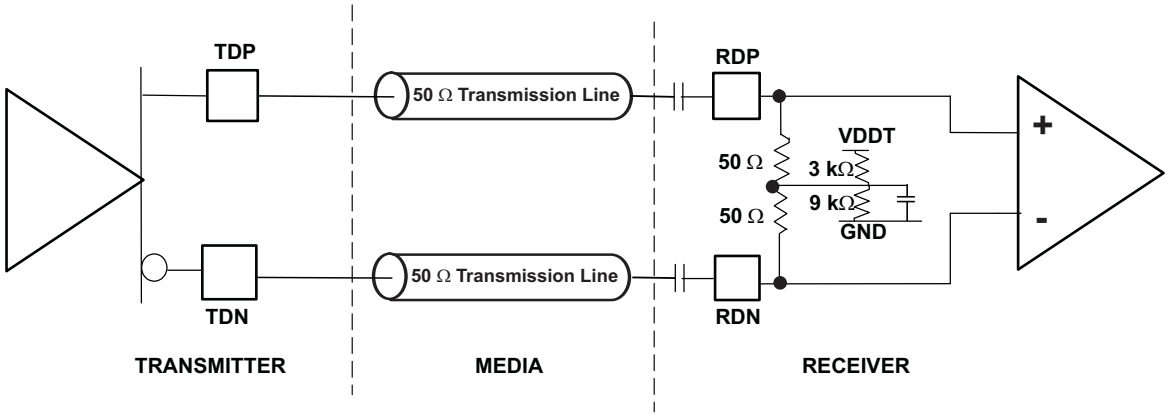


Figure 24. Example High Speed I/O AC Coupled Mode

Standard Current Mode Logic (CML) drivers usually require external components. The disadvantage of the external edge control is a limited edge rate due to package and line parasitic. The CML driver on TLK3138 has on-chip 50Ω termination resistors terminated to VDDT therefore provides optimum performance for increased speed requirements. The transmitter output driver is highly configurable allowing slew rate, output amplitude and pre-emphasis to be turned to a channel's individual requirements. An internal voltage reference derived from VDDT is also available to provide the target for output amplitude control loop. This reference is enabled by holding register bit 4/5.32900.6 low and results in a nominal output amplitude of ~1400mV differential pk-pk for 100% swing. The receiver input is internally biased to 2×VDDT/3 which is the optimum voltage for input sensitivity. As the input and output references are derived from VDDT, the tolerance of this supply dominates the accuracy of the internal reference. Applications requiring higher tolerance output amplitude are advised to provide a high accuracy external reference.

When transmitting data across long lengths of PCB trace or cable, the high frequency content of the signal is attenuated due to the skin effect of the media. This causes a *smearing* of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, 2-tap finite impulse response (FIR) transmit pre-emphasis is implemented. In a 1-tap FIR pre-emphasis, differential swing is increased or *pre-emphasized* for the bit immediately following a transition and subsequently reduced or *de-emphasized* for run lengths greater than one, as shown in Figure 25. This provides additional high frequency energy to compensate for PCB or cable loss.

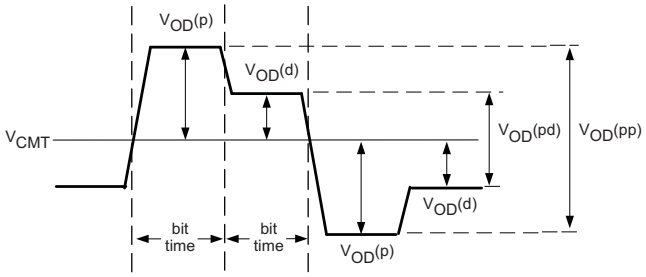


Figure 25.

The 2-stage mode operates in a similar manner but considers the logic level of the previous two transmitted bits when determined how much pre-emphasis to apply. The level and mode of the pre-emphasis is programmable via MDIO Register bits 4/5.32900.14:11. Users can control the strength of the pre-emphasis to optimize for a specific system requirement.

HIGH SPEED RECEIVER

The high speed receiver conforms to the physical layer requirements of IEEE 802.3ae Clause 47(XAUI). The termination impedances of the receiver is configured as 100 Ohms with the center tap weakly tied to 2×VDDT/3 with a capacitor to create an AC ground. AC coupling is always required on receiver inputs.

All receive channels incorporate an adaptive equalizer. This circuit compensates for channel insertion loss by amplifying the high frequency components of the signal, reducing inter-symbol interference. Setting 4/5.32900.2 enables adaptive equalization. In this mode, both the gain and bandwidth of the equalizer with be controlled by the receiver equalization logic. Bandwidth selection is based on the setting applied to 4/5.32901.14:13 and 4/5.32900.3. Equalization can be disabled by setting 4/5.32900.2 low.

LOOPBACK

In XAUI Mode, two internal loopback modes are possible for each XAUI Channel Group A and B. One, called XGMII loopback, allows the data input on the XGMII interface to be returned out the corresponding XGMII interface (A->A, B->B). The other, called XAUI loopback, allows serial data on the XAUI interface to be returned out the corresponding XAUI interface (A->A, B->B).

An external loopback (requiring external connection) is also supported, which can be used with the PRBS patterns, as well as the CJPAT, CRPAT, Mixed/High/Low Frequency tests.

LINK TEST FUNCTIONS

The TLK3138 has an extensive suite of built in test functions to support system diagnostic requirements. Each channel has built-in link test generator and verification logic. Several patterns can be selected via the MDIO that offer extensive test coverage. The patterns are: 2^7-1 or 2^{23}-1 PRBS (Pseudo Random Bit Stream), CJPAT, CRPAT, high and low and mixed frequency patterns.

MDIO Management Interface

The TLK3138 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 45 of the IEEE 802.3ae Ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK3138 is possible without use of this interface. However, some additional features are accessible only through the MDIO.

The following registers in the PROGRAMMERS REFERENCE are implemented as global registers (i.e Same physical register is accessed through XAUI-A register access or XAUI-B register access):

16'h8086, 16'h8088, 16'h8089, 16'h808B, 16'h808C, 16'h808E, 16'h8090, 16'h8091, 16'h8092, 16'h8093,16'h80A0, 16'h80A1, 16'h80A2

All other registers are implemented per XAUI channel (unique per channel).

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The device id and port address are determined by bootstrap pins (see Table 82). In Clause 45, the 5 bootstrap pins determine the port address. Of the port address bits, only the upper four bits are looked at. If the bottom bit of the incoming serial port address is a zero, then XGXS A is addressed. If the bottom bit of the incoming serial port address is a one, then XGXS B is addressed. The device ID is required to be either 4 or 5, so only the bottom device id bit is required. If device id bit 0 is a 0, then a PHY device is selected for both XGXS A and B. If device id bit 0 is a 1, then a DTE device is selected for both XGXS A and B. Note, each register is accessed as either DTE or PHY devices in the TLK3138, although physically there is only one register accessed two different ways. Also note, the XAUI interfaces must either be both DTE devices or both be PHY devices. An even PHY Address (as defined below) indicates an access to XAUI A register space, and an odd PHY Address indicates access to XAUI B register space.

Write transactions which address an invalid register or device, or a read only register are ignored. Read transactions which address an invalid register or device return a 0.

Timing for a Clause 45 address transaction is shown in Figure 26. The Clause 45 timing required to write to the internal registers is shown in Figure 27. The Clause 45 timing required to read from the internal registers is shown in Figure 28. The Clause 45 timing required to read from the internal registers and then increment the active address for the next transaction is shown in Figure 29.

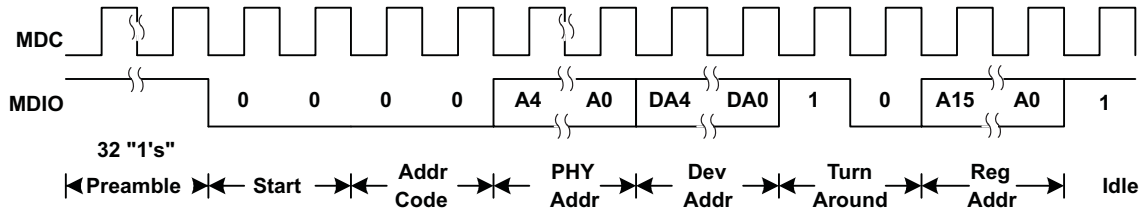


Figure 26. CL45 - Management Interface Extended Space Address Timing

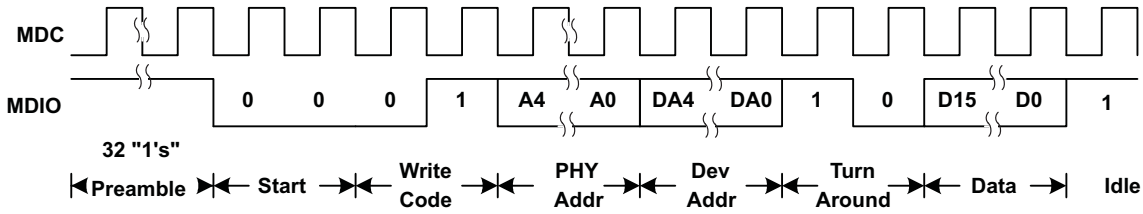


Figure 27. CL45 - Management Interface Extended Space Write Timing

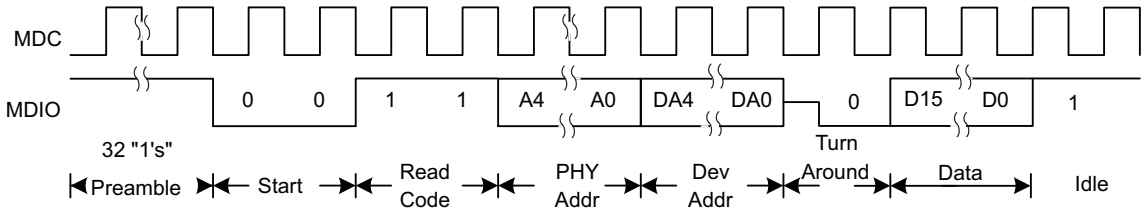


Figure 28. CL45 - Management Interface Extended Space Read Timing

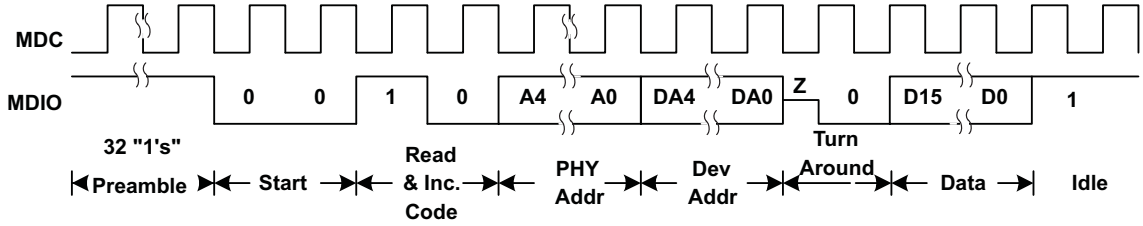


Figure 29. CL45 - Management Interface Extended Space Read And Increment Timing

The IEEE 802.3ae Clause 45 specification defines many of the registers, and additional registers have been implemented for expanded functionality.

PROGRAMMERS REFERENCE

Table 5. XS(1)_CONTROL_1

Address: 0x0000		Default: 0x2040	
Bit(s)	**Name**	**Description**	**Access(2)**
4/5.0.15	Reset	1 = XS reset (including all registers) 0 = Normal operation	RW SC

4/5.0.14	Loop back	1 = Enable loop back mode.
		If the device is configured as PHY XS (DVAD(0) = 0), then
		XAUI_LOOPBACK is performed (RX parallel to TX parallel)
		If the device is configured as DTE XS (DVAD(0) = 1), then
		XGMII_LOOPBACK is performed (TX serial to RX serial)
		0 = Disable loop back mode
			RW

4/5.0.13	Speed Selection	This bit always reads 1 indicating operation at 10 Gb/s and above.	
4/5.0.11	Low power	1 = Low power mode 0 = Normal operation	
4/5.0.6	Speed Selection	This bit always reads 1 indicating operation at 10Gbps and above.	
4/5.0.5:2	Speed Selection	These bits always read 0 indicating operation at 10Gbps.	

(1) In this section XS refers to either PHY or DTE XS device.
(2) RO: Read-Only, RW: Read-Write, SC: Self-Clearing, LL: Latching-Low, LH: Latching-High, COR: Clear-on-Read

Table 6. XS_STATUS_1

Address: 0x0001		Default: 0x0082	
Bit(s)	**Name**	**Description**	**Access**
4/5.1.7	Fault	1 = Fault condition detected (either on TX or RX side. This bit is OR ed version of 4/5.8.10 and 4/5.8.11) 0 = No fault condition detected	RO
4/5.1.2	XS Transmit Link Status	1 = XS Transmit link is up. 0 = XS Transmit links is down. (This bit is latched low version of 4/5.24.12)	RO/LL
4/5.1.1	Low Power Ability	This bit always reads 1 indicating support for low power mode	RO

Table 7. XS_DEVICE_IDENTIFIER_1

Address: 0x0002		Default: 0x4000	
Bit(s)	**Name**	**Description**	**Access**
4/5.2.15.0	OUI c:r	Organizationally unique identifier.	RO

Table 8. XS_DEVICE_IDENTIFIER_2

Address: 0x0003		Default: 0x50D0	
Bit(s)	**Name**	**Description**	**Access**
4/5.3.15:0	OUI c:r	Device identifier. Manufacturer model and revision number	RO

Table 9. XS_SPEED_ABILITY

Address: 0x0004		Default: 0x0001	
Bit(s)	**Name**	**Description**	**Access**
4/5.4.0	10G Capable	This bit always reads 1 indicating operation at 10Gb/s	RO

Table 10. XS_DEVICES_IN_PACKAGE_1

Address: 0x0005		Default: 0x0010	
Bit(s)	**Name**	**Description**	**Access**
4/5.5.5	DTE XS Present	1 = DTE XS present in the package. 0 = DTE XS not present in the package. Read returns 1, when dvad_in is high	RO
4/5.5.4	PHY XS Present	1 = PHY XS present in the package. 0 = PHY XS not present in the package. Read returns 1, when dvad_in is low	
4/5.5.3	PCS Present	Always reads 0	
4/5.5.2	WIS Present	Always reads 0	
4/5.5.1	PMD/PMA Present	Always reads 0	
4/5.5.0	Clause 22 registers Present	Always reads 0	

Table 11. XS_DEVICES_IN_PACKAGE_2

Address: 0x0006		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.6.15	Vendor Specific Device 2 Present	This bit always reads 0 indicating that vendor specific device 2 not present in package.	RO
4/5.6.14	Vendor Specific Device 1 Present	This bit always reads 0 indicating that vendor specific device 1 not present in package .	

Table 12. XS_STATUS_2

Address: 0x0008		Default: 0x8C00	
Bit(s)	**Name**	**Description**	**Access**
4/5.8.15:14	Device present	Always read 10 indicating that device responds at this address	RO
4/5.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
4/5.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	

Table 13. XS_PACKAGE_IDENTIFIER_1

Address: 0x000E		Default: 0x4000	
Bit(s)	**Name**	**Description**	**Access**
4/5.14.15:0	OUI c:r	Organizationally unique identifier.	RO

Table 14. XS_PACKAGE_IDENTIFIER_2

Address: 0x000F		Default: 0x50D0	
Bit(s)	**Name**	**Description**	**Access**
4/5.15.15:0	OUI c:r	Organizationally unique identifier Manufacturer model and revision number.	RO

Table 15. XS_LANE_STATUS

Address: 0x0018		Default: 0x0C00	
Bit(s)	**Name**	**Description**	**Access**
4/5.24.12	Align status	When 1, indicates all lanes are aligned	RO
4/5.24.11	Pattern testing ability	Always reads 1. Able to generate test patterns	
4/5.24.10	Loopback ability	Always read 1. Has the ability to perform loopback function	
4/5.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	
4/5.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	
4/5.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	
4/5.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	

Table 16. XS_TEST_CONTROL

Address: 0x0019		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.25.2	Receive test-pattern enable	When 1, indicates test pattern function is enabled.	RW
4/5.25.1:0	Test-pattern select	00 = High frequency test pattern 01 = Low frequency test pattern 10 = Mixed frequency test pattern 11 = Reserved	

Table 17. TEST_CONFIG

Address: 0x8000		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32768.1	CRPAT enable	When set, enables the CRPAT test pattern on all 4 lanes.	RW
4/5.32768.0	CJPAT enable	When set, enables the CJPAT test pattern on all 4 lanes.	

Table 18. TEST_VERIFICATION_CONTROL

Address: 0x8001		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32769.1	CRPAT check enable	When set, enables the verification of CRPAT test modes.	RW
4/5.32769.0	CJPAT check enable	When set, enables the verification of CJPAT test modes.	

Table 19. TX_FIFO_STATUS

Address: 0x8002		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32770.9	Lane 3 overflow	When high, indicates that transmit FIFO overflow condition occurred for the corresponding lane.	RO/LH
4/5.32770.8	Lane 2 overflow		
4/5.32770.7	Lane 1 overflow		
4/5.32770.6	Lane 0 overflow		
4/5.32770.5	Lane 3 underflow	When high, indicates that transmit FIFO underflow condition occurred for the corresponding lane.	RO/LH
4/5.32770.4	Lane 2 underflow		
4/5.32770.3	Lane 1 underflow		
4/5.32770.2	Lane 0 underflow		
4/5.32770.1	Overflow	When high, indicates that transmit FIFO overflow condition occurred in any lane.	
4/5.32770.0	Underflow	When high, indicates that transmit FIFO underflow condition occurred in any lane.	

Table 20. TX_FIFO_DROP_COUNT

Address: 0x8003		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32771.15:0	Drop count	Counter for number of idle drops in the transmit FIFO	RO/COR

Table 21. TX_FIFO_INSERT_COUNT

Address: 0x8004		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32772.15:0	Insert count	Counter for number of idle inserts in the transmit FIFO	RO/COR

Table 22. TX_CODEGEN_STATUS

Address: 0x8005		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32773.6	Invalid XGMII character in lane 3	When high, indicates invalid XGMII character received in the corresponding lane.	RO/LH
4/5.32773.5	Invalid XGMII character in lane 2		
4/5.32773.4	Invalid XGMII character in lane 1		
4/5.32773.3	Invalid XGMII character in lane 0		
4/5.32773.2	Invalid XGMII character error	When high, indicates invalid XGMII character received in any lane	RO/LH
4/5.32773.1	Invalid T column error	When high, indicates invalid Terminate column (column that contains Terminate character not followed by Idle character(s)) received from the XGMII interface.	
4/5.32773.0	Invalid S column error	When high, indicates invalid Start column (column that contains Start character in a lane other than lane 0) received from the XGMII interface.	

Table 23. LANE_0_TEST_ERROR_COUNT

Address: 0x8006		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32774.15:0	Lane 0 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 0. This counter increments by 1 for each received character that has error.	RO/COR

Table 24. LANE_1_ TEST_ERROR_COUNT

Address: 0x8007		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32775.15:0	Lane 1 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 1. This counter increments by 1 for each received character that has error.	RO/COR

Table 25. LANE_2_ TEST_ERROR_COUNT

Address: 0x8008		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32776.15:0	Lane 2 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 2. This counter is incremented by 1 for each received character that has error.	RO/COR

Table 26. LANE_3_ TEST_ERROR_COUNT

Address: 0x8009		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32777.15:0	Lane 3 test pattern error counter	This counter reflects errors for High, Medium or Low Frequency test patterns for lane 3. This counter increments by one for each received character that has error.	RO/COR

Table 27. CRPAT_CJPAT_TEST_ERROR_COUNT_1(1)

Address: 0x800A		Default: 0xFFFF	
Bit(s)	**Name**	**Description**	**Access**
4/5.32778.15:0	CRPAT/CJPAT test error counter	MSB of CRPAT/CJPAT error counter for all 4 lanes	RO

(1) User has to make sure that register 32778 is read first and then register 32779. If user reads register 32779 without reading register 32778 first, then the count value read through 32779 register may not be correct.

Table 28. CRPAT_CJPAT_TEST_ERROR_COUNT_2(1)

Address: 0x800B		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32779.15:0	CRPAT/CJPAT test error counter	LSB of CRPAT/CJPAT error counter for all 4 lanes	RO

(1) User has to make sure that register 32778 is read first and then register 32779. If user reads register 32779 without reading register 32778 first, then the count value read through 32779 register may not be correct.

Table 29. LANE_0_EOP_ERROR_COUNT(1)

Address: 0x800C		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32780.15:0	Lane 0 end of packet error counter	End of packet termination error counter for lane 0. End of packet error for lane 0 is detected on the RX side. It is detected when Terminate character is in lane 0 and one or both of the following holds:	RO/COR
		• Terminate character is not followed by /K/ characters in lanes 1, 2 and 3	
		• The column following the terminate column is neither ||K|| or ||A||.	

(1) Counter is incremented by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter holds on to its value when align_status goes low or when the counter reaches its maximum value. It is cleared when it is read.

Table 30. LANE_1_EOP_ERROR_COUNT(1)

Address: 0x800D		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32781.15:0	Lane 1 end of packet error counter	End of packet termination error counter for lane 1. End of packet error for lane 1 is detected on the RX side. It is detected when Terminate character is in lane 1 and one or both of the following holds:	RO/COR
		• Terminate character is not followed by /K/ characters in lanes 2 and 3	
		• The column following the terminate column is neither ||K|| or ||A||.	

(1) Counter is incremented by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter holds on to its value when align_status goes low or when the counter reaches its maximum value. It is cleared when it is read.

Table 31. LANE_2_EOP_ERROR_COUNT(1)

Address: 0x800E		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32782.15:0	Lane 2 end of packet error counter	End of packet termination error counter for lane 2. End of packet error for lane 2 is detected on the RX side. It is detected when Terminate character is in lane 2 and one or both of the following holds:	RO/COR
		• Terminate character is not followed by /K/ characters in lane 3	
		• The column following the terminate column is neither ||K|| or ||A||.	

(1) Counter is incremented by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter holds on to its value when align_status goes low or when the counter reaches its maximum value. It is cleared when it is read.

Table 32. LANE_3_EOP_ERROR_COUNT(1)

Address: 0x800F		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32783.15:0	Lane 3 end of packet error counter	End of packet termination error counter for lane 3. End of packet error for lane 3 is detected on the RX side. It is detected when Terminate character is in lane 3 and the column following the terminate column is neither ||K|| or ||A||.	RO/COR

(1) Counter is incremented by 1 when EOP error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter holds on to its value when align_status goes low or when the counter reaches its maximum value. It is cleared when it is read.

Table 33. LANE_0_CODE_ERROR_COUNT(1)

Address: 0x8010		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32784.15:0	Lane 0 code error counter	Output 16-bit counter for invalid code group found in lane 0. Invalid code group is detected when the 8B10B decoder cannot decode the received codeword.	RO/COR

(1) Counter is incremented by 1 when codeword error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter holds on to its value when align_status goes low or when the counter reaches its maximum value. It is cleared when it is read.

Table 34. LANE_1_CODE_ERROR_COUNT(1)

Address: 0x8011		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32785.15:0	Lane 1 code error counter	Output 16-bit counter for invalid code group found in lane 1. Invalid code group is detected when the 8B10B decoder cannot decode the received codeword.	RO/COR

(1) Counter is incremented by 1 when codeword error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter holds on to its value when align_status goes low or when the counter reaches its maximum value. It is cleared when it is read.

Table 35. LANE_2_CODE_ERROR_COUNT(1)

Address: 0x8012		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32786.15:0	Lane 2 code error counter	Output 16-bit counter for invalid code group found in lane 2. Invalid code group is detected when the 8B10B decoder cannot decode the received codeword.	RO/COR

(1) Counter is incremented by 1 when codeword error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter holds on to its value when align_status goes low or when the counter reaches its maximum value. It is cleared when it is read.

Table 36. LANE_3_CODE_ERROR_COUNT(1)

Address: 0x8013		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32787.15:0	Lane 3 code error counter	Output 16-bit counter for invalid code group found in lane 3. Invalid code group is detected when the 8B10B decoder cannot decode the received codeword.	RO/COR

(1) Counter is incremented by 1 when codeword error is found on the corresponding lane and when all the lanes are aligned (align_status should be high). Counter holds on to its value when align_status goes low or when the counter reaches its maximum value. It is cleared when it is read.

Table 37. RX_CHANNEL_SYNC_STATE

Address: 0x8014		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32788.11:9	Channel synchronization FSM state for lane 0	Current state of sync state machine in lane 0	RO
4/5.32788.8:6	Channel synchronization FSM state for lane 1	Current state of sync state machine in lane 1	
4/5.32788.5:3	Channel synchronization FSM state for lane 2	Current state of sync state machine in lane 2	
4/5.32788.2:0	Channel synchronization FSM state for lane 3	Current state of sync state machine in lane 3	

Table 38. RX_LANE_ALIGN_STATUS

Address: 0x8015		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32789.15:12	Align state	Current lane alignment FSM state	RO
4/5.32789.0	Lane Alignment FIFO collision	Collision status for lane alignment FIFO. When high, indicates that there is collision error in lane alignment FIFO.	RO/LH

Table 39. RX_CHANNEL_SYNC_STATUS

Address: 0x8016		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32790.11	Channel Synchronization status for all lanes	1 = Channel synchronization is achieved in all lanes. 0 = Channel synchronization is lost in one or more lanes	RO/LL

Table 40. BIT_ORDER

Address: 0x8017		Default: 0x0005	
Bit(s)	**Name**	**Description**	**Access**
4/5.32791. 3	XGMII RX bit order	When high, reverses the order of bits in the parallel data sent from XAUI RX for each lane.	RW
4/5.32791. 2	XAUI RX bit order	When high, reverses the order of bits in the parallel data received from SERDES RX macros for each lane.	
4/5.32791. 1	XGMII TX bit order	When high, reverses the order of bits in the parallel data received from the XGMII interface each lane.	
4/5.32791. 0	XAUI TX bit order	When high, reverses the order of bits in the parallel data sent to the SERDES TX macro for each lane.	

Table 41. LOOPBACK_CONTROL (1)

Address: 0x8018		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32792. 1	XAUI side loopback	When high, loops back 32 bit data and 4 control bits from the RX path to the TX path. (4/5.0.14 should be 0 else no effect)	RW
4/5.32792. 0	XGMII side loopback	When 1, loops back 40 bit data from TX path to the RX path (4/5.0.14 should be 0 else no effect)	

(1) See Loopback section for more information.

Table 42. TX_BYPASS_CONTROL

Address: 0x8019		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32793.15	TX IPG management bypass	When high, disables IPG management (replacing Idle XGMII characters with /A/K/R/Q/ code-words) in transmit side.	RW
4/5.32793.11	TX CTC Bypass	When high, disables clock tolerance compensation in transmit side	
4/5.32793.7	Lane 3 8B10B encoder bypass	When high, disables 8B10B encoding on the corresponding lane	RW
4/5.32793.6	Lane 2 8B10B encoder bypass		
4/5.32793.5	Lane 1 8B10B encoder bypass		
4/5.32793.4	Lane 0 8B10B encoder bypass		

Table 43. RX_CTC_STATUS

Address: 0x801A		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32794.9	Lane 3 overflow	When high, indicates overflow error in the corresponding lane.	RO/LH
4/5.32794.8	Lane 2 overflow		
4/5.32794.7	Lane 1 overflow		
4/5.32794.6	Lane 0 overflow		
4/5.32794.5	Lane 3 underflow	When high, indicates underflow error in the corresponding lane.	RO/LH
4/5.32794.4	Lane 2 underflow		
4/5.32794.3	Lane 1 underflow		
4/5.32794.2	Lane 0 underflow		
4/5.32794.1	Overflow	When high, indicates overflow error in any lane.	
4/5.32794.0	Underflow	When high, indicates underflow error in any lane.	

Table 44. RX_CTC_INSERT_COUNT

Address: 0x801B		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32795.15:0	Idle insert count	Counter for number of idle insertions in RX side	RO/COR

Table 45. RX_CTC_DELETE_COUNT

Address: 0x801C		Default: 0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
4/5.32796.15:0	Idle delete count	Counter for number of idle deletions on RX side	RO/COR

Table 46. DATA_DOWN

Address: 0x801D		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32797.3	Lane 3 data down	When high, indicates that link for the corresponding lane was inactive (data did not toggle) for 4095 cycles of 312.5MHz clock. The 312.5MHz is generated internally by the PLL from the 156MHz Reference clock.	RO/COR
4/5.32797.2	Lane 2 data down		
4/5.32797.1	Lane 1 data down		
4/5.32797.0	Lane 0 data down		

Table 47. RX_BYPASS_CONTROL

Address: 0x801E		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32798.15	RX CTC bypass	When set, bypasses clock tolerance compensation on the RX side	RW
4/5.32798.14	IPG Checker bypass	When set, bypasses the replacement of /A/K/R/ into Idles and also bypasses end-of-packet error checking.	
4/5.32798.11	Lane 3 8B/10B decoder bypass	When set, disables the 8B/10B decoding for the corresponding lane	RW
4/5.32798.10	Lane 2 8B/10B decoder bypass		
4/5.32798.9	Lane 1 8B/10B decoder bypass		
4/5.32798.8	Lane 0 8B/10B decoder bypass		
4/5.32798.7	Consider sequence column part of IPG	When set, sequence columns are counted as part of IPG When low, sequence columns are not counted as IPG	
4/5.32798.3	RX Lane align bypass	When set, bypasses lane alignment on the RX side	

Table 48. CLOCK_DOWN_STATUS

Address: 0x801F		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32799. 7	Lane 3 clock 312 down	When high, indicates that 312MHz clock is down on the corresponding lane for 255 or more cycles. The detection is done on the transmit side. The 312.5MHz is generated internally by the PLL from the 156MHz Reference clock.	RO/LH
4/5.32799. 6	Lane 2 clock 312 down		
4/5.32799. 5	Lane 1 clock 312 down		
4/5.32799. 4	Lane 0 clock 312 down		
4/5.32799. 3	Lane 3 clock 156 down	When high, indicates that 156MHz XGMII clock is down on the corresponding lane for 255 or more cycles. The detection is done on the transmit side	RO/LH
4/5.32799. 2	Lane 2 clock 156 down		
4/5.32799. 1	Lane 1 clock 156 down		
4/5.32799. 0	Lane 0 clock 156 down		

Table 49. AUXILIARY_RESET_CONTROL

Address: 0x8020		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32800. 15	Transmit auxiliary reset	When set, resets XAUI transmit data path but does not reset any R/W registers.	RW/SC
4/5.32800.14	Receive auxiliary reset	When set, resets XAUI receive data path but does not reset any R/W registers.	
4/5.32800.13	TLK3138 auxiliary reset	When set, resets the DDR, RETIME muxing, A/B muxing logic but does not reset any R/W registers.	

Table 50. TEST_PATTERN_STATUS

Address: 0x8021		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5/32801.15	Test pattern sync status	When high, indicates that preamble for CRPAT/CJPAT has been recovered.	RO

Table 51. LANE_0_ERROR_CODE

Address: 0x8022		Default: 0xCE00	
Bit(s)	**Name**	**Description**	**Access**
4/5.32802.15:7	Lane 0 error code select.	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 0 corresponds to 8′h9C with the control bit being 1′b1. The default values for lanes 0~3 correspond to ||LF||	RW

Table 52. LANE_1_ERROR_CODE

Address: 0x8023		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32803.15:7	Lane 1 error code select.	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 1 corresponds to 8″h00 with the control bit being 1″b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 53. LANE_2_ERROR_CODE

Address: 0x8024		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32804.15:7	Lane 2 error code select.	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 2 corresponds to 8″h00 with the control bit being 1″b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 54. LANE_3_ERROR_CODE

Address: 0x8025		Default: 0x0080	
Bit(s)	**Name**	**Description**	**Access**
4/5.32805.15:7	Lane 3 error code select.	Error code to be transmitted in case of error condition. This applies to both TX and RX data paths. The msb is the control bit; remaining 8 bits constitute the error code. The default value for lane 3 corresponds to 8″h01 with the control bit being 1″b0. The default values for lanes 0~3 correspond to ||LF||	RW

Table 55. RX_PHASE_SHIFT_CONTROL

Address: 0x8026		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32806. 15	Lane 3 phase shift	When set, delays the RX data sent to the XGMII interface by one clock cycle	RW
4/5.32806. 14	Lane 2 phase shift		
4/5.32806. 13	Lane 1 phase shift		
4/5.32806. 12	Lane 0 phase shift		
4/5.32806. 11	XGMII Rx Source timing	When high supports source aligned timing on the XGMII receive output bus When low supports source centered timing on the XGMII receive output bus (Default)	

Table 56. CHANNEL_SYNC_CONTROL

Address: 0x8027		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32807. 15	Lane 3 channel sync bypass	When set, lane synchronization for the corresponding lane is bypassed	RW
4/5.32807. 14	Lane 2 channel sync bypass		
4/5.32807. 13	Lane 1 channel sync bypass		
4/5.32807. 12	Lane 0 channel sync bypass		
4/5.32807. 11	Lane 3 channel sync freeze	When set, freezes the last acquired word alignment for the corresponding lane	RW
4/5.32807. 10	Lane 2 channel sync freeze		
4/5.32807. 9	Lane 1 channel sync freeze		
4/5.32807. 8	Lane 0 channel sync freeze		

Table 57. SERDES_CONFIG_1(1)

Address: 0x8084		Default: 0x806C	
Bit(s)	**Name**	**Description**	**Access**
4/5.32900.15	TXBCLKM CFG[23]	0 = Individual lane TXBCLK ports are used 1 = TXBCLK[1] is used to time TD for all lanes (default)	RW
4/5.32900.14:11	Pre emphasis (TX_CFG[7:4])	See Table 58: Transmit Pre-emphasis Settings Depends on transmit swing setting controlled by CFG_TX [3:2]. These bits do not have any effect if CFG[3:2] = 2″b10 (Default 4'b0000)	
4/5.32900.10:9	SWING (TX_CFG[3:2])	Output swing setting 00 = Maximum transmit amplitude, pre-emphasis available (Default) 01 = 62.5% transmit amplitude, increased pre-emphasis available 10 = 37.5% transmit amplitude, pre-emphasis unavailable 11 = 0% transmit amplitude	RW
4/5.32900.8:7	Slew Rate (CFG[16:15])	Slew Rate setting See Table 59: Slew rate control. Tx Rise and Fall times 00 = Fastest edge rate, independent of DATARATE (Default) 01 = Intermediate edge rate for given DATARATE 10 = Slower intermediate edge rate for given DATARATE 11 = Slowest edge rate for given DATARATE	RW
4/5.32900.6	EXTREF (CFG[14])	0 = Internally generated reference is used to set output amplitude 1 = External reference VREF is used to set output amplitude (Default) External reference is not supported.	RW
4/5.32900.5	AC Coupled (CFG[13])	0 = AC coupled operation is disabled 1 = AC coupled operation is enabled (Default) Only AC coupled mode is supported.	RW
4/5.32900.4	Enable LOL (CFG[12])	0 = Loss of link detection is disabled (Default) 1 = Loss of link detection is enabled	RW
4/5.32900.3	FASTEQ (CFG[11])	0 = Adaptive equalization set on low data rate 1 = Adaptive equalization set on high data rate (Default)	RW
4/5.32900.2	ENEQ (CFG[10])	0 = Adaptive equalization is disabled 1 = Adaptive equalization is enabled (Default)	RW
4/5.32900.1	FASTUPDT (CFG[9])	0 = Fast update mode is disabled (Default) 1 = Fast update mode is enabled	RW
4/5.32900.0	FASTLOCK (CFG[8])	0 = Fast-lock mode is disabled (Default) 1 = Fast-lock mode is enabled	RW

(1) Above control bits are only for vendor testing only. Customer should leave them at their default values. They can be accessed from A side or B side.

Table 58. Transmit Pre-Emphasis Settings

MODE	CFG_TX[7:4]	100% SWING		62.5% SWING	
		1st BIT	2nd BIT	1st BIT	2nd BIT
Disabled	0000	0%	0%	0%	0%
1 – Tap	0001	5%	0%	9%	0%
	0010	11%	0%	19%	0%
	0011	18%	0%	32%	0%
	0100	25%	0%	47%	0%
	0101	33%	0%	67%	0%
	0110	43%	0%	92%	0%
	0111	67%	0%	178%	0%
	1000	100%	0%	400%	0%

Table 58. Transmit Pre-Emphasis Settings (continued)

MODE	CFG_TX[7:4]	100% SWING		62.5% SWING	
		1st BIT	2nd BIT	1st BIT	2nd BIT
2 –Tap	1001	25%	18%	47%	32%
	1010	33%	18%	67%	32%
	1011	33%	25%	67%	47%
	1100	43%	25%	92%	47%
	1101	54%	25%	127%	47%
	1110	82%	54%	257%	127%
	1111	100%	54%	400%	127%

The slew rate of the differential driver may be controlled to suit different transmission media and data rates. This is controlled through CFG [16:15] and CFG [6:5], the effects are shown in Table 58.

Table 59. Slew Rate Control. Tx Rise and Fall Times

	CFG[6:5] = 01 or 10		CFG[6:5] = 00	
CFG[16:15]	MIN	MAX	MIN	MAX
00	90 ps	104 ps	90 ps	104 ps
01	146 ps	202 ps	101 ps	145 ps
10	173 ps	240 ps	126 ps	169 ps
11	281 ps	403 ps	144 ps	196 ps

Table 60. SERDES_CONFIG_2

Address: 0x8085		Default: 0x0AC0	
Bit(s)	Name	Description	Access
4/5.32901.15	JNCSEL (CFG[7])	0 = JOGCOM[0..7] controls whether comma alignment is enabled on lane 0..7 (Default) 1 = JOGCOM[0..7] induces an alignment jog on lane 0..7	RW
4/5.32901.14:13	DATARATE (CFG[6:5] / CFG[20:19])	00 = Full Rate (Default) 01 = Half Rate 10 = Quarter Rate 11 = Reserved	
4/5.32901.12	EN8 (CFG[4])	0 = 10 bit operation (Default) 1 = 8 bit operation	
4/5.32901.11	PLL_LBW (CFG[3])	0 = High loop bandwidth 1 = Low loop bandwidth (Default)	
4/5.32901.10:8	PLLMUL (CFG[2:0])	PLL multiply factor. Can be calculated from following equation. $\text{REFCLK(freq)} = \frac{\text{LINERATE}}{\text{PLLMULTIPLY} \times 2}$ 000 = 5x 001 = 25x 010 = 10x (Default) 011 = 15x 100 = 4x 101 = 20x 110 = 8x 111 = Reserved	
4/5.32901.7	ENTEST_TX (TX_CFG[1])	1 = Tx Test Features Enabled (Default) 0 = Tx Test Features Disabled	
4/5.32901.6	ENTEST_RX (RX_CFG[1])	1 = Rx Test Features Enabled (Default) 0 = Rx Test Features Disabled	

Table 61. SERDES_DATA_CONTROL (1)

Address: 0x8086		Default: 0xFFFF	
Bit(s)	**Name**	**Description**	**Access**
4/5.32902.15:8	Enable TX (TX_CFG[0])	1 = Transmit data pair is enabled for channels 7~0 0 = Transmit data pair is disabled for channels 7~0 (Bit 15 corresponds to channel 7)	RW
4/5.32902.7:0	Enable RX (RX_CFG[0]	1 = Receive data pair is enabled for channels 7~0. 0 = Receive data pair is disabled for channels 7~0 (Bit 7 corresponds to channel 7)	

(1) When power down mode is enabled using Control register (4/5.0), the SERDES macros go into power down mode where the TX and RX data pairs are disabled for all channels. When A side is powered down, TX and RX data pairs are disabled for channels 3~0. When B side is powered down TX and RX data pairs are disabled for channels 7~4. These low-power modes override the settings in this register. Bits 11:8 corresponds to A side and bits 15:12 corresponds to B side of TX path. Bits 3:0 corresponds to A side and bits 7:4 corresponds to B side of RX path. In normal mode(A side as primary channel, A_B = 1) all the bits needs to be enabled for the normal operation and when B side acts as primary channel(A_B = 0), A side bits can be disabled.

Table 62. SERDES_PLL_CONTROL

Address: 0x8087		Default: 0x8000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32903.15	PLL Enable	1 = Enabled 0 = Disabled	RW

Table 63. SERDES_SYNC_STATUS

Address: 0x8088		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32904.15:8	Sync	Synchronous detect. When high, indicates a comma character has been detected for lanes 7~0 (Feature not supported. Bits made available for future use)	RO
4/5.32904.7:0	Loss of link	Loss of link. When high, indicates that link at the receiver 7~0 lanes is lost (Feature not supported. Bits made available for future use)	

Table 64. SERDES_TESTFAIL_CONTROL

Address: 0x8089		Default: 0x8000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32905.15	Test fail select	Test fail select controls. According to these selection bits, following Test fail signals are given out as testfail_mux_out to the Output Pins 0 = TX TESTFAIL selected 1 = RX TESTFAIL selected	RW

Table 65. SERDES_TEST_CONFIG(1)

Address: 0x808A		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32906.15:14	TESTCFG[15:14]	Reserved	RW
4/5.32906.13:12	EQTESTMD TESTCFG[13:12]	00 – Equalizer test mode disabled (Default) 01 – 16 Parametric devices observable 10 – 17 Parametric devises are observable 11 – High impedance mode	
4/5.32906.11	PADLPBACK TESTCFG[11]	0 – Pad loop back disabled (Default) 1 – Pad loop back enabled TESTCFG[10] should be enabled else no effect	
4/5.32906.10	LOOPBACK TESTCFG[10]	0 – Loop back disabled (Default) 1 – Loop back enabled (*For Internal Test Pattern Verification*)	
4/5.32906.9	BSIN	Enable boundary scan inputs. This bit has no affect on transmit SERDES macro.	
4/5.32906.8	BSOUT	Enable boundary scan outputs. This bit has no affect on receive SERDES macro.	
4/5.32906.7:4	AFR TESTCFG[7:4]	Asynchronous frequency ramp mode. Refer to Table 66: Asynchronous frequency ramp mode (Default 4'b0000)	
4/5.32906.3	TESTCLK TESTCFG[3]	0 – PLL bypass disabled (Default) 1 – PLL bypass enabled	
4/5.32906.2:0	TESTPATT TESTCFG[2:0]	000 – Test pattern gen/verification disabled (Default) 001 – Clock pattern gen/verification enabled 010 – 2^7– 1 PRBS gen/verification enabled 011 – 2^{23}– 1 PRBS gen/verification enabled 100 – Low frequency clock pattern 101 – Reserved 110 – Reserved 111 – Reserved	

(1) Above control bits are only for vendor testing only. Customer should leave them at their default values.

Table 66. Asynchronous Frequency Ramp Mode

AFR		
CFG[9]	**TESTCFG[7:4]**	**RAMP MODE**
x	x x x 0	Disabled
0	0 0 0 1	– 521 ppm
0	0 0 1 1	+521 ppm
0	0 1 0 1	–390 ppm
0	0 1 1 1	+390 ppm
0	1 0 0 1	–195 ppm
0	1 0 1 1	+195 ppm
0	1 1 0 1	–98 ppm
0	1 1 1 1	+98 ppm
1	0 0 0 1	–521 ppm
1	0 0 1 1	+521 ppm
1	0 1 0 1	– 390 ppm
1	0 1 1 1	+390 ppm
1	1 0 0 1	– 195 ppm
1	1 0 1 1	+195 ppm
1	1 1 0 1	–695 ppm
1	1 1 1 1	+695 ppm

Table 67. REDUNDANCY_CONTROL

Address: 0x808B		Default: 0x2700	
Bit(s)	**Name**	**Description**	**Access**
4/5.32907.15:13	External voltage divider control 1	Setting for External voltage divider for SERDES 1 [15, 14, 13] 0 0 0 – 0.50 v 0 0 1 – 0.40 v (Default) 0 1 0 – 0.45 v 0 1 1 – 0.35 v 1 0 0 – 0.475 v 1 0 1 – 0.375 v 1 1 0 – 0.425 v 1 1 1 – 0.325 v	RW
4/5.32907.12:10	External voltage divider control 0	Setting for External voltage divider for SERDES 0 [12, 11, 10] 0 0 0 – 0.50 v 0 0 1 – 0.40 v (Default) 0 1 0 – 0.45 v 0 1 1 – 0.35 v 1 0 0 – 0.475 v 1 0 1 – 0.375 v 1 1 0 – 0.425 v 1 1 1 – 0.325 v	
4/5.32907.9	HSTL input termination enable 1	Active LOW termination enable. When 0 enables termination resistance on HSTL inputs on B side. Default HIGH (termination disable)	
4/5.32907.8	HSTL input termination enable 0	Active LOW termination enable. When 0 enables termination resistance on HSTL inputs on A side. Default HIGH (termination disable)	
4/5.32907.7	Redundant XGMII mode	When set, puts device in Redundant XGMII Mode	
4/5.32907.6	Redundant XAUI mode	When set, puts device in Redundant XAUI Mode	
4/5.32907.5	XGMII 1 Tristate	When set, 3-states the data outputs on the XGMII 1 side.	
4/5.32907.4	IDLE	When set, during non-retime mode, generates Idle on all lanes of the redundant XAUI channel.	
4/5.32907.3	A/B select	When set, channel A is selected as primary else channel B acts as primary channel.	
4/5.32907.2	RETIME	When set, device goes into retime mode else non-retime mode. (Default 0)	
4/5.32907.1	XGMII 0 Tristate	When set, 3-states the data outputs on the XGMII 0 side.	
4/5.32907.0	Transition code	Output code to be sent during transition from A to B or B to A. When 0 FE, when 1 LF is transmitted.	

Table 68. TRANSITION_TIME_CONTROL

Address: 0x808C		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32908.15:0	Transition time	Transition time interval control in 312.5MHz clock intervals (In Redundant XAUI Mode). Transition time interval control in 156.25MHz clock intervals (In Redundant XGMII Mode).	RW

Table 69. SERDES_JOGCOM_CONTROL(1)

Address: 0x808E		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32910.15:8	JOGCOM[7:0] RX_CFG[2]	Jog alignment/ Comma enable bit (one bit per lane). When CFG[7] is set to 0, this bit acts as comma alignment enable control. JOGCOM[i] = 0 : Comma alignment enabled for lane i JOGCOM[i] = 1 : Comma alignment disabled for lane i When CFG[7] is set to 1, this bit induces alignment jog on lanes 7..0 JOGCOM[i] = 0 : Alignment jog disabled for lane i JOGCOM[i] = 1 : Alignment jog enabled for lane i	RW

(1) Above control bits are for vendor testing only. Customer should leave them at their default values.

Table 70. DIE_ID_3

Address: 0x8090		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32912.15:0	Die ID [63:48]	Bits [63:48] of the Die ID. Unique TI DIE identifier.	RO

Table 71. DIE_ID_2

Address: 0x8091		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32913.15:0	Die ID [47:32]	Bits [47:32] of the Die ID. Unique TI DIE identifier.	RO

Table 72. DIE_ID_1

Address: 0x8092		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32914.15:0	Die ID [31:16]	Bits [31:16] of the Die ID. Unique TI DIE identifier.	RO

Table 73. : DIE_ID_0

Address: 0x8093		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32915.15:0	Die ID [15:0]	Bits [15:0] of the Die ID. Unique TI DIE identifier.	RO

Table 74. BIST_CONTROL

Address: 0x80A0		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32928.11	bist_enable	When set enables memory BIST testing	RW

Table 75. BIST_STATUS

Address: 0x80A1		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32929.15	bist_fail_l	When low, indicates memory BIST test has failed.	RO
4/5.32929.14	bist_done	When high, indicates memory BIST test has completed	

Table 76. RESERVED_CONTROL

Address: 0x80A2		Default: 0x8000	
Bit(s)	**Name**	**Description**	**Access**
4/5.32930.15	Reserved	Reserved	RW

JITTER TEST PATTERN GENERATION AND VERIFICATION

Use one of the following procedures to generate and verify the respective jitter test pattern:

- High Frequency Test Pattern:
  - Issue a hard or soft reset
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register to clear.
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register and verify it is cleared. This indicates that the RX link is up
  - Bypass the Lane Alignment by writing 1 to the RX Lane Align Bypass bit of the RX_BYPASS_CONTROL register.
  - Write 00 to the pattern_select field of the TEST_CONTROL register (4/5.25.1:0).
  - Start the pattern generation on the XAUI_TX and verification on the XAUI_RX by writing 1 to the test_enable bit of the TEST_CONTROL register (4/5.25.2).

  - Read the test pattern error counters for all channels (CHANNEL_0~3_ TEST_ERR_CNT), to clear the counters.
  - At this point the pattern verification is in progress and the errors are reported in the error counters.
  - Reading the counters has no effect on the test except clearing them, i.e. the verification of the pattern continues until the test_enable bit of the TEST_CONTROL register is cleared.
- Low Frequency Test Pattern:
  - Issue a hard or soft reset
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register to clear
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register and verify it is cleared. This indicates that the RX link is up.
  - Bypass the Lane Alignment by writing 1 to the RX Lane Align Bypass bit of the RX_BYPASS_CONTROL register.
  - Write 01 to the pattern_select field of the TEST_CONTROL register (4/5.25.1:0).
  - Start the pattern generation on the XAUI_TX and verification on the XAUI_RX by writing 1 to the test_enable bit of the TEST_CONTROL register (4/5.25.2).
  - Read the test pattern error counters for all channels (CHANNEL_0~3_ TEST_ERR_CNT), to clear the counters
  - At this point the pattern verification is in progress and the errors are reported in the error counters.
  - Reading the counters has no effect on the test except clearing them, i.e. the verification of the pattern continues until the test_enable bit of the TEST_CONTROL register is cleared.
- Mixed Frequency Test Pattern:
  - Issue a hard or soft reset
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register to clear.
  - Read the RX Local Fault bit (4/5/8.10) of the XS_STATUS_2 register and verify it is cleared. This indicates that the RX link is up
  - Bypass the Lane Alignment by writing 1 to the RX Lane Align Bypass bit of the RX_BYPASS_CONTROL register.
  - Write 10 to the pattern_select field of the TEST_CONTROL register (4/5.25.1:0).
  - Start the pattern generation on the XAUI_TX and verification on the XAUI_RX by writing 1 to the test_enable bit of the TEST_CONTROL register (4/5.25.2).
  - Read the test pattern error counters for all channels (CHANNEL_0~3_ TEST_ERR_CNT), to clear the counters.
  - At this point the pattern verification is in progress and the errors are reported in the error counters.
  - Reading the counters has no effect on the test except clearing them, i.e. the verification of the pattern continues until the test_enable bit of the TEST_CONTROL register is cleared.
- Continuous Random Test Pattern (CRPAT):
  - Issue a hard or soft reset
  - Read the test pattern error counter cr_cj_err_cnt registers (4/5.32778 – 4/5.32779) to clear
  - Write 1 to the crpat_enable bit of the Vendor Specific TEST_CONFIG register (4/5.32768.1).
  - Enable the CRPAT verifier by writing 1 to CRPAT Check Enable bit of the TEST_VERIFICATION_CONTROL register (4/5.32769.1)
  - In order for the Test Pattern Verifier to start checking the test pattern, it has to receive the Preamble /SFD that is sent at every packet from the test pattern generator. To make sure that the test pattern checking has started, read the 4/5/32801.15 (Test Pattern Status) bit of the Test Pattern Verification Status register. Make sure that the Test Pattern Sync bit is HIGH. If the sync status is not high, this indicates that the verifier never received the Preamble, which may indicate a more severe link problem.
  - Read Align Status (4/5.1.2) to clear old information. Discard the values read.
  - Read the CRPAT_CJPAT_TEST_ERROR_COUNT register. Align Status (4/5.1.2) has to read HIGH for the CRPAT_CJPAT_ERR_COUNTER to be valid as this test is packet based. If Align Status reads LOW, the test is not actively comparing data.
  - The CRPAT_CJPAT_TEST_ERROR_COUNT counter can be read as many times as desired.
  - If another test is to be performed go to the first step

- Continuous Jitter Test Pattern (CJPAT):
  - Issue a hard or soft reset
  - Read the test pattern error counter cr_cj_err_cnt registers (4/5.32778 – 4/5.32779) to clear
  - Write 1 to the crpat_enable bit of the Vendor Specific TEST_CONFIG register (4/5.32768.0).
  - Enable the CJPAT verifier by writing 1 to CJPAT Check Enable bit of the TEST_VERIFICATION_CONTROL register (4/5.32769.0)
  - In order for the Test Pattern Verifier to start checking the test pattern, it has to receive the Preamble /SFD that is sent at every packet from the test pattern generator. To make sure that the test pattern checking has started, read the 4/5/32801.15 (Test Pattern Status) bit of the Test Pattern Verification Status register. Make sure that the Test Pattern Sync bit is HIGH. If the sync status is not high, this indicates that the verifier never received the Preamble, which may indicate a more severe link problem.
  - Read Align Status (4/5.1.2) to clear old information. Discard the values read.
  - Read the CRPAT_CJPAT_TEST_ERROR_COUNT register. Align Status (4/5.1.2) has to read HIGH for the CRPAT_CJPAT_ERR_COUNTER to be valid as this test is packet based. If Align Status reads LOW, the test is not actively comparing data.
  - The CRPAT_CJPAT_TEST_ERROR_COUNT counter can be read as many times as desired.
  - If another test is to be performed go to the first step

If more than one test is specified results are unpredictable.

SIGNAL PIN DESCRIPTION

Table 77. Global Signals

<table>
<tr><th>SIGNAL</th><th>LOCATION</th><th>VOLTAGE</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>RST_N</td><td>D08</td><td>VDDP/
VDDO</td><td>2.5V
LVCMOS
I
Internal
Pull Up</td><td>Chip Reset (Active Low) When asserted (low logic level), this signal reinitializes the entire device. Must be asserted (low logic level) for at least 10 µs after device power up.</td></tr>
<tr><td>REFSEL</td><td>L18</td><td>VDDP/
VDDO</td><td>2.5V
LVCMOS
I
Internal
Pull Down</td><td>Reference Select This input selects which reference clock input to use as the default internal clock (0 = REFCLK0, 1 = REFCLK1).</td></tr>
<tr><td>REFINEN[1:0]</td><td>E15, E14</td><td>VDDP/
VDDO</td><td>2.5V
LVCMOS
I
Internal
Pull Down</td><td>Reference Enable This signal selects which reference clock source is to be used for a given XGXS core (Receive and Transmit Directions).
<table>
<tr><th>REFSEL</th><th>REFINEN[0]</th><th>Clock Selected for XGXS 0</th></tr>
<tr><td>0</td><td>0</td><td>REFCLK0</td></tr>
<tr><td>0</td><td>1</td><td>REFCLK0</td></tr>
<tr><td>1</td><td>0</td><td>REFCLK0</td></tr>
<tr><td>1</td><td>1</td><td>REFCLK1</td></tr>
</table>
<table>
<tr><th>REFSEL</th><th>REFINEN[1]</th><th>Clock Selected for XGXS 1</th></tr>
<tr><td>0</td><td>0</td><td>REFCLK1</td></tr>
<tr><td>0</td><td>1</td><td>REFCLK0</td></tr>
<tr><td>1</td><td>0</td><td>REFCLK1</td></tr>
<tr><td>1</td><td>1</td><td>REFCLK1</td></tr>
</table></td></tr>
</table>

Table 78. JTAG Signals

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
TDI	V19	VDDP/ VDDO	2.5V LVCMOS Input (Internal Pullup)	**JTAG Input Data.** TDI is used to serially shift test data and test instructions into the device during the operation of the test port.
TDO	W20	VDDP/ VDDO	2.5V LVCMOS Output	**JTAG Output Data.** TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state.
TMS	U18	VDDP/ VDDO	2.5V LVCMOS Input (Internal Pullup)	**JTAG Mode Select.** TMS is used to control the state of the internal test-port controller.
TCK	Y20	VDDP/ VDDO	2.5V LVCMOS Input	**JTAG Clock.** TCK is used to clock state information and test data into and out of the device during the operation of the test port.
TRST_N	AB20	VDDP/ VDDO	2.5V LVCMOS Input (Internal Pull Down)	**JTAG Test Reset.** TRST_N is used to reset the JTAG logic into system operational mode.

Table 79. MDIO Related Signals

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
MDEN0	AB03	VDDM0	1.2/2.5V LVCMOS Input	**Management Interface Enable** Enables MDIO management port 0 when asserted (high). This must be tied to logic zero if management port 0 is unused. It is expected that MDIO Interface 0 and 1 are not both simultaneously active.
MDEN1	F14	VDDM1	1.2/2.5V LVCMOS Input	**Management Interface Enable** Enables MDIO management port 1 when asserted (high) . This must be tied to logic zero if management port 1 is unused. It is expected that MDIO Interface 0 and 1 are not both simultaneously active.
MDC0	V04	VDDM0	1.2/2.5V LVCMOS Input	**Management Interface Clock (Port 0)** This clock is used to sample the MDIO0 signal. This must be tied to logic zero if management port 0 is unused.
MDIO0	AA03	VDDM0	1.2/2.5V LVCMOS Input/ Output	**Management Interface Data (Port 0)** This bidirectional data line for MDIO Port 0 is sampled on the rising edge of MDC0. This must be pulled to logic zero if management port 0 is unused.
MDC1	F16	VDDM1	1.2/2.5V LVCMOS Input	**Management Interface Clock (Port 1)** This clock is used to sample the MDIO1 signal. This must be tied to logic zero if management port 1 is unused.
MDIO1	F15	VDDM1	1.2/2.5V LVCMOS Input/ Output	**Management Interface Data (Port 1)** This bidirectional data line for MDIO Port 1 is sampled on the rising edge of MDC1. This must be pulled to logic zero if management port 1 is unused.

Table 80. Parallel Data Pins

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
TX_CLK0_[3:0]	D04, J06, F02, J02	VDDQ0/ VTT0/ VREF0	1.5V HSTL Input	**Transmit Data Clocks (XGMII 0)** These four signals are the XGMII side input clocks per channel. Only TX_CLK0_[1] is used to sample all 36 data/control inputs. TX_CLK0_[3:2,0] are unused, and should be driven (not floating) in the application.
TX_CLK1_[3:0]	U20, P22, M20, K21	VDDQ1/ VTT1/ VREF1	1.5V HSTL Input	**Transmit Data Clocks (XGMII 1)** These four signals are the XGMII side input clocks per channel. Only TX_CLK1_[1] is used to sample all 36 data/control inputs. TX_CLK1_[3:2,0] are unused, and should be driven (not floating) in the application.

Table 80. Parallel Data Pins (continued)

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
TXD0_[31:0]	C04, F05, B06, C05, E04, F04, G05, B04, H05, C03, E03, H04, F03, G03, B02, J05, D02, J04, E02, G02, J03, K05, H02, D01, F01, K03, G01, L06, H01, M05, J01, L04	VDDQ0/ VTT0/ VREF0	1.5V HSTL Input	**Transmit Data Pins (XGMII 0)** Parallel interface data pins.
TXD1_[31:0]	U22, U21, U19, T18, T20, T19, R18, T21, R21, R19, R20, N22, P21, P20, P19, P18, M21, N19, N20, L22, K22, N18, J22, L21, L20, E22, D22, G22, C22, M19, J21, M18	VDDQ1/ VTT1/ VREF1	1.5V HSTL Input	**Transmit Data Pins (XGMII 1)** Parallel interface data pins.
TXC0_[7:0]	E05, B03, H03, K06, B05, D03, C02, E01	VDDQ0/ VTT0/ VREF0	1.5V HSTL Input	**Transmit Data Control (XGMII 0)** XGMII Control inputs. Bits 7:4 are unused, and 3:0 are the control bits per lane.
TXC1_[7:0]	W22, T22, N21, F22, V22, R22, M22, H22	VDDQ1/ VTT1/ VREF1	1.5V HSTL Input	**Transmit Data Control (XGMII 1)** XGMII Control inputs. Bits 7:4 are unused, and 3:0 are the control bits per lane
RX_CLK0_[3:0]	Y02, V02, P05, M04	VDDQ0	1.5V HSTL Output	**Receive Data Clocks (XGMII 0)** These four signals are the XGMII side output clocks per channel. Only RX_CLK0_[1] is used. RX_CLK0_[3:2,0] are driven static.
RX_CLK1_[3:0]	C12, E19, J18, K20	VDDQ1	1.5V HSTL Output	**Receive Data Clocks (XGMII 1)** These four signals are the XGMII side output clocks per channel. Only RX_CLK1_[1] is used. RX_CLK1_[3:2,0] are driven static.
RXD0_[31:0]	Y03, W03, U05, V03, T05, U04, AB01, T06, T04, W02, R06, U02,R05, R04, Y01, W01, T02, P04, R03, V01, N04, U01, N05, R02, R01, P01, P02, N01, N02, M02, M01, M03	VDDQ0	1.5V HSTL Output	**Receive Data Pins (XGMII 0)** Parallel interface data pins.

Table 80. Parallel Data Pins (continued)

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
RXD1_[31:0]	D12, D13, E17, D15, D14, D16, D17, C10, D18, C17, H18, G18, E18, G19, D19, C18, G20, J19, C19, F20, H19, C20, K18, H20, D21, E21, G21, J20, H21, F21, B21, L19	VDDQ1	1.5V HSTL Output	**Receive Data Pins (XGMII 1)** Parallel interface data pins.
RXC0_[7:0]	AB02, AA01, T03, N03, AA02, U03, P03, T01	VDDQ0	1.5V HSTL Output	**Receive Data Control (XGMII 0)** XGMII Control inputs. Bits 7:4 are unused, and 3:0 are the control bits per lane.
RXC1_[7:0]	D11, F19, E20, K19, C11, F18, D20, C21	VDDQ1	1.5V HSTL Output	**Receive Data Control (XGMII 1)** XGMII Control inputs. Bits 7:4 are unused, and 3:0 are the control bits per lane.

Table 81. LED Interface Pins

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
PLL_LOCK1	Y21	VDDP/ VDDO	2.5V LVCMOS Output 12mA	**PLL Lock** Indicates when PLL 1 is locked. (Currently, this pin is for compatibility, and not supported in TLK3138, and is tied high internally). TLK3138 3-states this pin during RESET_N asserted.
PLL_LOCK0	AB22	VDDP/ VDDO	2.5V LVCMOS Output 12mA	**PLL Lock** Indicates when PLL 0 is locked. (Currently, this pin is for compatibility, and not supported in TLK3138, and ia tied high internally). TLK3138 3-states this pin during RESET_N asserted.
LINKLED1	AA21	VDDP/ VDDO	2.5V LVCMOS Output 12mA	**Link Up** Indicates when asserted XGXS 1 link is up. TLK3138 3-states this pin during RESET_N asserted.
LINKLED0	AB21	VDDP/ VDDO	2.5V LVCMOS Output 12mA	**Link Up** Indicates when asserted XGXS 0 link is up. TLK3138 3-states this pin during RESET_N asserted.
TXLED1	AA22	VDDP/ VDDO	2.5V LVCMOS Output 12mA	**Transmit Packets** Indicates when XGXS 1 is transmitting packets. TLK3138 3-states this pin during RESET_N asserted. This signal toggles at a 6-Hz rate when the chip is transmitting data on the XAUI interface. When not transmitting, this signal is deasserted.
TXLED0	V21	VDDP/ VDDO	2.5V LVCMOS Output/ Input* 12mA Internal Pull Down	**Transmit Packets** Indicates when XGXS 0 is transmitting packets. Should have a pullup or pull down resistor to support bootstrap operation (see Table 82). TLK3138 3-states this pin during RESET_N asserted. This signal toggles at a 6-Hz rate when the chip is transmitting data on the XAUI interface. When not transmitting, this signal is deasserted.
RXLED1	W21	VDDP/ VDDO	2.5V LVCMOS Output 12mA	**Receive Packets** Indicates when XGXS 1 is receiving packets. TLK3138 3-states this pin during RESET_N asserted. This signal toggles at a 6-Hz rate when the chip is receiving data on the XAUI interface. When not receiving, this signal is deasserted.
RXLED0	Y22	VDDP/ VDDO	2.5V LVCMOS Output 12mA	**Receive Packets** Indicates when XGXS 0 is receiving packets. TLK3138 3-states this pin during RESET_N asserted. This signal toggles at a 6 Hz rate when the chip is receiving data on the XAUI interface. When not receiving, this signal is deasserted.

Table 82. Bootstrap Interface Pins

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
XGMII0_ST	D06	VDDP/ VDDO	2.5V LVCMOS Input Internal Pull Down	**Not Used** Not used, exists for compatibility. Tie High or Low in Application.
MDIO0_ST	E07	VDDP/ VDDO	2.5V LVCMOS Input Internal Pull Down	**Not Used** Not used, exists for compatibility. Tie High or Low in Application.
MDMX	E06	VDDP/ VDDO	2.5V LVCMOS Input Internal Pull Down	**Not Used** Not used, exists for compatibility. Tie High or Low in Application.
PRTAD[4:0]	C07, B08, C06, D05, B07	VDDP/ VDDO	2.5V LVCMOS Input Internal Pull Down	**Port Address** Used to select the Device Id/Port ID in Clause 45 MDIO modes. Only the upper four bits are used.
DEVID[4:0]	AB22, W21, AA22, Y22, V21	VDDP/ VDDO	Ishared	**Device ID** Selects Device ID for the MDIO interface. Only the lower bit is used (Only DTE or PHY device ID is supported). Shared with PLL_LOCK0, RXLED1, TXLED1, RXLED0, and TXLED0.

Table 83. Serial Side Data/Clock Pins

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
REFCLKP0/ REFCLKN0	U10, V10	AVDD	LVDS/ DPECL Input	**Reference Clock** 156.25 MHz Differential Input Reference Clock 0. AC Coupled.
REFCLKP1/ REFCLKN1	U16, V16	AVDD	LVDS/ DPECL Input	**Reference Clock** 156.25 MHz Differential Input Reference Clock 1. AC Coupled.
TDP3_0/TDN3_0 TDP2_0/TDN2_0 TDP1_0/TDN1_0 TDP0_0/TDN0_0	AA08, AB08, W09, Y09, AA10, AB10, W11, Y11	AVDD	CML Output	**Transmit Differential Pairs, XAUI Lane A (Lane 0)**, High speed serial outputs. Minimum bit time 320 pS. AC coupling required.
TDP3_1/TDN3_1 TDP2_1/TDN2_1 TDP1_1/TDN1_1 TDP0_1/TDN0_1	AA16, AB16, W17, Y17, AA18, AB18, W19, Y19	AVDD	CML Output	**Transmit Differential Pairs, XAUI Lane B (Lane 1)**, High speed serial outputs. Minimum bit time 320 pS. AC coupling required.
RDP3_0/RDN3_0 RDP2_0/RDN2_0 RDP1_0/RDN1_0 RDP0_0/RDN0_0	W07, Y07, AA06, AB06, W05, Y05, AA04, AB04	AVDD	CML Input	**Receive Differential Pairs, XAUI Lane A (Lane 0)**, High speed serial inputs with on-chip 100Ω differential termination. Each input pair is terminated differentially across an on-chip 100-Ω resistor. Minimum bit time 320 pS.
RDP3_1/RDN3_1 RDP2_1/RDN2_1 RDP1_1/RDN1_1 RDP0_1/RDN0_1	W15, Y15, AA14, AB14, W13, Y13, AA12, AB12	AVDD	CML Input	**Receive Differential Pairs, XAUI Lane B (Lane 1)**, High speed serial inputs with on-chip 100Ω differential termination. Each input pair is terminated differentially across an onchip 100-Ω resistor. Minimum bit time 320 pS.

Table 84. Miscellaneous Pins

SIGNAL	LOCATION	VOLTAGE	TYPE	DESCRIPTION
GPI4 GPI3 GPI0	R09, R14, R17	VDDP/ VDDO	LVCMOS 2.5V Input	**General Purpose Input**– Must Be Grounded in the System Application.
GPO[5:0]	D07, U08, U14, V08, V14, V20	VDDP/ VDDO	LVCMOS 2.5V Output	**General Purpose Output**– Must be N/C in the System Application.

Table 85. Voltage Supply and Reference Pins

SIGNAL	LOCATION	TYPE	DESCRIPTION
DVDD	A01, A04, A09, A14, A19, A22, E16, H08, H09, H10, H11, H12, H13, H14, H15, J08, J09, J10, J11, J12, J13, J14, J15, K01, K08, K15, L01, M06, M08, M15, P07	P	Digital Core Power (1.2V)
VDDP	A06, A11, A12, A17, E11, G07, G09, G12, G16, J07, J16, L08, L15, L17, N07, N16, R16, AA20	P	Pad Pre-Driver Power (2.5V)
VDDO	A05, A10, A13, A18, F13, G10, G13, G15, H07, H16, L07, L16	P	CMOS Pad Driver Power (2.5V)
VDDM[1:0]	P16, P06	P	Management Pad Power (2.5V, 1.2V) VDDM[1] is used to power MDEN1, MDIO1, MDC1. VDDM[0] is used to power MDEN0, MDIO0, MDC0. These voltages can be at either 2.5V or 1.2V independently.
VDDQ1	A15, A20, G11, G17, H17, K17	P	XGMII 1 Pad Power (1.5V)
VDDQ0	A03, A08, C01, F07, F09, F11, G06, K04, N06	P	XGMII 0 Pad Power (1.5V)
VREF	A02, A16, A21, F12, G14, N17, A07, B01, F10, H06, K07, M07, R07, M17, L05	P	XGMII Input Pad Termination Power (.75V) Should track VDDQ1/2 and VDDQ0/2.
VREF1	F08	P	XGMII Input Pad Termination Power (.75V) Should track VDDQ1/2 and VDDQ0/2.
VREF2	G04	P	XGMII Input Pad Termination Power (.75V) Should track VDDQ1/2 and VDDQ0/2.
VREF3	J17	P	XGMII Input Pad Termination Power (.75V) Should track VDDQ1/2 and VDDQ0/2.
VREF4	P17	P	XGMII Input Pad Termination Power (.75V) Should track VDDQ1/2 and VDDQ0/2.
DGND	B09, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B22, C08, C09, C13, C14, C15, C16, D09, D10, E08, E09, E10, E12, E13, F06, F17, G08, K02, K09, K10, K11, K12, K13, K14, K16, L02, L03, L09, L10, L11, L12, L13, L14, M09, M10, M11, M12, M13, M14, M16, N08, N09, N10, N11, N12, N13, N14, N15, P08, P09, P10, P11, P12, P13, P14, P15, R10, R11, R12, R13	G	Digital Ground
AVDD	U09, U17, V11, Y04, Y06, Y08, Y10, Y12, Y14, Y16, Y18, AB05, AB07, AB09, AB11, AB13, AB15, AB17, AB19	P	Analog Power Supply (1.2V)
AGND	R08, R15, T07, T08, T09, T10, T11, T12, T13, T14, T15, T16, T17, U06, U07, U11, U12, U13, U15, V05, V06, V07, V09, V12, V13, V15, V17, V18, W04, W06, W08, W10, W12, W14, W16, W18, AA05, AA07, AA09, AA11, AA13, AA15, AA17, AA19	G	Analog Ground

	01	02	03	04	05	06	07	08	09	10	11
A	DVDD	VREF	VDDQ0	DVDD	VDDO	VDDP	VREF	VDDQ0	DVDD	VDDO	VDDP
B	VREF	TXD0_17	TXC0_6	TXD0_24	TXC0_3	TXD0_29	PRTAD0	PRTAD3	DGND	DGND	DGND
C	VDDQ0	TXC0_1	TXD0_22	TXD0_31	TXD0_28	PRTAD2	PRTAD4	DGND	DGND	RXD1_24	RXC1_3
D	TXD0_08	TXD0_15	TXC0_2	TX_CLK0_3	PRTAD1	XGMII0_ST	GPO5	RST_N	DGND	DNGD	RXC1_7
E	TXC0_0	TXD0_13	TXD0_21	TXD0_27	TXC0_7	MDMX	MDIO0_ST	DGND	DGND	DGND	VDDP
F	TXD0_07	TX_CLK0_1	TXD0_19	TXD0_26	TXD0_30	DGND	VDDQ0	VREF1	VDDQ0	VREF	VDDQ0
G	TXD0_05	TXD0_12	TXD0_18	VREF2	TXD0_25	VDDQ0	VDDP	DGND	VDDP	VDDO	VDDQ1
H	TXD0_03	TXD0_09	TXC0_5	TXD0_20	TXD0_23	VREF	VDDO	DVDD	DVDD	DVDD	DVDD
J	TXD0_01	TX_CLK0_0	TXD0_11	TXD0_14	TXD0_16	TX_CLK0_2	VDDP	DVDD	DVDD	DVDD	DVDD
K	DVDD	DGND	TXD0_06	VDDQ0	TXD0_10	TXC0_4	VREF	DVDD	DGND	DGND	DGND
L	DVDD	DGND	DGND	TXD0_00	VREF	TXD0_04	VDDO	VDDP	DGND	DGND	DGND
M	RXD0_01	RXD0_02	RXD0_00	RX_CLK0_0	TXD0_02	DVDD	VREF	DVDD	DGND	DGND	DGND
N	RXD0_04	RXD0_03	RXC0_4	RXD0_11	RXD0_09	VDDQ0	VDDP	DGND	DGND	DGND	DGND
P	RXD0_06	RXD0_05	RXC0_1	RXD0_14	RX_CLK0_1	VDDM0	DVDD	DGND	DGND	DGND	DGND
R	RXD0_07	RXD0_08	RXD0_13	RXD0_18	RXD0_19	RXD0_21	VREF	AGND	GPI4	DGND	DGND
T	RXC0_0	RXD0_15	RXC0_5	RXD0_23	RXD0_27	RXD0_24	AGND	AGND	AGND	AGND	AGND
U	RXD0_10	RXD0_20	RXC0_2	RXD0_26	RXD0_29	AGND	AGND	GPO4	AVDD	REFCLKP0	AGND
V	RXD0_12	RX_CLK0_2	RXD0_28	MDC0	AGND	AGND	AGND	GPO2	AGND	REFCLKN0	AVDD
W	RXD0_16	RXD0_22	RXD0_30	AGND	RDP1_0	AGND	RDP3_0	AGND	TDP2_0	AGND	TDP0_0
Y	RXD0_17	RX_CLK0_3	RXD0_31	AVDD	RDN1_0	AVDD	RDN3_0	AVDD	TDN2_0	AVDD	TDN0_0
AA	RXC0_6	RXC0_3	MDIO0	RDP0_0	AGND	RDP2_0	AGND	TDP3_0	AGND	TDP1_0	AGND
AB	RXD0_25	RXC0_7	MDEN0	RDN0_0	AVDD	RDN2_0	AVDD	TDN3_0	AVDD	TDN1_0	AVDD

Figure 30. Device Pinout Diagram (Part 1) (Top View)

	12	13	14	15	16	17	18	19	20	21	22
A	VDDP	VDDO	DVDD	VDDQ1	VREF	VDDP	VDDO	DVDD	VDDQ1	VREF	DVDD
B	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	RXD1_01	DGND
C	RX_CLK1_3	DGND	DGND	DGND	DGND	RXD1_22	RXD1_16	RXD1_13	RXD1_10	RXC1_0	TXD1_03
D	RXD1_31	RXD1_30	RXD1_27	RXD1_28	RXD1_26	RXD1_25	RXD1_23	RXD1_17	RXC1_1	RXD1_07	TXD1_05
E	DGND	DGND	REFINEN0	REFINEN1	DVDD	RXD1_29	RXD1_19	RX_CLK1_2	RXC1_5	RXD1_06	TXD1_06
F	VREF	VDD0	MDEN1	MDIO1	MDC1	DGND	RXC1_2	RXC1_6	RXD1_12	RXD1_02	TXC1_4
G	VDDP	VDDO	VREF	VDDO	VDDP	VDDQ1	RXD1_20	RXD1_18	RXD1_15	RXD1_05	TXD1_04
H	DVDD	DVDD	DVDD	DVDD	VDDO	VDDQ1	RXD1_21	RXD1_11	RXD1_08	RXD1_03	TXC1_0
J	DVDD	DVDD	DVDD	DVDD	VDDP	VREF3	RX_CLK1_1	RXD1_14	RXD1_04	TXD1_01	TXD1_09
K	DGND	DGND	DGND	DVDD	DGND	VDDQ1	RXD1_09	RXC1_4	RX_CLK1_0	TX_CLK1_0	TXD1_11
L	DGND	DGND	DGND	VDDP	VDDO	VDDP	REFSEL	RXD1_00	TXD1_07	TXD1_08	TXD1_12
M	DGND	DGND	DGND	DVDD	DGND	VREF	TXD1_00	TXD1_02	TX_CLK1_1	TXD1_15	TXC1_1
N	DGND	DGND	DGND	DGND	VDDP	VREF	TXD1_10	TXD1_14	TXD1_13	TXC1_5	TXD1_20
P	DGND	DGND	DGND	DGND	VDDM1	VREF4	TXD1_16	TXD1_17	TXD1_18	TXD1_19	TX_CLK1_2
R	DGND	DGND	GPI3	AGND	VDDP	GPI0	TXD1_25	TXD1_22	TXD1_21	TXD1_23	TXC1_2
T	AGND	AGND	AGND	AGND	AGND	AGND	TXD1_28	TXD1_26	TXD1_27	TXD1_24	TXC1_6
U	AGND	AGND	GPO3	AGND	REFCLKP1	AVDD	TMS	TXD1_29	TX_CLK1_3	TXD1_30	TXD1_31
V	AGND	AGND	GPO1	AGND	REFCLKN1	AGND	AGND	TDI	GPO0	TXLED0	TXC1_3
W	AGND	RDP1_1	AGND	RDP3_1	AGND	TDP2_1	AGND	TDP0_1	TDO	RXLED1	TXC1_7
Y	AVDD	RDN1_1	AVDD	RDN3_1	AVDD	TDN2_1	AVDD	TDN0_1	TCK	PLL_LOCK1	RXLED0
AA	RDP0_1	AGND	RDP2_1	AGND	TDP3_1	AGND	TDP1_1	AGND	VDDP	LINKLED1	TXLED1
AB	RDN0_1	AVDD	RDN2_1	AVDD	TDN3_1	AVDD	TDN1_1	AVDD	TRST_N	LINKLED0	PLL_LOCK0

Figure 31. Device Pinout Diagram (Part 2) (Top View)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
	Supply voltage(2)	DVDD, AVDD, VTT, VREF	-0.3 to 1.5	V
		VDDQ	-0.3 to 1.6	
		VDDP, VDDO, VDDM	-0.3 to 3	
V_I	Input Voltage	LVCMOS	-0.3 to Supply 3	
		HSTL CLASS 1	-0.3 to 2	
	Storage temperature		-65 to 150	°C
	Electrostatic Discharge	HBM	2	KV
		CDM	500	V
	Characterized free-air operating temperature range		0 to 70	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
DVDD	Core Supply Voltage		1.14	1.2	1.26	V
AVDD	Analog Supply Voltage		1.14	1.2	1.26	
VDDQ1/0	Parallel HSTL I/O Supply Votage (1.5V Application)		1.4	1.5	1.6	
VDDP VDDO	LVCMOS I/O Supply Voltage		2.38	2.5	2.63	
VDDM1	Port 1 MDIO I/O Supply Voltage (2.5V Application)		2.38	2.5	2.63	
VDDM0	Port 0 MDIO I/O Supply Voltage (2.5V Application)		2.38	2.5	2.63	
VDDM1	Port 1 MDIO I/O Supply Voltage (1.2V Application)		1.14	1.2	1.26	
VDDM0	Port 0 MDIO I/O Supply Voltage (1.2V Application)		1.14	1.2	1.26	
VTT 1/0 VREF1/0	HSTL bias supply voltage (1.5V Application) VDDQ1/0 Divided By Two		0.7	0.75	0.8	
I_{DVDD}	Digital Core Supply Current	R_ω = 156.25MHz (DVDD = 1.26V)			815	mA
$I_{VDDM/P/O}$	LVCMOS I/O Supply Current	R_ω = 156.25MHz (VDDP/VDDO = 2.625V)			195	
I_{VDDQ}	HSTL I/O Supply Current	R_ω = 156.25MHz (VDDQ = 1.6V)			450	
I_{AVDD}	Analog Supply Current	R_ω = 156.25MHz (AVDD = 1.26V)			740	
P_D	Total power consumption 1.5V HSTL I/O Mode	HSTL Input Terminations Disabled		2.42	3.22	W
		HSTL Input Terminations Enabled		2.72	3.63	
Isda	Analog Shutdown Current			500		µA
Isdd	Core Shutdown Current			11		mA

REFERENCE CLOCK TIMING REQUIREMENTS (REFCLKP/N)(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	Normal	156.25	156.25	156.25	MHz
Accuracy	Relative to Nominal	–100	0	100	ppm
Accuracy	Independent Channel Mode	0	0	0	
Duty Cycle		45%	50%	55%	
Jitter	Random and deterministic			40	ps

(1) This clock should be crystal referenced to meet the requirements of the above table.

REFERENCE CLOCK ELECTRICAL CHARACTERISTICS (REFCLKP/N)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{id}	Differential input voltage		100		2000	mV_{PP}
C_{IN}	Input capacitance				3	pF
R_{IN}	Input differential impedance		80	100	120	Ω
T_{rise}	Rise time	20% to 80%	50		600	ps

LVCMOS ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –100 µA, Driver Enabled	VDDP/ VDDO–0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 100 µA, Driver Enabled			0.2	
V_{IH}	High-level input voltage		0.7 × VDDP/ VDDO			
V_{IL}	Low-level input voltage		0		0.3 × VDDP/ VDDO	
I_H, I_L	Low/High input current				±1	µA
I_Z	Low input current	Driver Only, driver disabled			±20	
C_{IN}	Input capacitance				5	pF

MDIO ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	VDDM = 2.5V	2.1		VDDM+ 0.3	V
V_{IL}	Low-level input voltage	VDDM = 2.5V	0		0.8	
V_{IH}	High-level input voltage	VDDM = 1.2V	1		VDDM+ 0.3	
V_{IL}	Low-level input voltage	VDDM = 1.2V	0		0.36	
V_{OL}	Low-level output voltage	VDDM = 2.5V	0		0.4	
V_{OL}	Low=level output voltage	VDDM = 1.2V	0		0.2	
V_{OH}	High-level output voltage	VDDM = 1.2/2.5V (Open Drain Driver) Pulled up on the customer board				
I_H, I_L	Low/high input current				±1	µA
I_Z	Low input current	Driver only, driver disabled			±20	µA
C_{IN}	Input capacitance				5	pF

HSTL SIGNALS (VDDQ1/0 = 1.5 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(dc)}$	High-level output voltage		VDDQ–0.4		VDDQ	V
$V_{OL(dc)}$	Low-level output voltage				0.4	
$V_{OH(ac)}$	High-level output voltage		VDDQ–0.5		VDDQ	
$V_{OL(ac)}$	Low-level output voltage				0.5	
$V_{IH(dc)}$	High-level DC input voltage	DC input, logic high	VREF + 0.1		VDDQ + 0.3	
$V_{IL(dc)}$	Low-level DC input voltage	DC input, logic low	–0.3		VREF –0.1	
$V_{IH(ac)}$	High-level AC input voltage	AC input, logic high	VREF + 0.2			
$V_{IL(ac)}$	Low-level AC input voltage	AC input, logic low			VREF – 0.2	
$I_{OH(dc)}$	High output current		-8			mA
$I_{OL(dc)}$	Low output current		8			
C_{IN}	Input Capacitance				4	pF

SERIAL TRANSMITTER/RECEIVER CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(pp)}$	TX output differential peak-to-peak voltage swing	Maximum pre-emphasis Enabled - Emphasized Bit See Figure 32, 4/5.32900.14:11 = 1000 (Binary)	1100	1280	1450	mV_{PP}
$V_{OD(pd)}$		Maximum Pre-emphasis Enabled- De-emphasized Bit, See Figure 32 4/5.32900.14:11 = 1000 (Binary)	650	760	875	
$V_{OD(pp)}$		Pre-emphasis disabled 4/5.32900.14:11 = 0000 (Binary)	1250	1400	1575	
I_{LKG}	RX input leakage current		–10		10	µA
C_I	RX input capacitance				2	pF
t_r, t_f	Differential output signal rise, fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, See Figure 32	80		160	ps
J_{TOL}	Jitter Tolerance, Total Jitter at Serial Input	Zero crossing, See Figure 35			0.6	UI(1)
J_{DR}	Serial Input Deterministic Jitter	Zero crossing, See Figure 35			0.36	
J_T	Serial Output Total Jitter	PRBS at 3.125 GHz, See Figure 35		0.20	0.35	
J_D	Serial Output Deterministic Jitter	PRBS at 3.125 GHz, See Figure 35			0.17	
$R_{(LATENCY)}$	Total delay from RX input to RD output	See Figure 15			950	Bit Times
$T_{(LATENCY)}$	Total delay from TD input to TX output	See Figure 14			650	

(1) Unit Interval = 0ne serial bit time (min 320 ps)

Table 86. Driver Template Parameters

PARAMETER	NEAR END VALUE	FAR END VALUE	UNIT
X1 (See Figure 33)	0.175	0.275	UI
X2 (See Figure 33)	0.390	0.400	
A1 (See Figure 33)	400	100	mV
A2 (See Figure 33)	800	800	

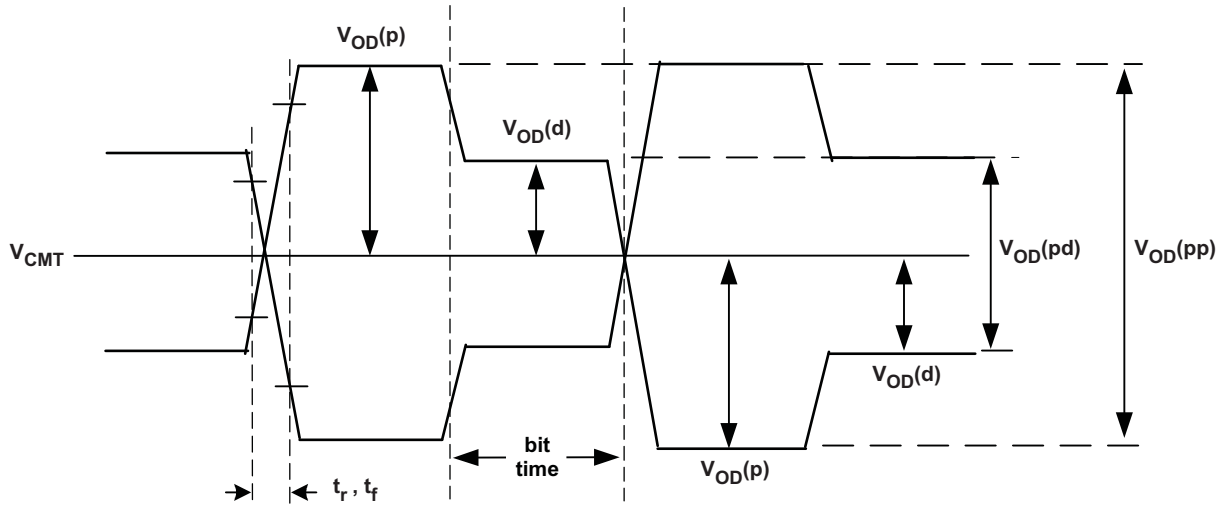


Figure 32. Transmit Output Waveform Parameter Definitions

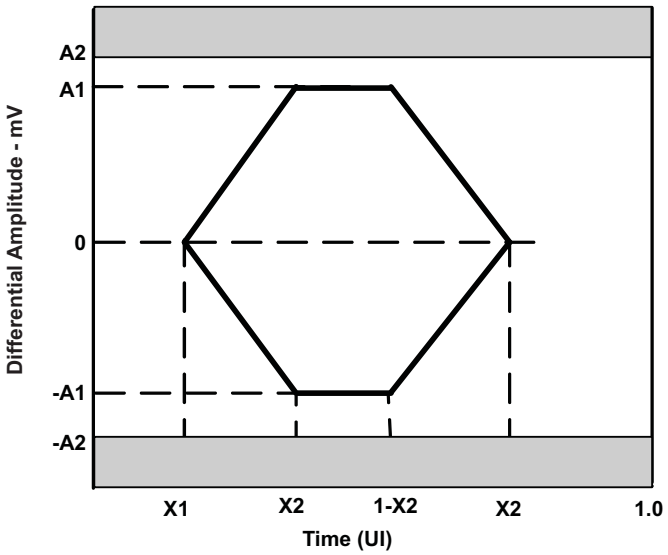


Figure 33. Transmit Template

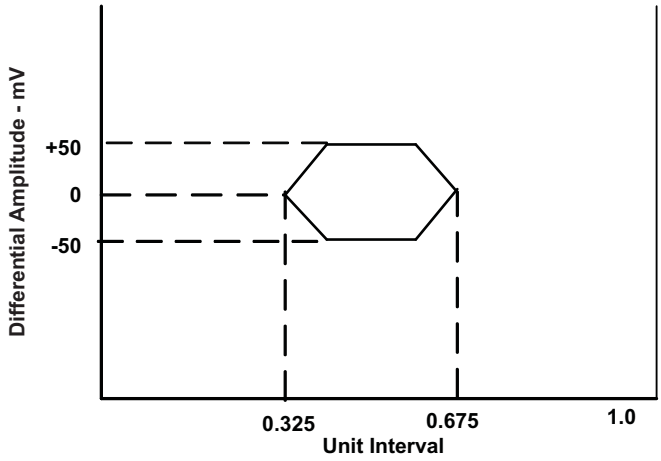
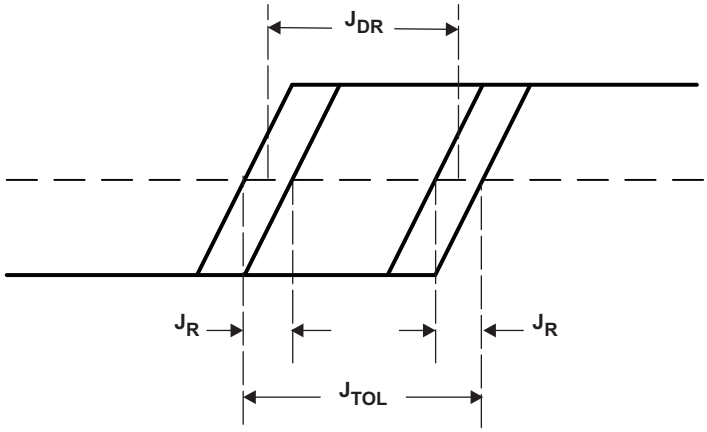


Figure 34. Receive Template



NOTE: $J_{TOL} = J_R + J_{DR}$, where J_{TOL} is the receive jitter tolerance, J_{DR} is the received deterministic jitter, and J_R is the Gaussian random edge jitter distribution at a maximum BER = 10^{-12}.

Figure 35. Input Jitter

HSTL OUTPUT SWITCHING CHARACTERISTICS (DDR)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{setup}	RXD0/1_[31:0], RXC0/1_[7:0]setup prior to RX_CLK transition high or low	See Figure 36	960	960	960	ps
t_{hold}	RXD0/1_[31:0], RXC0/1_[7:0] hold after RX_CLK transition high or low	See Figure 36	960	960	960	
T_{duty}	RX_CLK_0/1_[3:0] Duty Cycle	Source Centered and Source Aligned	40%		60%	
t_{period}	RX_CLK_0/1_[3:0] Period	Source Centered and Source Aligned		6.25		ns
T_{pd}	RX_CLK_0/1_[3:0] rising or falling to RXD0/1_[31:0], RXC0/1_[7:0] valid	See Figure 37	–640		640	ps

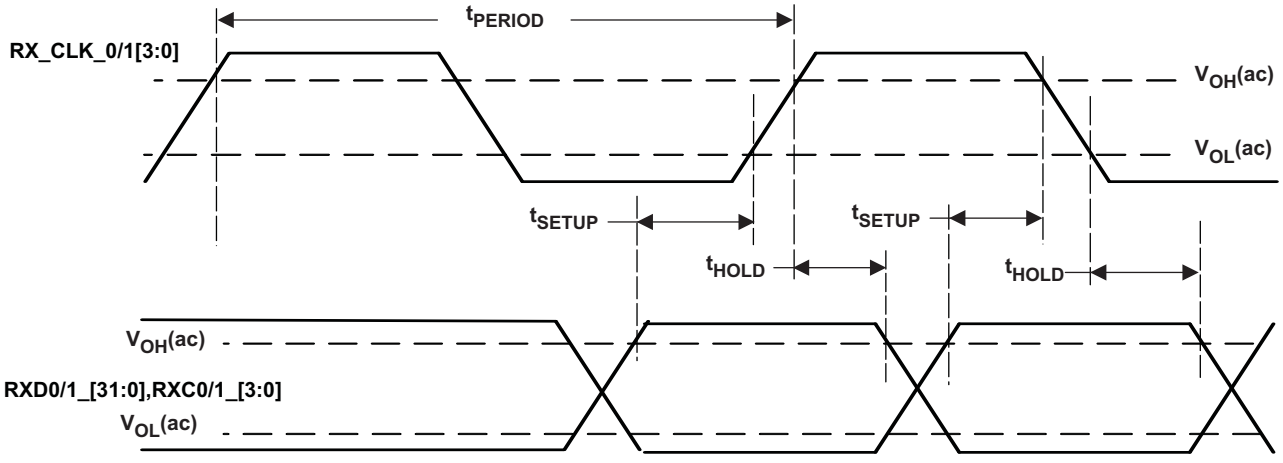


Figure 36. HSTL (DDR Mode) Source Centered Output Timing Requirements

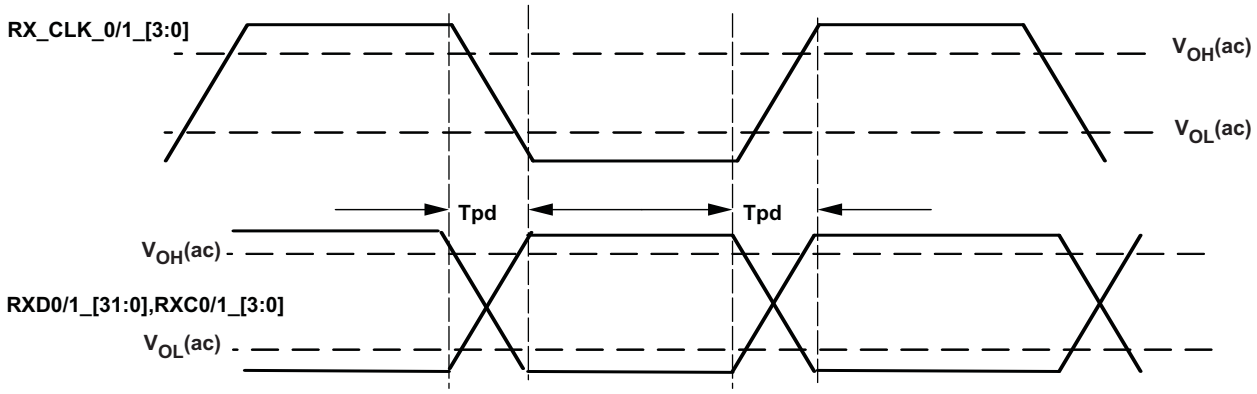


Figure 37. HSTL (DDR Mode) Source Aligned Output Timing Requirements

HSTL (DDR MODE) INPUT TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{setup}	TXD0/1_[31:0], TXC0/1_[3:0] setup prior to TX_CLK_0/1_[3:0] transition high or low	See Figure 38	480	480	480	ps
t_{hold}	TXD0/1_[31:0], TXC0/1_[3:0] hold after TX_CLK_0/1_[3:0] transition high or low	See Figure 38	480	480	480	
T_{duty}	TX_CLK_0/1_[3:0] Duty Cycle		40%		60%	
t_{period}	TX_CLK_0/1_[3:0] Period	156.25 Mhz ±100 ppm		6.25		ns

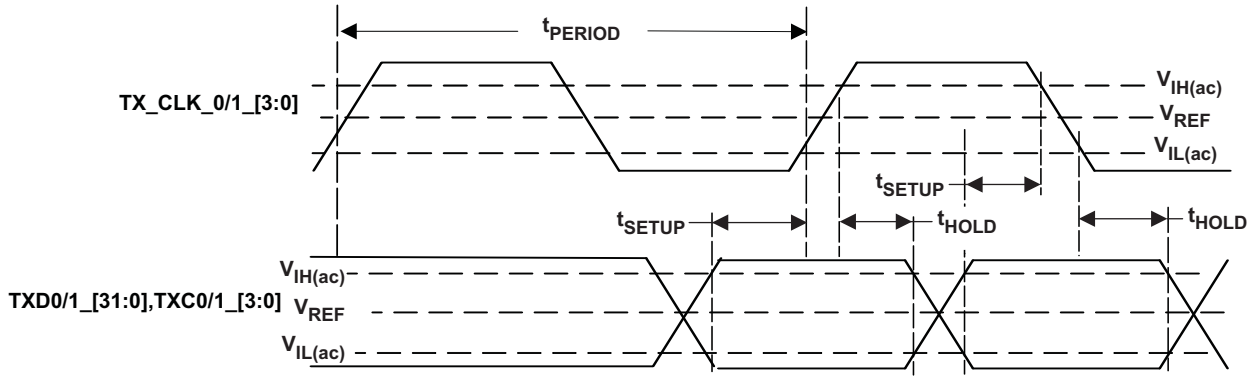


Figure 38. HSTL (DDR Mode) Data Input Timing Requirements

MDIO TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{period}	MDC0/1 period	See Figure 39	100			nS
t_{setup}	MDIO0/1 setup to ↑ MDC0/1	See Figure 39	10			
t_{hold}	MDIO0/1 hold to ↑ MDC0/1	See Figure 39	10			
T_{valid}	MDIO0/1 valid from MDC ↑		0		300	

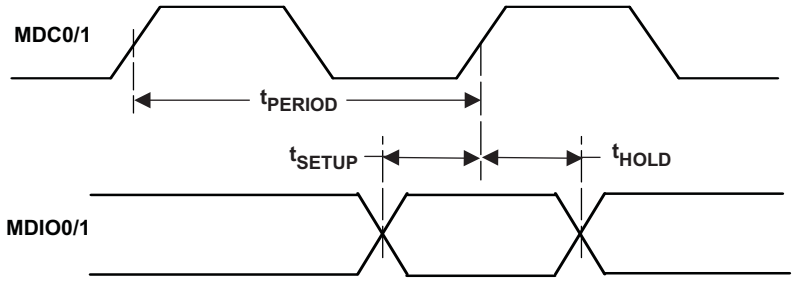


Figure 39. MDIO Read/Write Timing

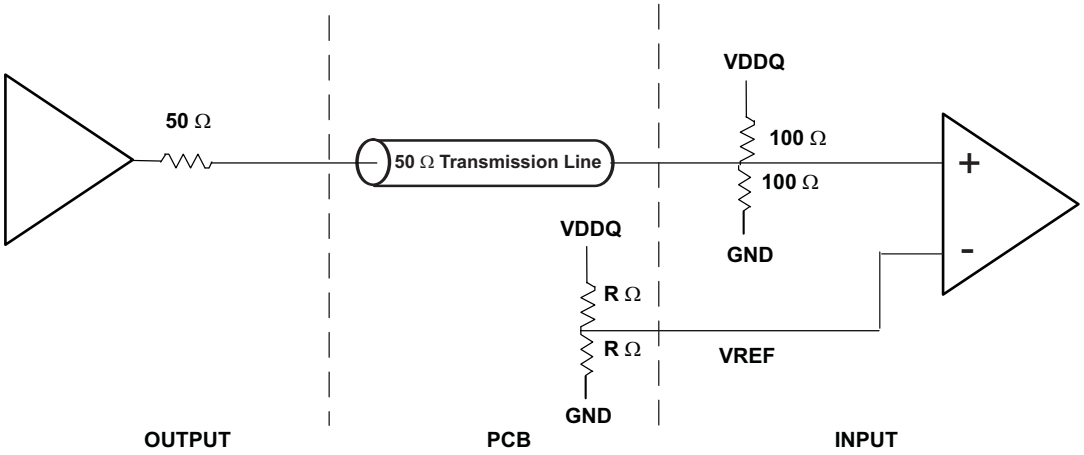


Figure 40. HSTL I/O Schematic

Table 87. Device Thermal Characteristics

PACKAGE THERMAL THETA VALUES			
	Airflow (ft/min)	**Value**	**Unit**
θ_{JA}	0	14.11	(°C/W)
	100	12.66	
	250	11.60	
	400	11.04	
	600	10.56	
θ_{JB}	5.42		
θ_{JC}	2.63		
θ_{JL}	3.57		
Device Maximum Characteristics			
Maximum Junction Temperature	115		°C
Maximum Power Dissipation	3.63		Watts

DEVICE TEST MODE

Table 88 shows how testability pins are muxed with device pins. This is for TI only, and may be ignored by external users of this device.

Table 88. Device Test Mode Pin Configuration

Functional Device Pin Name	Functional Mode Signal Direction	Test Mode Signal Direction	Functional Mode/JTAG Testing	Scan Mode/RedJinn Canned TDL	MEMBIST/ Efuse Mode	Low Speed SERDES Diagnostics
GPI[4]	I	I	0	O	1	1
GPI[0]	I	I	0	1	0	1
PLL_LOCK1	O	O	—	Scan Out 0	Efuse Data Out	Test Failure Out 0
PLL_LOCK0	O	O	—	Scan Out 1		Test Failure Out 1
LINKLED1	O	O	—	Scan Out 2		Test Failure Out 2
LINKLED0	O	O	—	Scan Out 3		Test Failure Out 3
TXLED1	O	O	—	Scan Out 4		Test Failure Out 4
TXLED0	B	I/O	—	Scan Enable		Test Failure Out 5
RXLED1	O	O	—	Scan Out 5		Test Failure Out 6
RXLED0	O	O	—	Burnin Output	Burnin Output (MBIST)	Test Failure Out 7
REFINEN1	I	I	—	Scan Config 0	Debug HS Clock(1)	—
REFINEN0	I	I	—	Scan Config 1	RAM Clock Bypass(1)	—
PRTAD0	I	I	—	Scan Clock	MBIST Enable	—
PRTAD1	I	I	—	Scan In 0	Efuse CTL MODE	—
PRTAD2	I	I	—	Scan In 1	Efuse Clock	—
PRTAD3	I	I	—	Scan In 2	Efuse Data In	—
PRTAD4	I	I	—	Scan In 3	MBIST Resume(2)	—
XGMII0_ST	I	I	—	Scan In 4	MBIST Hold(3)	—
MDIO0_ST	I	I	—	Scan In 5	MBIST Debug(1)	—
MDEN1	I	I	—	Scan In 6	—	—
MDMX	I	I		TESTCLK T	—	TESTCLK T
REFSEL	I	I	—	TESTCLK R	—	TESTCLK R
GPI[3]	I	I	IDDQ	IDDQ	IDDQ	IDDQ
GPO[5]	O	O	MBIST Start Retention	MBIST Start Retention	MBIST Start Retention	MBIST Start Retention
GPO[4]	O	O	MBIST Fail	MBIST Fail	MBIST Fail	MBIST Fail
GPO[3]	O	O	MBIST Done	MBIST Done	MBIST Done	MBIST Done
GPO[2]	O	O	MBIST Diag Scan Out	MBIST Diag Scan Out	MBIST Diag Scan Out	MBIST Diag Scan Out
GPO[1]	O	O	MBIST Restart	MBIST Restart	MBIST Restart	MBIST Restart
GPO[0]	O	O	LOW	Scan Out 6	LOW	LOW
TCK(4)	I	I	TCK	TCK	MBIST Diag Clock	TCK

(1) This signal is internally connected to LOW (unasserted) when not available at external pins.
(2) This signal is internally connected to HIGH (asserted) when not available at external pins.
(3) This signal is internally connected to HIGH (unasserted) when not available at external pins.
(4) TCK is not a muxed test pin. TCK is used as MBIST diagnostic clock but still retains its functionality.

Table 89. MEMBIST Control

DEVICE MODE	MDIO(1)	JTAG(1)	PIN(1)
Functional Mode	Yes	Yes	No
Scan Mode	No	No	No
MEMBIST/Efuse Mode	No	No	Yes
Serdes Diagnostic Mode	Yes	Yes	No

(1) **Yes**– this control is enabled, **No**– this control is disabled

Procedures for Testing Memory BIST

TLK3138 supports Memory BIST (MBIST) execution through JTAG, PIN and MDIO controls. In all 3 modes MBIST_DONE and MBIST_FAIL_L signals are broadcast on to the pins GPO5 and GPO4 respectively. When MBIST is disabled (MBIST_EN = 0), both MBIST_DONE and MBIST_FAIL_L report LOW value. Before any MBIST testing the user must execute a hardware reset through the RST_N pin. This reset must be held asserted for at least 10µs.

MBIST Through JTAG

MBIST execution through JTAG allows the user to test the Memory cells inside TLK3138 without accessing many pins on the device. In addition to JTAG related pins, only REFCLK and RST_N pins need to be controlled to test the MBIST. MBIST execution is enabled through the *ti_mbist_en* instruction, and status is checked via the *ti_mbist_status* instruction. REFCLK acts as a source clock for the at-speed MBIST execution. The user has to provide a 156.25 MHz clock through REFCLK pins in order to execute MBIST. The following paragraphs explain each MBIST JTAG instruction in detail:

ti_mbist_en: This JTAG instruction with op code 4'b1100 allows the user to control the internal MBIST_EN signal. Once the instruction is completed MBIST_EN assumes the TDI value during the update-dr state of instruction. When MBIST_EN is set to HIGH, MBIST execution starts. Once the test is completed and the status signals are checked, the ti_mbist_en instruction can be reissued with TDI set to a logic LOW value and MBIST_EN assumes a logic LOW value.

ti_mbist_status: This JTAG instruction with op code 4'b1101 allows the user to check the status of the internal MBIST_DONE and MBIST_FAIL_L signals. Once MBIST_EN is set to HIGH, the status of the MBIST_DONE signal should be checked for a logic HIGH value, which indicates completion of the test and MBIST_FAIL_L signal should be checked for a logic HIGH value, which indicates MBIST execution completed without any errors. The MBIST_FAIL_L signal is LOW true (i.e if MBIST_FAIL_L is LOW, then it indicates that the MBIST execution completed with errors). The MBIST_DONE and MBIST_FAIL_L status signals are captured and scanned out through TDO at the next 2 TCK cycles respectively after entering into capture_dr state. When MBIST is disabled (MBIST_EN = 0), both MBIST_DONE and MBIST_FAIL_L reports logic LOW values.

MBIST Through MDIO

MBIST can be tested through MDIO by following MDIO instructions.

- Write 1'b1 to bit 11 of BIST_CONTROL register (0x80A0) to enable MBIST test.
- Read MBIST_DONE status by reading bit 14 of BIST_STATUS register (0x80A1). If the MBIST test is finished then this bit reads HIGH. Once MBIST_DONE is reported HIGH, read MBIST_FAIL_L status by reading bit 15 of BIST_STATUS register (0x80A1). If MBIST test completes without any errors this bit reads HIGH. If any errors are encountered during MBIST tests this bit reads back LOW.

Repeat MBIST Testing

In order to run repeat MBIST tests the device requires a software initiated or hardware reset to clear the MBIST_DONE signal between executions.

For powering down individual blocks and the I/O buffers based on the mode pins (GPI[4], GPI[0]) and the IDDQ mode, the following truth table applies.

Table 90. Power Down Scheme

IDDQ	GPI[4]	GPI[0]	Software Power Down	Operational Mode
0	0	0	0	***Normal functional mode.*** All IO buffers are powered all clocks are enabled.
X	0	0	1	***Software initiated powerdown.*** All IO buffers that can be disabled or powered down are disabled/powered down. All clocks are disabled. REDJINN transmit and receive macros and the REDJINN PLL are disabled.
1	0	0	X	***IDDQ pin initiated powerdown.*** All I/O buffers that can be disabled or powered down are disabled/powered down. All clocks are disabled. REDJINN transmit and receive macros and the REDJINN PLL are disabled.
X	1	1	X	***Serdes Test Mode.*** All IO buffers are powered all clocks are enabled.
X	1	0	X	***EFUSE mode.*** All IO buffers are powered, all clocks are enabled.
0	0	1	X	***Normal Scan test mode.*** All IO buffers are powered all clocks are enabled.
1	0	1	X	***IDDQ Scan test mode.*** All non scan IO buffers that can be disabled or powered down are disabled/powered down. All clocks are enabled

MDIO CHANGES

Following are the changes in MDIO programmer's reference.

	REGISTER ADRESS	BIT(s)	CHANGE
1	0x8026	11	Added XGMII Rx Source centered/aligned control bit
2	0x8085	7:6	Added ENTEST bits
3	0x808B	5	Added XGMII 0 3-state control bit. Bit 0 for XGMII 0 Tristate control
4	0x808B	7	Added XGMII Redundancy mode control bit
5	0x808B	9/8	Added HSTL_TERMINATION_EN control bits
6	0x808D		All Removed Composite status bits
7	0x809(8-A)		All Removed VTP Control registers
8	0x8084	6	Default changed to 1. Ext reference VREF is used to set output amplitude
9	0x808B	15:10	Added SERDES external voltage divider control bits.
10	0x80A0	11	Added BIST control bits
11	0x80A1	15:14	Added BIST status bits
12	0x80A2	15	Added Reserved bit.

JTAG LIMITATION

RST_N must be asserted (and released if desired) before executing JTAG instructions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLK3138ZDU	ACTIVE	BGA	ZDU	484	60	Pb-Free (RoHS)	SNAGCU	Level-4-260C-72 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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