

TLP759

Digital Logic Ground Isolation
 Line Receiver
 Microprocessor System Interfaces
 Switching Power Supply Feedback Control
 Industrial Inverter

The TOSHIBA TLP759 consists of a high-output infrared emitting diode and a high speed detector of one chip photo diode-transistor. This unit is 8-lead DIP.

TLP759 has no internal base connection, and a Faraday shield integrated on the photodetector chip provides an effective common mode noise transient immunity.

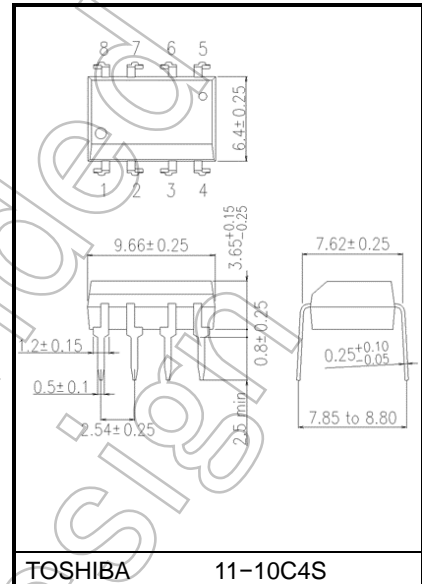
So this is suitable for application in noisy environmental condition.

- Isolation voltage: 5000 Vrms (min)
- Switching speed: $t_{pHL} = 0.2\mu s$ (typ.)
 $t_{pLH} = 0.3\mu s$ (typ.) ($R_L=1.9 k\Omega$)
- TTL compatible
- UL-recognized: UL 1577, File No. E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
 File No.E67349
- VDE-approved: EN 60747-5-5 (Note 1)

Note 1: When a VDE approved type is needed, please designate the **Option (D4)**.

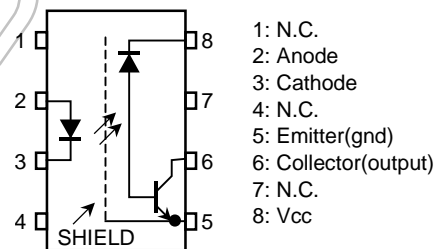
- Mechanical Parameters
 Creepage distance: 7.0 mm (min)
 Clearance: 7.0 mm (min)
 Insulation thickness: 0.4 mm (min)

Unit: mm

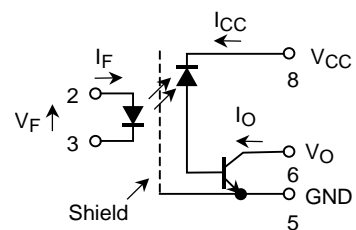


Weight: 0.54 g (typ.)

Pin Configuration (top view)



Schematic



Start of commercial production
 1993-01

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current	I _F	25	mA
	Forward current derating (Ta ≥70°C)	I _F / Ta	-0.8	mA / °C
	Pulse forward current (Note 1)	I _{FP}	50	mA
	Peak transient forward current (Note 2)	I _{FPT}	1	A
	Reverse voltage	V _R	5	V
	Diode power dissipation (Note 3)	P _D	45	mW
Detector	Output current	I _O	8	mA
	Peak output current	I _{OP}	16	mA
	Output voltage	V _O	-0.5 to 20	V
	Supply voltage	V _{CC}	-0.5 to 30	V
	Output power dissipation	P _O	100	mW
	Output power dissipation derating (Ta ≥70°C)	P _O / Ta	-2	mW / °C
Operating temperature range		T _{opr}	-55 to 100	°C
Storage temperature range		T _{stg}	-55 to 125	°C
Lead solder temperature (10 s) (Note 4)		T _{sol}	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60 %) (Note 5)		B _{Vs}	5000	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) 50 % duty cycle, 1 ms pulse width. Derate 1.6 mA / °C above 70 °C.

(Note 2) Pulse width ≤ 1 μs, 300 pps.

(Note 3) Derate 0.9 mW / °C above 70 °C.

(Note 4) Soldering portion of lead: Up to 2 mm from the body of the device.

(Note 5) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
LDE	Forward voltage	V_F	$I_F = 16 \text{ mA}$	—	1.65	1.85	V
	Forward voltage temperature coefficient	$\Delta V_F / \Delta T_a$	$I_F = 16 \text{ mA}$	—	-2	—	mV / °C
	Reverse current	I_R	$V_R = 5 \text{ V}$	—	—	10	μA
	Capacitance between terminals	C_T	$V = 0 \text{ V}, f = 1 \text{ MHz}$	—	45	—	pF
Detector	High level output current	$I_{OH(1)}$	$I_F = 0 \text{ mA}, V_{CC} = V_O = 5.5 \text{ V}$	—	3	500	nA
		$I_{OH(2)}$	$I_F = 0 \text{ mA}, V_{CC} = 30 \text{ V}, V_O = 20 \text{ V}$	—	—	5	μA
		I_{OH}	$I_F = 0 \text{ mA}, V_{CC} = 30 \text{ V}, V_O = 20 \text{ V}$ $T_a = 70 \text{ °C}$	—	—	50	
	High level supply voltage	I_{CCH}	$I_F = 0 \text{ mA}, V_{CC} = 30 \text{ V}$	—	0.01	1	μA
Coupled	Current transfer ratio	I_O / I_F	$I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}$ $V_O = 0.4 \text{ V}$	20	40	—	%
	Low level output voltage	V_{OL}	$I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}$ $I_O = 2.4 \text{ mA}$	—	—	0.4	V
	Resistance (input-output)	R_S	$R.H. \leq 60 \%, V_S = 500 \text{ V}$ (Note 5)	1×10^{12}	10^{14}	—	Ω
	Capacitance (input-output)	C_S	$V_S = 0 \text{ V}, f = 1 \text{ MHz}$ (Note 5)	—	0.8	—	pF
	Isolation voltage	BVS	$AC, 60 \text{ s}$ (Note 5)	5000	—	—	Vrms

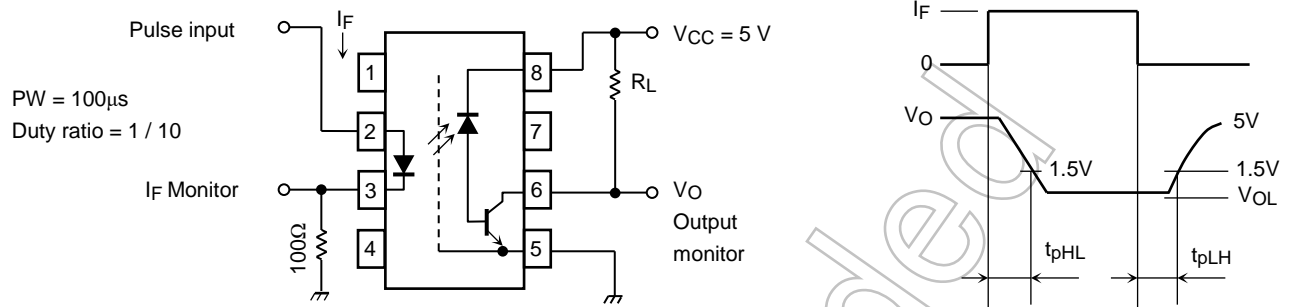
Switching Characteristics (Ta = 25°C, VCC = 5V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H → L)	t_{pHL}	1	$I_F = 0 \rightarrow 16 \text{ mA},$ $R_L = 1.9 \text{ k}\Omega$	—	0.2	0.8	μs
Propagation delay time (L → H)	t_{pLH}		$I_F = 16 \rightarrow 0 \text{ mA},$ $R_L = 1.9 \text{ k}\Omega$	—	0.3	0.8	μs
Common mode transient immunity at logic high output (Note 1)	CM_H	2	$I_F = 0 \text{ mA}, V_{CM} = 400 \text{ V}_{p-p}$ $R_L = 4.1 \text{ k}\Omega$	5000	10000	—	V / μs
Common mode transient immunity at logic low output (Note 1)	CM_L		$I_F = 16 \text{ mA}, V_{CM} = 400 \text{ V}_{p-p}$ $R_L = 4.1 \text{ k}\Omega$	-5000	-10000	—	V / μs

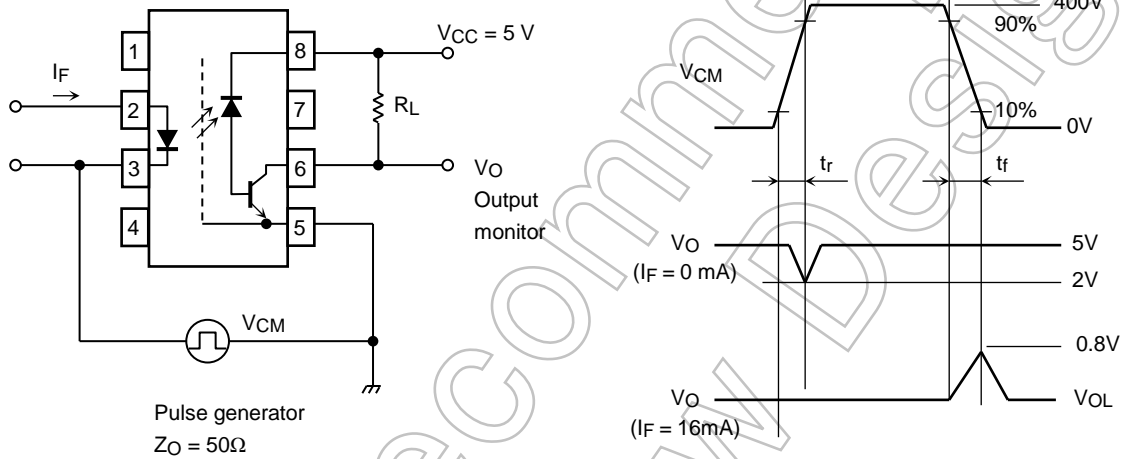
(Note 1) CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8 \text{ V}$).

CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0 \text{ V}$).

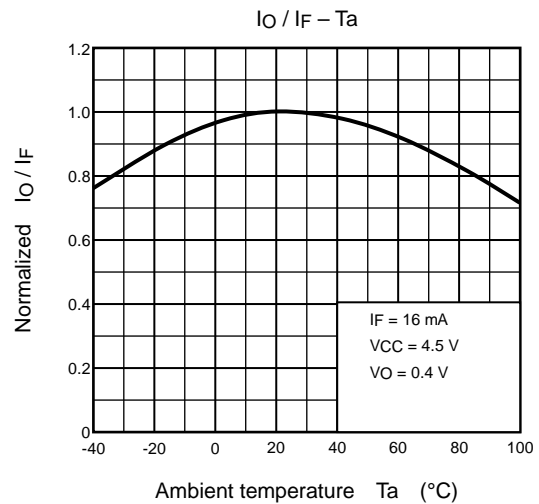
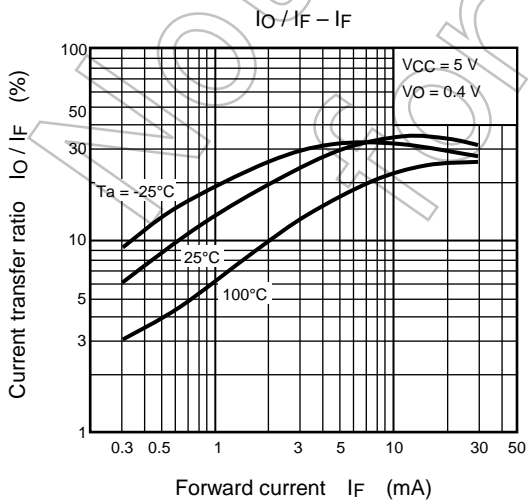
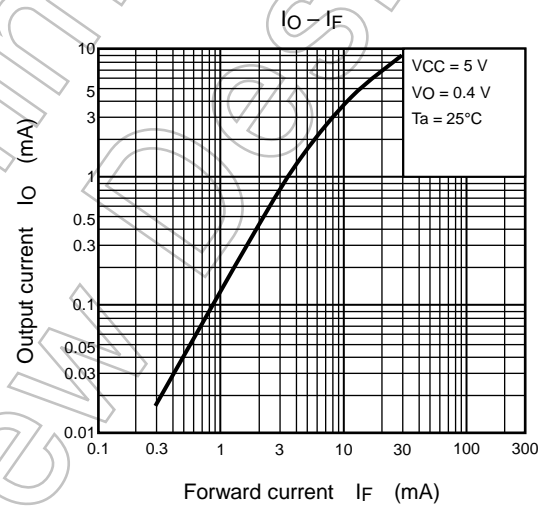
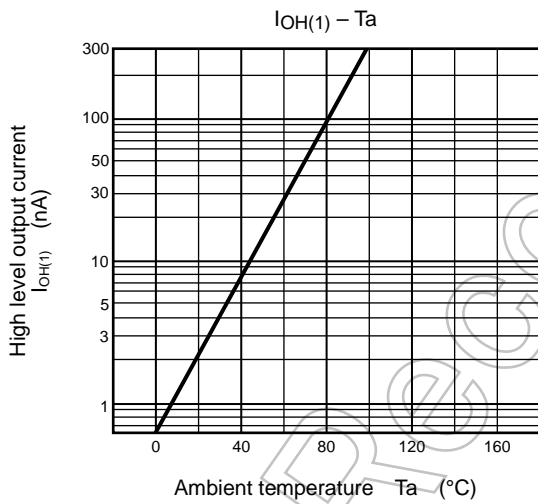
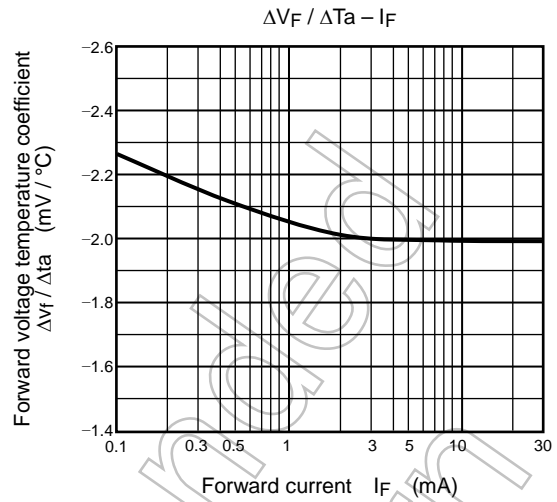
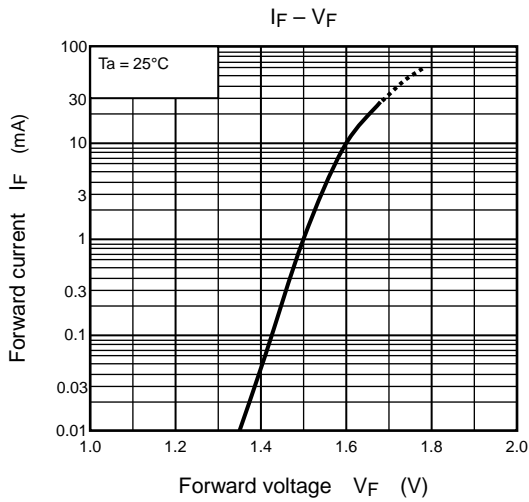
Test Circuit 1: Switching Time Test Circuit



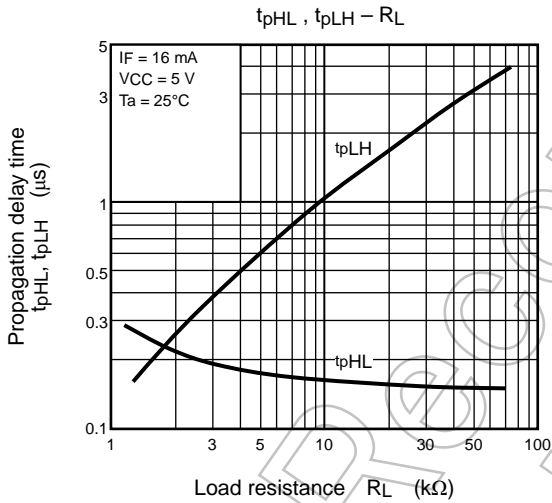
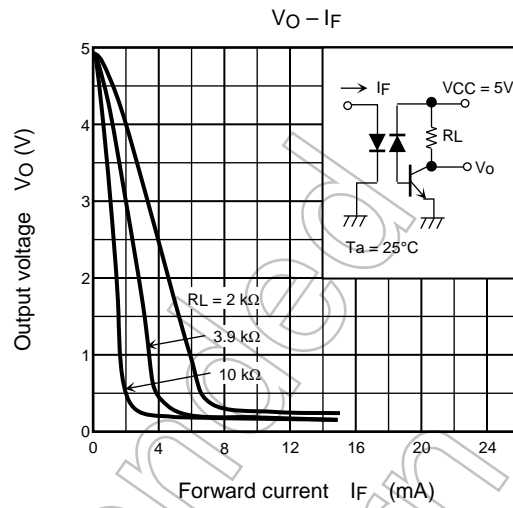
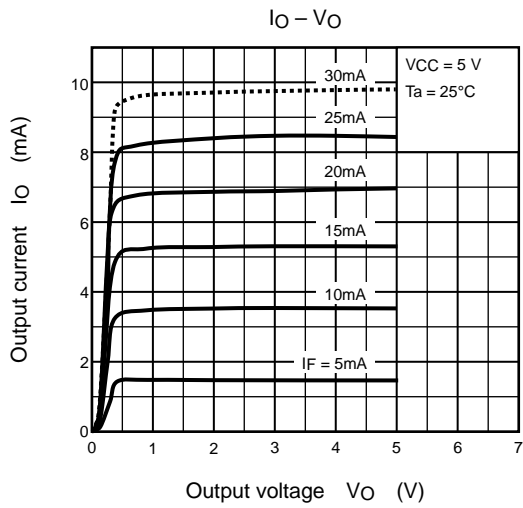
Test Circuit 2: Common Mode Noise Immunity Test Circuit



$$CM_H = \frac{320\text{ (V)}}{t_r\text{ (\mu s)}}, CM_L = \frac{320\text{ (V)}}{t_f\text{ (\mu s)}}$$



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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