Supertex inc.

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number /Package	
				TO-243AA*	Die†
18V	2.5Ω	250mA	1.0V	TN2501N8	TN2501ND

*Same as SOT-89. Product supplied on 2000 piece carrier tape reels.
†MIL visual screening available.

Product marking for TO-243AA:

TN5U✳

Where ✳ = 2-week alpha date code

Features

❏ Low threshold

❏ High input impedance

❏ Low input capacitance — 110pF max.

❏ Fast switching speeds

❏ Low on resistance

❏ Free from secondary breakdown

❏ Low input and output leakage

Applications

❏ Logic level interfaces – ideal for TTL and CMOS

❏ Solid state relays

❏ Battery operated systems

❏ Photo voltaic drives

❏ Analog switches

❏ General purpose line drivers

❏ Telecom switches
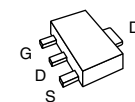
Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option

TO-243AA
(SOT-89)

Note: See Package Outline section for dimensions.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 15V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

11/12/01

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	400mA	560mA	1.6W†	15	78†	560mA	750mA

* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

| Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	18			V	$V_{GS} = 0V$, $I_D = 1.0mA$
$V_{GS(th)}$	Gate Threshold Voltage	0.3		1.0	V	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1.0mA$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 15V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{GS} = 0V$, V_{DS} = Max Rating
				1.0	mA	$V_{GS} = 0V$, $V_{DS} = 0.8$ Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	250	600		mA	$V_{GS} = V_{DS} = 3.0V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			25	Ω	$V_{GS} = 1.2V$, $I_D = 3.0mA$
				3.5		$V_{GS} = 2.0V$, $I_D = 50mA$
				2.5		$V_{GS} = 3.0V$, $I_D = 200mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	%/°C	$V_{GS} = 3.0V$, $I_D = 200mA$
G_{FS}	Forward Transconductance	0.15	0.3		℧	$V_{DS} = 3.0V$, $I_D = 200mA$
C_{ISS}	Input Capacitance			110	pF	$V_{GS} = 0V$, $V_{DS} = 15V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance			60		
C_{RSS}	Reverse Transfer Capacitance			35		
$t_{d(ON)}$	Turn-ON Delay Time			5.0	ns	$V_{DD} = 15V$, $I_D = 250mA$, $R_{GEN} = 25\Omega$
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			15		
t_f	Fall Time			8.0		
V_{SD}	Diode Forward Voltage Drop		1.1	1.8	V	$V_{GS} = 0V$, $I_{SD} = 200mA$
t_{rr}	Reverse Recovery Time		100		ns	$V_{GS} = 0V$, $I_{SD} = 200mA$

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μsec pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

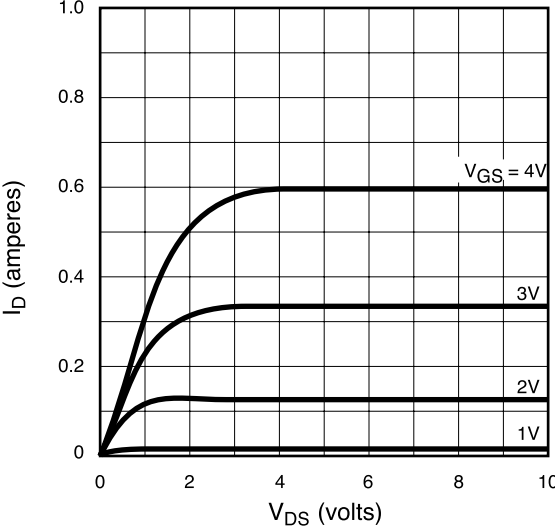## Switching Waveforms and Test Circuit
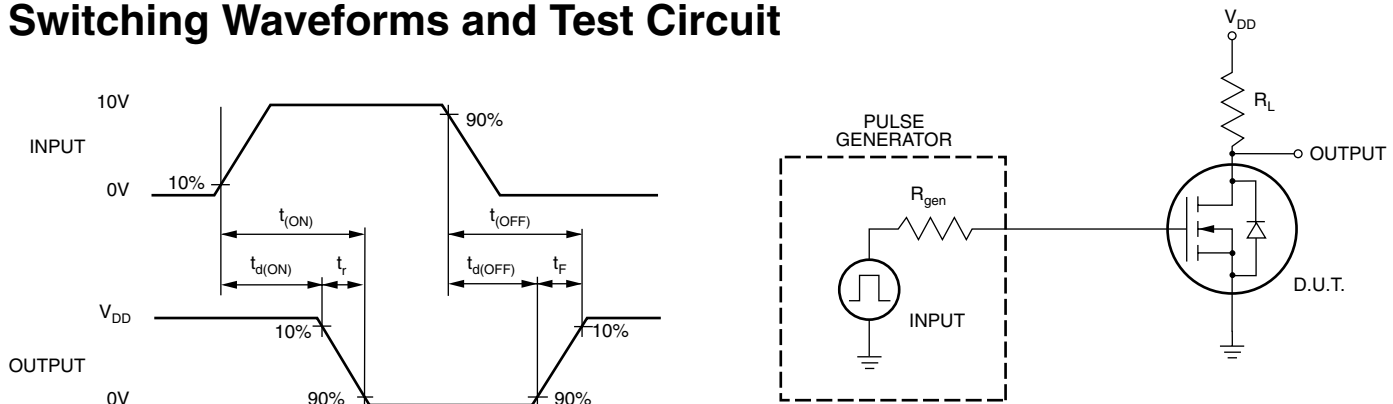
Typical Performance Curves
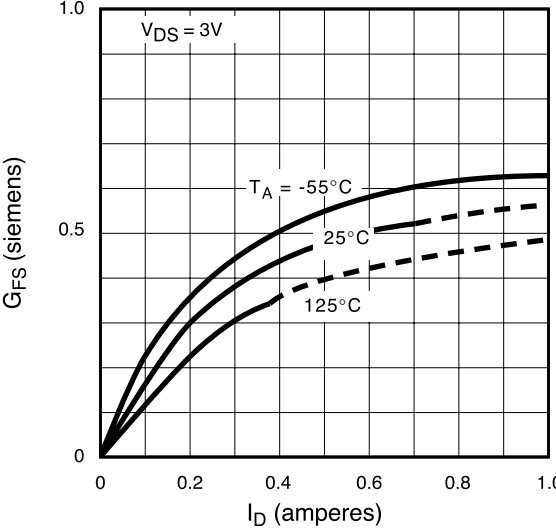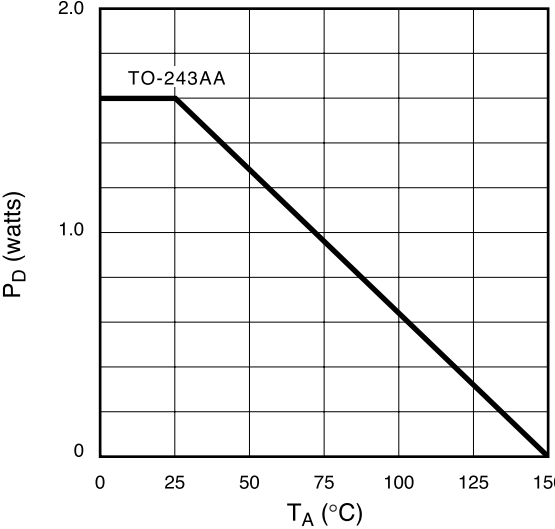
Output Characteristics
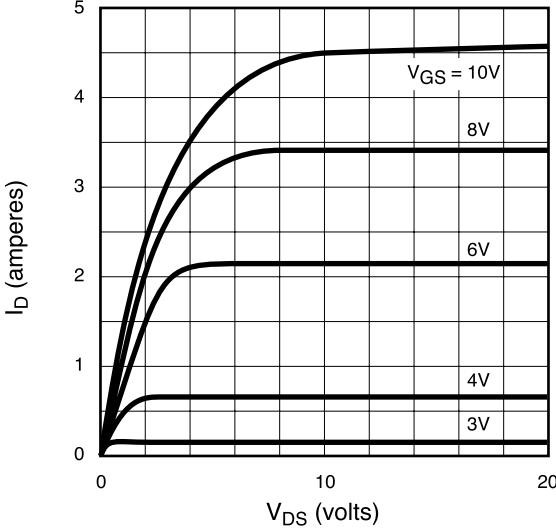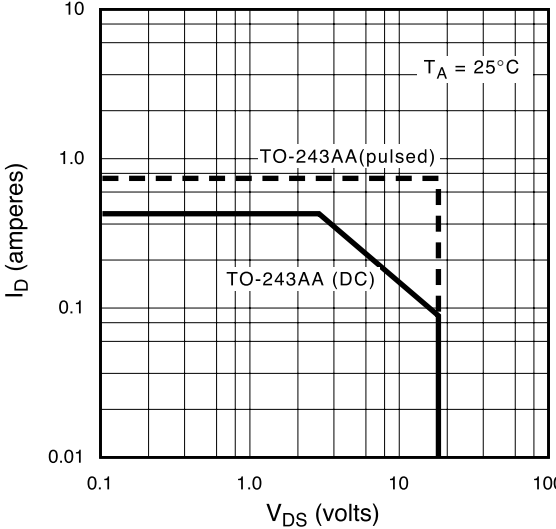

Saturation Characteristics

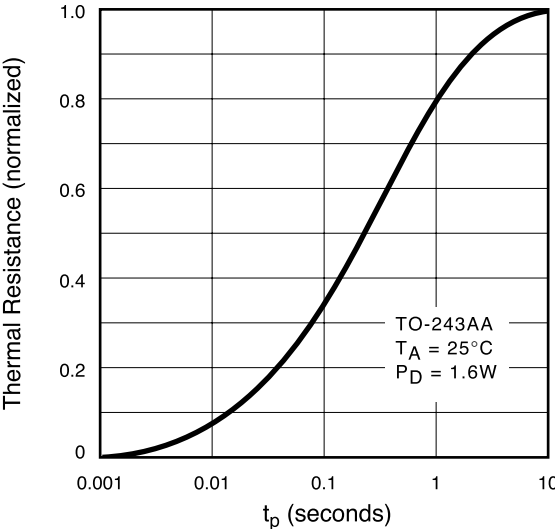### Transconductance vs. Drain Current

Power Dissipation vs. Ambient Temperature

Maximum Rated Safe Operating Area

Thermal Response Characteristics

3

Typical Performance Curves

BV_{DSS} Variation with Temperature

BV_{DSS} (normalized)

1.1
1.0
0.9

-50   0   50   100   150

T_j (°C)

On-Resistance vs. I_D

$R_{DS(ON)}$ (ohms)

10
8
6
4
2
0

$V_{GS} = 2V$

$V_{GS} = 3V$

0   0.2   0.4   0.6   0.8   1.0

I_D (amperes)

Transfer Characteristics

I_D (amperes)

1.0
0.8
0.6
0.4
0.2
0

$V_{DS} = 15V$

25°C

$T_A = -55°C$ 125°C

0   2   4   6   8   10

V_{GS} (volts)

$V_{(th)}$ and R_{DS} Variation with Temperature

$V_{GS(th)}$ (normalized)

1.4
1.2
1.0
0.8
0.6

$R_{DS(ON)}$ @ 3V, 0.2A

$V_{(th)}$ @ 1mA

$R_{DS(ON)}$ (normalized)

1.6
1.4
1.2
1.0
0.8
0.6

-50   0   50   100   150

T_j (°C)

Capacitance vs. Drain-to-Source Voltage

C (picofarads)

100
75
50
25
0

f = 1MHz

C_{ISS}
C_{OSS}
C_{RSS}

0   5   10   15   20

V_{DS} (volts)

Gate Drive Dynamic Characteristics

V_{GS} (volts)

10
8
6
4
2
0

$V_{DS} = 10V$
130 pF

$V_{DS} = 15V$

60pF

0   0.4   0.8   1.2   1.6   2.0

Q_G (nanocoulombs)

Supertex inc.

©2001 Supertex Inc. All rights reserved. Unauthorized use or reproduction prohibited.

1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 744-0100 • FAX: (408) 222-4895
www.supertex.com