



Low Threshold N-Channel Enhancement-Mode Vertical DMOS FET

Features

- ▶ Low threshold — 2.0V max
- ▶ High input impedance
- ▶ Low input capacitance — 125pF max
- ▶ Fast switching speeds
- ▶ Low ON-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage
- ▶ Complementary N and P-channel devices

Applications

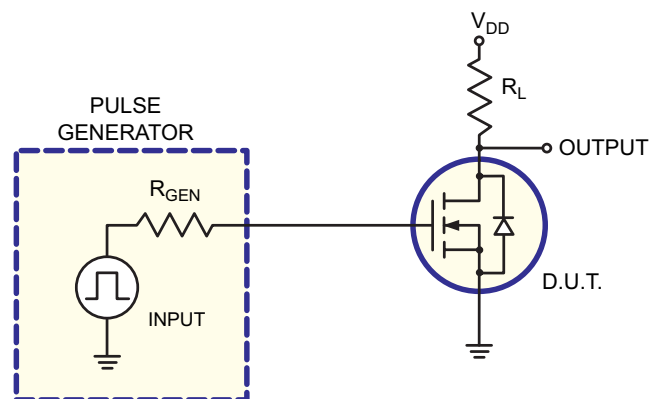
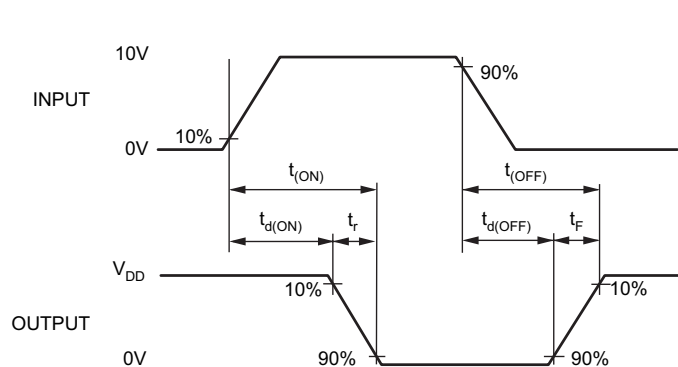
- ▶ Logic level interfaces — ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic devices
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

General Description

The Supertex TN2540 is a low threshold enhancement-mode transistor that utilizes an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Switching Waveforms and Test Circuit



Ordering Information

Device	Package Options			BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$V_{GS(th)}$ (max) (V)	$I_{D(ON)}$ (min) (A)
	TO-92	TO-243AA (SOT-89)	Die*				
TN2540	TN2540N3-G	TN2540N8-G	TN2540ND	400	12	2.0	1.0

-G indicates package is RoHS compliant ("Green")

* MIL visual screening available.



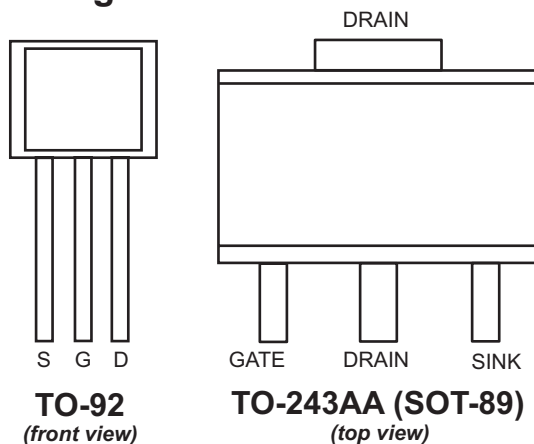
Absolute Maximum Ratings

Parameter	Value
Drain to source voltage	BV_{DSS}
Drain to gate voltage	BV_{DGS}
Gate to source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature*	$300^{\circ}C$

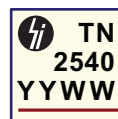
* Distance of 1.6mm from case for 10 seconds.

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



Product Marking



YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

TO-92 (N3)



W = Code for week sealed

TO-243AA (SOT-89) (N8)

Thermal Characteristics

Package	I_D (continuous) (mA)	I_D (pulsed) (A)	Power Dissipation @ $T_A = 25^{\circ}C$ (W)	θ_{jc} ($^{\circ}C/W$)	θ_{ja} ($^{\circ}C/W$)	I_{DR}^{\dagger} (mA)	I_{DRM} (A)
TO-92	175	2.0	1.0	125	170	175	2.0
TO-243AA (SOT-89)	260	1.8	1.6 \ddagger	15	78 \ddagger	260	1.8

Notes:

$\dagger I_D$ (continuous) is limited by max rated T_J .

\ddagger Mounted on FR5 board, 25mm x 25mm x 1.57mm.

Electrical Characteristics (@ 25°C unless otherwise specified)

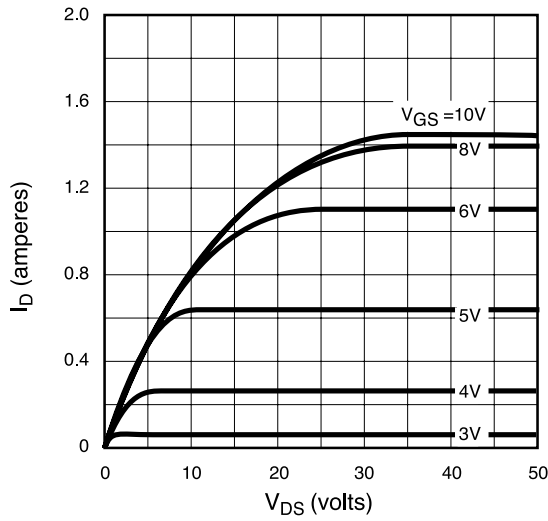
Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	400	-	-	V	$V_{GS} = 0V, I_D = 100\mu A$
$V_{GS(th)}$	Gate threshold voltage	0.6	-	2.0	V	$V_{GS} = V_{DS}, I_D = 1.0mA$
$\Delta V_{GS(th)}$	$V_{GS(th)}$ change with temperature	-	-2.5	-4.0	mV/°C	$V_{GS} = V_{DS}, I_D = 1.0mA$
I_{GSS}	Gate body leakage current	-	-	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	-	-	10	μA	$V_{GS} = 0V, V_{DS} = \text{Max rating}$
		-	-	1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ C$
$I_{D(ON)}$	ON-state drain current	0.3	0.5	-	A	$V_{GS} = 4.5V, V_{DS} = 25V$
		0.75	1.0	-		$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static drain-to-source ON-state resistance	-	8.0	12	Ω	$V_{GS} = 4.5V, I_D = 150mA$
		-	8.0	12		$V_{GS} = 10V, I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	0.75	%/°C	$V_{GS} = 10V, I_D = 500mA$
G_{FS}	Forward transconductance	125	200	-	mmho	$V_{DS} = 25V, I_D = 100mA$
C_{ISS}	Input capacitance	-	95	125	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$
C_{OSS}	Common source output capacitance	-	20	70		
C_{RSS}	Reverse transfer capacitance	-	10	25		
$t_{d(ON)}$	Turn-ON delay time	-	-	20	ns	$V_{DD} = 25V, I_D = 1.0A, R_{GEN} = 25\Omega$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-OFF delay time	-	-	25		
t_f	Fall time	-	-	20		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = 0V, I_{SD} = 200mA$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = 1.0A$

Notes:

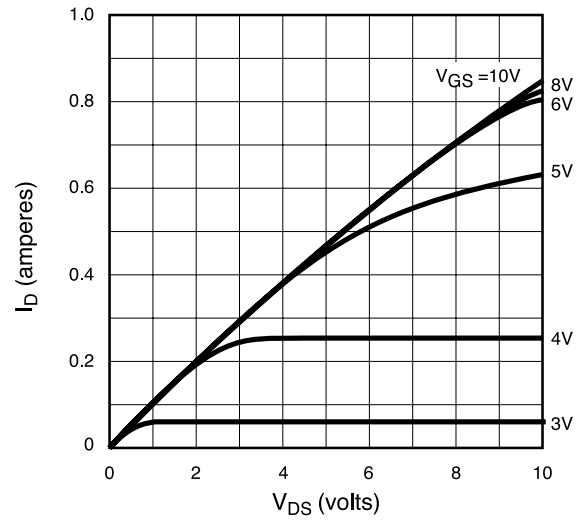
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μ s pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Typical Performance Curves

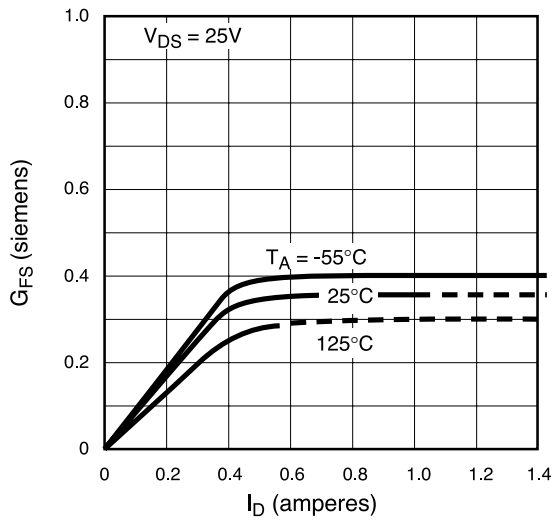
Output Characteristics



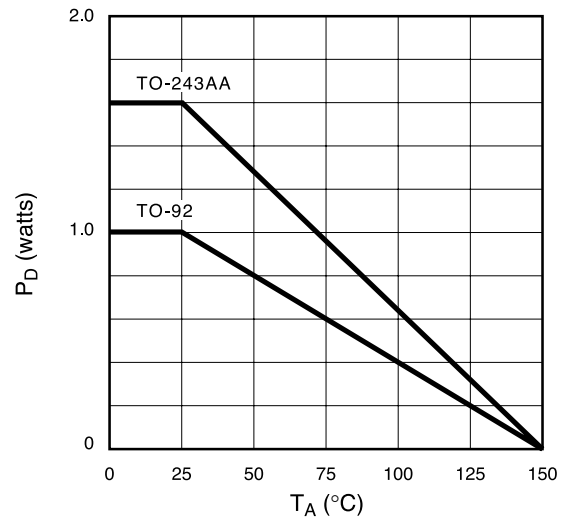
Saturation Characteristics



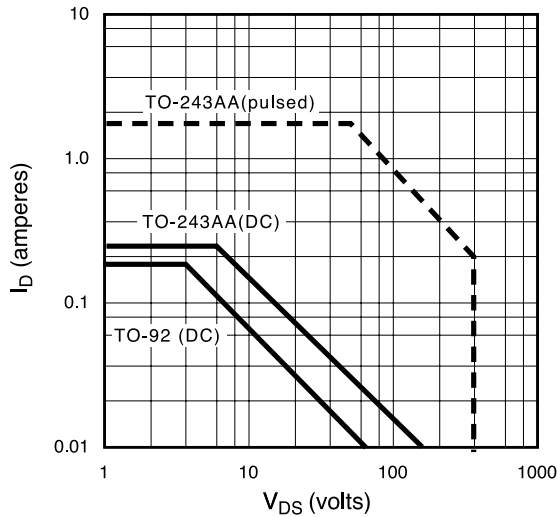
Transconductance vs. Drain Current



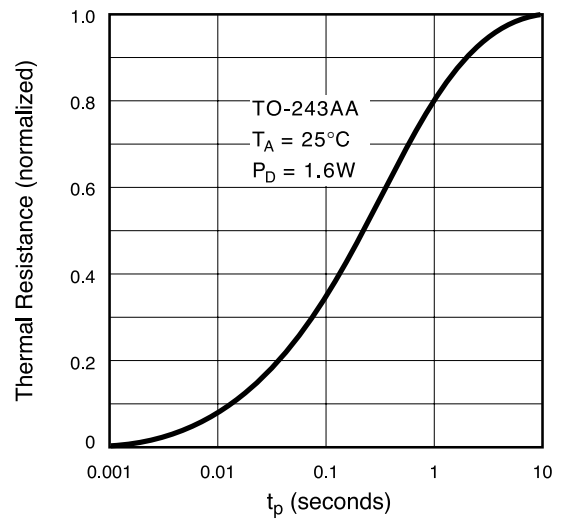
Power Dissipation vs. Ambient Temperature



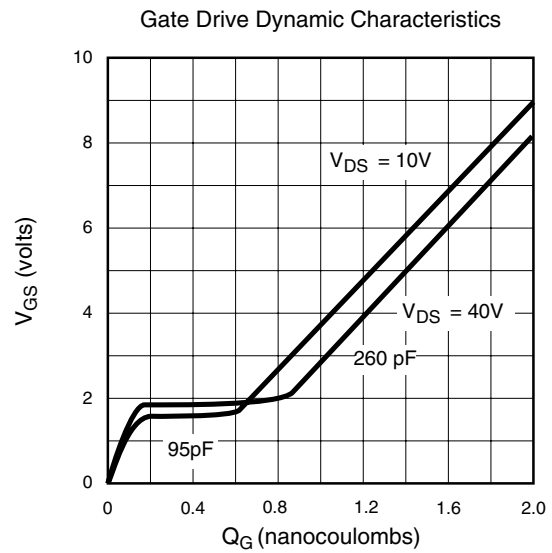
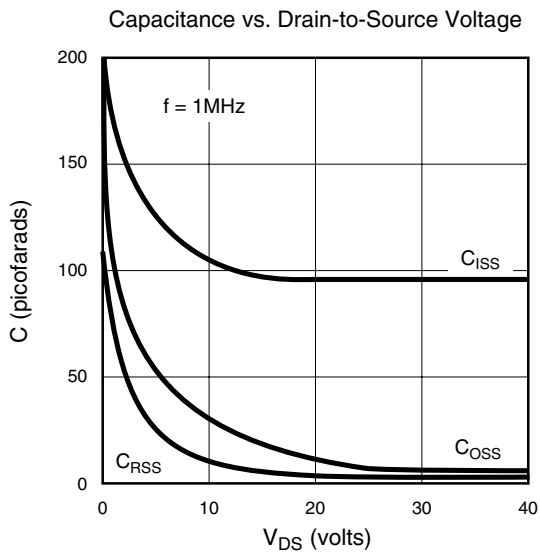
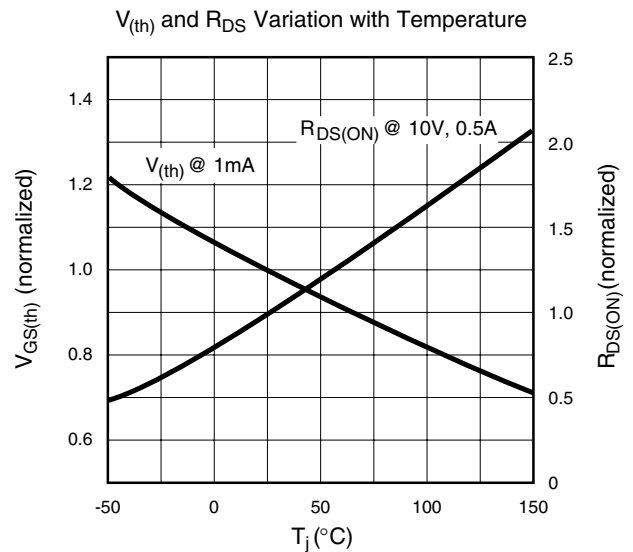
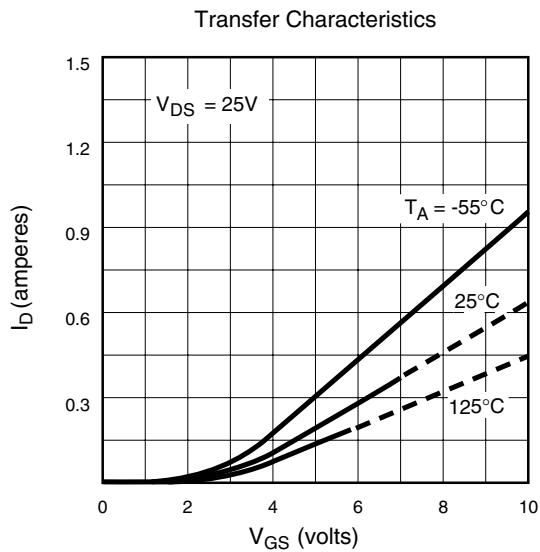
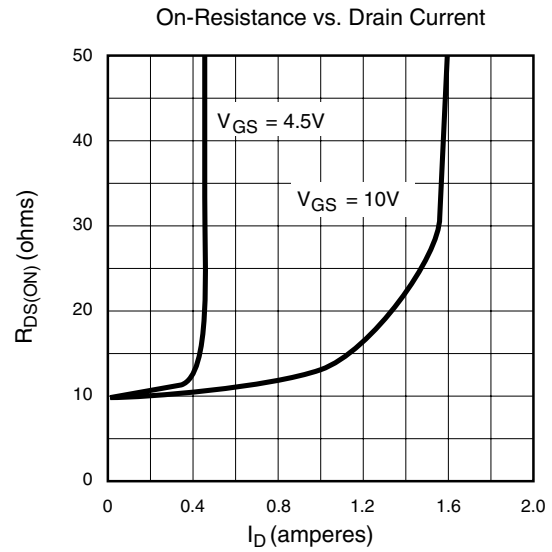
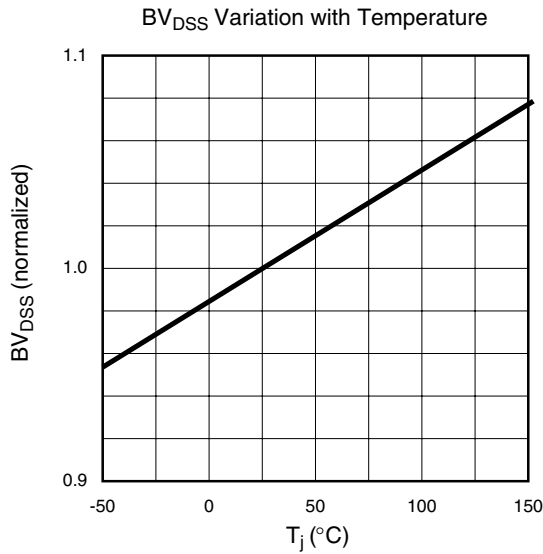
Maximum Rated Safe Operating Area



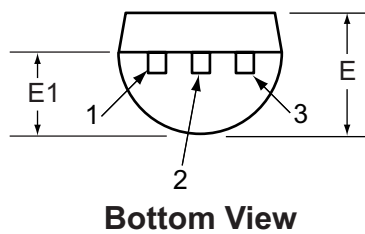
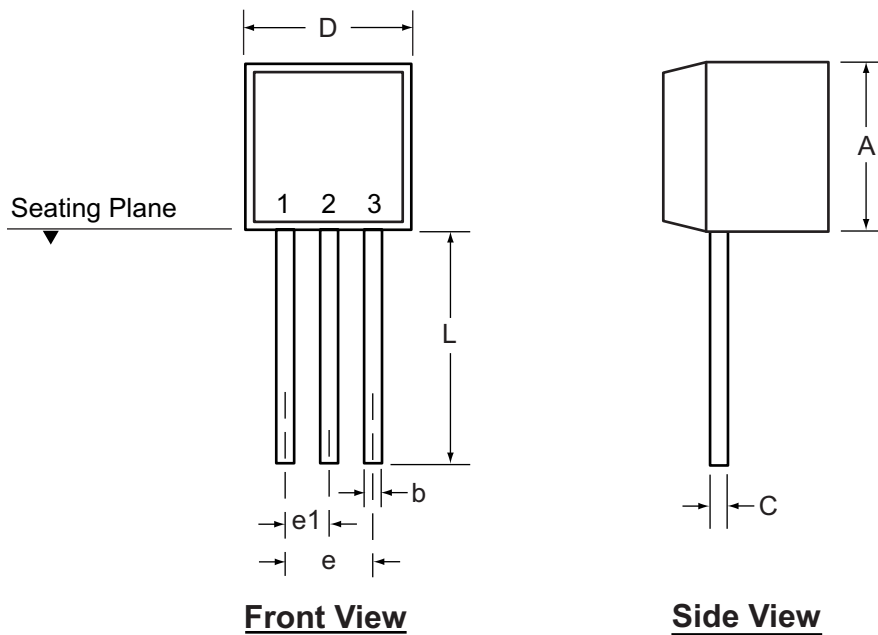
Thermal Response Characteristics



Typical Performance Curves (cont.)



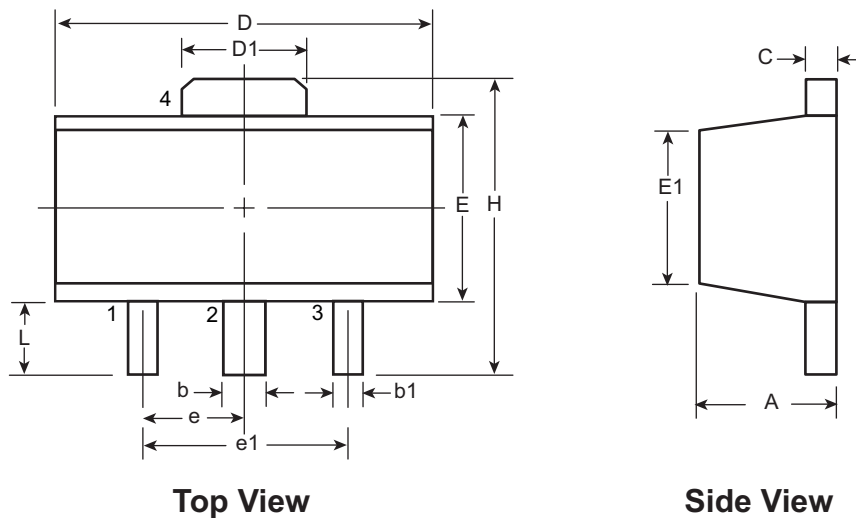
3-Lead TO-92 Package Outline (N3)



Symbol		A	b	C	D	E	E1	e	e1	L
Dimension (inches)	MIN	.170	.014	.014	.175	.125	.800	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022	.022	.205	.165	.105	.105	.055	-

Drawings not to scale.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.13	1.50 BSC	3.00 BSC	3.94	0.89
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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