N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
				TO-236AB	TO-243AA*	Wafer
350V	15Ω	2.0V	750mA	TN5335K1	TN5335N8	TN5335NW

* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

Features

- ❑ Low threshold – 2.0V max.
- ❑ High input impedance
- ❑ Low input capacitance
- ❑ Fast switching speeds
- ❑ Low on resistance
- ❑ Free from secondary breakdown
- ❑ Low input and output leakage

Product marking for SOT-23

N3S✳

Where ✳ = 2-week alpha date code

Product marking for TO-243AA

TN3S✳

Where ✳ = 2-week alpha date code

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

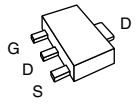
Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ❑ Logic level interfaces – ideal for TTL and CMOS
- ❑ Solid state relays
- ❑ Battery operated systems
- ❑ Photo voltaic drives
- ❑ Analog switches
- ❑ General purpose line drivers
- ❑ Telecom switches
- ❑ Modem hook switches

Package Options

TO-236AB
(SOT-23)
top view



TO-243AA
(SOT-89)

Note: See Package Outline section for dimensions.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_A = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-236AB	110mA	800mA	0.36W	200	350	110mA	800mA
TO-243AA	230mA	1.3A	1.6W†	15	78†	230mA	1.3A

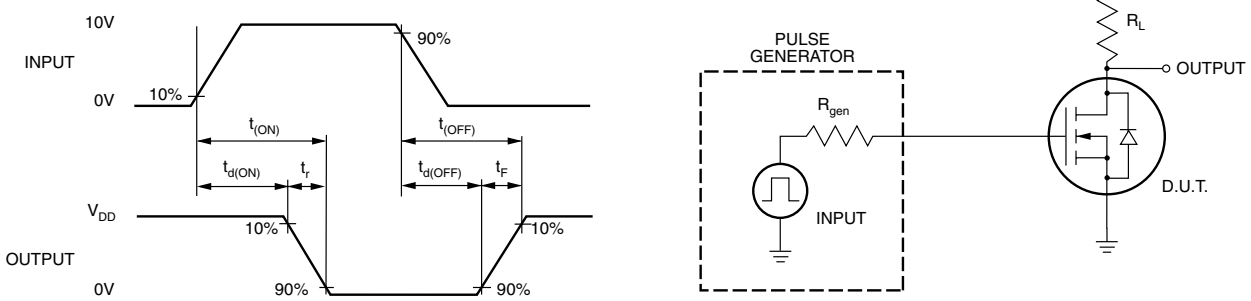
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	350			V	V_{GS} = 0V, I_D = 100μA
$V_{GS(th)}$	Gate Threshold Voltage	0.6		2.0	V	V_{GS} = V_{DS}, I_D= 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.5	mV/°C	V_{GS} = V_{DS}, I_D= 1mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ± 20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			1.0	μA	V_{GS} = 0V, V_{DS} = 100V
				10	μA	V_{GS} = 0V, V_{DS} = Max Rating
				1.0	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating, T_A = 125°C
				5.0	nA	V_{GS} = 0V, V_{DS} = 330V
$I_{D(ON)}$	ON-State Drain Current	300			mA	V_{GS} = 4.5V, V_{DS} = 25V
		750				V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to Source On-State Resistance			15	Ω	V_{GS} = 3.0V, I_D = 20mA
				15		V_{GS} = 4.5V, I_D = 150mA
				15		V_{GS} = 10V, I_D = 200mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.0	%/°C	V_{GS} = 4.5V, I_D = 150mA
G_{FS}	Forward Transconductance	125			m℧	V_{DS} = 25V, I_D = 200mA
C_{ISS}	Input Capacitance			110	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1Mhz
C_{OSS}	Common Source Output Capacitance			60		
C_{RSS}	Reverse Transfer Capacitance			22		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	V_{DD} = 25V, I_D = 150mA, R_{GEN} = 25Ω
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			25		
t_f	Fall Time			25		
V_{SD}	Diode Forward Voltage Drop			1.8	V	V_{GS} = 0V, I_{SD} = 200mA
t_{rr}	Reverse Recovery Time		800		ns	V_{GS} = 0V, I_{SD} = 200mA

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



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