

P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number/Package TO-236AB*
-60V	10Ω	-50mA	TP0610T

Product marking for SOT-23:

T50*

where * = 2-week alpha date code

Features

- ☐ Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{iss} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Logic level interfaces ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

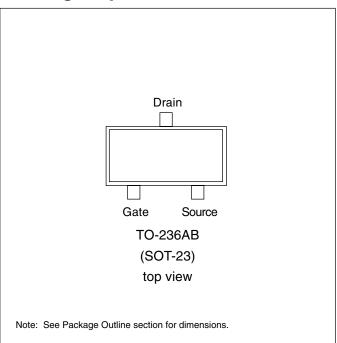
^{*} Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



^{*}Same as SOT-23. All units shipped on 3,000 piece carrier tape reels.

Thermal Characteristics

Package	I _D (continuous)*	I _D (pulsed)	Power Dissipation @ T _A = 25°C	$ heta_{ m jc}$ $^{\circ}$ C/W	$ heta_{ extsf{ja}}$ $^{\circ}$ C/W	I _{DR} *	I _{DRM}
SOT-23	-120mA	-400mA	0.36W	200	350	-120mA	-400mA

^{*} I_D (continuous) is limited by max rated T_j.

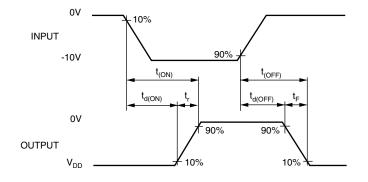
Electrical Characteristics (@ 25°C unless otherwise specified)

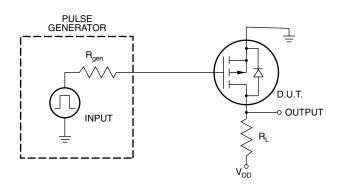
Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	-60			V	$V_{GS} = 0V, I_D = -10\mu A$	
V _{GS(th)}	Gate Threshold Voltage	-1.0		-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1.0$ mA	
$\Delta V_{GS(th)}$	Change in V _{GS(th)} with Temperature			6.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = -1.0$ mA	
I _{GSS}	Gate Body Leakage			±10	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I _{DSS}	Zero Gate Voltage Drain Current			-1	μΑ	$V_{GS} = 0V$, $V_{DS} = Max$ Rating	
				-200	μΑ	$V_{GS} = 0V$, $V_{DS} = 0.8$ Max Rating $T_A = 125$ °C	
I _{D(ON)}	ON-State Drain Current	-50			mA	$V_{GS} = -4.5V, V_{DS} = -10V$	
R _{DS(ON)}	Static Drain-to-Source			25	Ω	$V_{GS} = -4.5V, I_{D} = -25mA$	
	ON-State Resistance			10	Ω	$V_{GS} = -10V, I_D = -0.2A$	
$\Delta R_{DS(ON)}$	Change in R _{DS(ON)} with Temperature			1.0	%/°C	$V_{GS} = -10V, I_D = -0.2A$	
G _{FS}	Forward Transconductance	60			mъ	$V_{DS} = -10V, I_{D} = -0.1A$	
C _{ISS}	Input Capacitance			60	pF		
C _{OSS}	Common Source Output Capacitance			30		$V_{GS} = 0V, V_{DS} = -25V$ f = 1 MHz	
C _{RSS}	Reverse Transfer Capacitance			10		1 – 1 101112	
t _{d(ON)}	Turn-ON Delay Time			10			
t _r	Rise Time			15	ns	$V_{DD} = -25V$ $I_{D} = -0.18A$	
t _{d(OFF)}	Turn-OFF Delay Time			15		$R_{GEN} = 25\Omega$	
t _f	Fall Time			20		GLIN -	
V _{SD}	Diode Forward Voltage Drop			-2.0	V	V _{GS} = 0V, I _{SD} = -0.12A	
t _{rr}	Reverse Recovery Time		400		ns	$V_{GS} = 0V, I_{SD} = -0.4A$	

Notes:

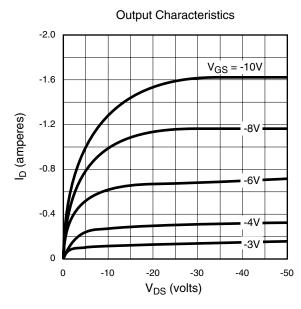
- 1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu s$ pulse, 2% duty cycle.)
- 2. All A.C. parameters sample tested.

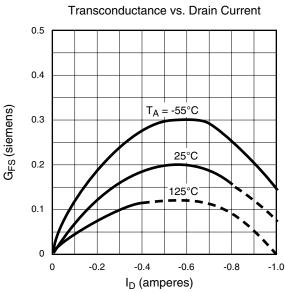
Switching Waveforms and Test Circuit

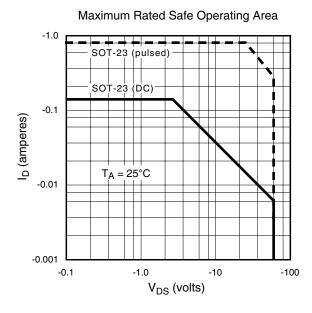


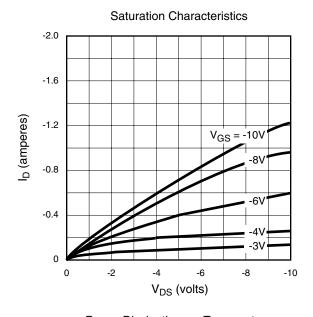


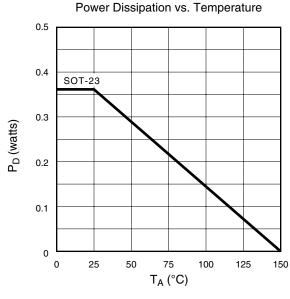
Typical Performance Curves

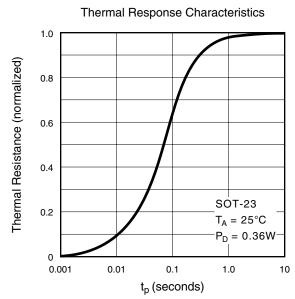




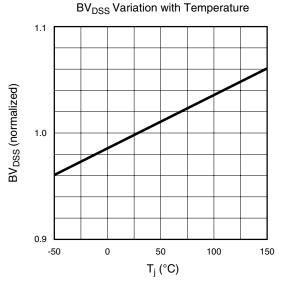


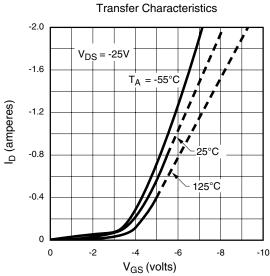


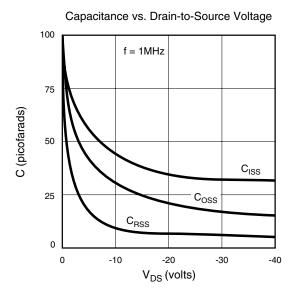


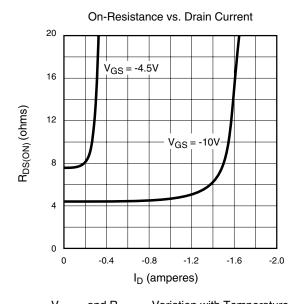


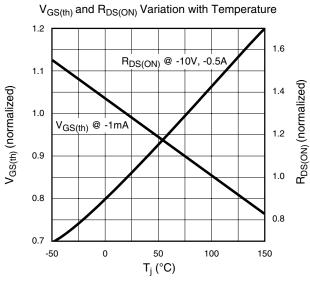
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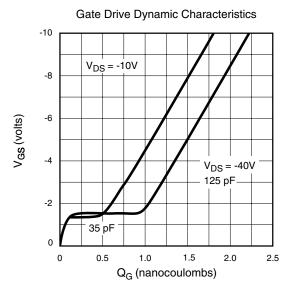












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