TOPRO
凌越科技
Topro Technology Inc.

TP6410

160-OUTPUT STN SEGMENT DRIVER

DataSheet

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OVERVIEW

Description

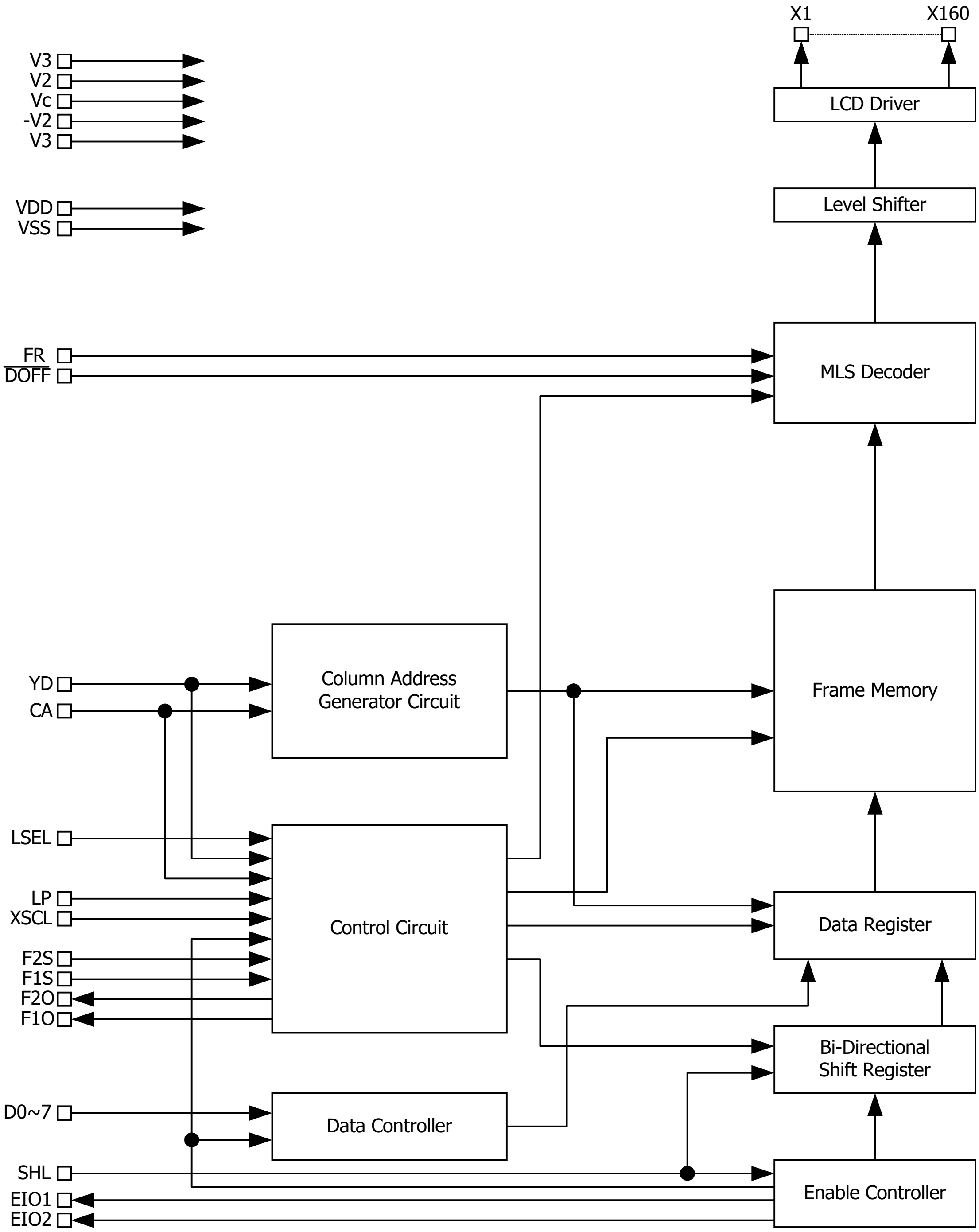
The TP6410 is a 160-output, 5-level segment (column) driver for MLS (Multi-Line Selection) driving, able to drive with both high contrast and high speed. It is used in conjunction with the TP6401. When paired with the TP6401 it can be connected to LCD controller.
Because the TP6410 stores display data in its internal display RAM and generates LC drive signals, display data transmission from the controller can be suspended except for when there are changes to the display, thereby enabling an ultra low power display system. The TP6410 uses a slim package, facilitating the construction of thinner LCD panels, and the low-voltage operation of its logic power source makes it appropriate to a wide range of applications.

FEATURES

• Number of simultaneous line selects: 4 Lines
• Drive duty ratio (MAX) 1/240 duty
• LCD driver outputs 160 outputs
• Internal display RAM 160 × 240 bit
• Extremely low consumption current
• Power Source Voltages Logic System: 3.0 to 3.6V (Max)
LCD System: 6.0 to 7.2V (Max)
• High speed, low power data transmission possible through the 4-bit/8-bit switchable bus enable chain method
• Non-biased display off function
• Output shift direction pin select supported
• Slim chip shape
• Shipment status:
In CHIP form TP6410D0B
In TCP form TP6410T0A
• This product is not designed for resistance to light or radiation

BLOCK DIAGRAM

Block Diagram



Pin Functions

Pin Functions Table

Pin Name	I/O	Function	# of Pins
X1 to X160	O	Segment (column) output to drive the LC.Output transition occurs on falling edge of LP.	160
BSEL	I	Display data input bit number select input. "L": 4 bit input. "H": 8 bit input.	1
LSEL	I	1/2 H operation select input. "L":Normal operation. "H": 1/2 H operation.	1
D0 toD7	I	Display data input. When 4 bit input is used, D0 toD3 is used,and D4 toD7 can be left NC.	8
XSCL	I	Display data shift clock input. Display data (D0 toD7) is read sequentially into the data register on the falling edge.	1
LP	I	Display data latch clock input * Accepts into the LCD driver the control signal from the LC driver selected by the MLS decoder, doing so at the falling edge, and outputs the LC driver output. * Writes the contents of the data registers to the frame memory 4 LP at a time for the specified column address. * Resets the enable control circuit. * When 1/2 operation is selected, inputs the LP with twice the normal frequency.	1
EIO1 EIO2	I/O	Enable I/O * Is set to input or output depending on the SHL input level. * When output, the LP input is reset (in an "H" state), and when the 160 bit of display data has been read in, the signal automatically falls to L. *When connected in cascade, is connected to the next stage EIO input.	1 1
SHL	I	Shift direction select and EIO terminal I/O control input. WHEN BSEL= "L" (i.e. 4-bit input): When the display data has been input to terminals (D3, D2, D1, D0) in the order (a, b, c, d) (e, f, g, h)... (w, x, y, z), the relationship between the data and the segment is as shown in the table below: SHL SHLXn (Segment Output) EIO 160 159 158 157 156 155 154 153 ... 8 7 6 5 4 3 2 1 1 2 L a b c d e f g h ... s t u v w	1

x
y
z
Output
Input

H
z
y
x
w
v
u
t
s
...
h
g
f
e
d
c
b
a
Input
Output

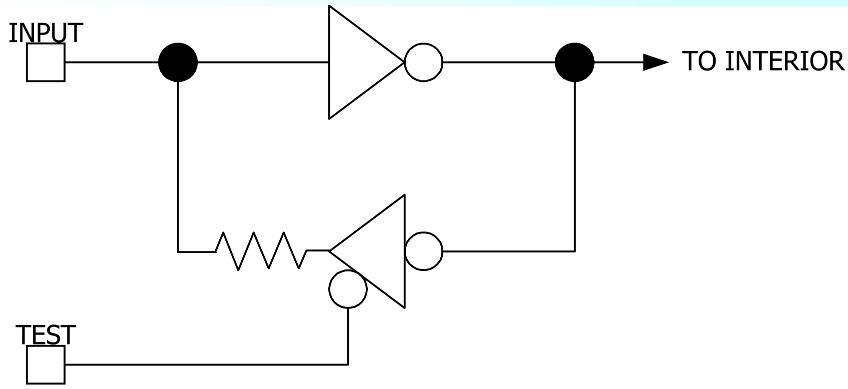
WHEN BSEL = "H" (i.e., 8-bit input):
When the display data has been input to terminals (D7, D6, D5, D4, D3, D2, D1, D0) in the order (a, b, c, d, e, f, g, h) ... (s, t, u, v, w, x, y, z), the relationship between the data and the segment is as shown in the table below:
SHL
SHLXn (Segment Output)
EIO

160
159
158
157
156
155
154
153
...
8
7
6
5
4
3
2
1
1
2

L
a
b
c
d
e
f
g
h
...
s
t
u
v

		w x y z Output Input H z y x w v u t s … h g f e d c b a Input Output	
DOFF	I	Forced blank input. When at "L" level, segment output is forced to Vc. The display RAM data is maintained.	1
FR	I	LC drive output AC signal input. With terminator (*1).	1
YD	I	Frame running start input * Resets the column address for writing or reading. * The number of running lines for writing (column address number) relating to frame memory is determined based on the number of LP pulses input during a single YD cycle.	1
CA	I	Field delimiter signal input. With terminator (*1). This signal is input at the start of each new field, and is output by the TP6401.	1
F1S F2S	I	Drive pattern cutover gap set input (F2S, F1S) = (0,0), (0,1), (1,0), (1,1) Cutover gap Field, 8H, 2H, 4H	1 1
F1O F2O	O	Driver pattern select output for the Y driver. Connects to the common (row) driver.	1 1
VDD, VSS	Power	Power supply for logic.	1 each
V3, V2, VC, −V2, −V3	Power	Power supply for LC driver. V3 > V2 > VC > −V2 > −V3	5 each

Note: *1Regarding the terminator


INPUT
TO INTERIOR
TEST

FUNCTIONS

The Functional Blocks

Enable Control

When the enable signal is in a disable state (EIO = "H"), the internal clock signal and data bus are fixed at "L", placing the chip in power save mode.
When multiple segment drivers are used, the EIO terminals of the various drivers are cascade connected and the EIO terminal of the first driver is connected to "VSS".
The enable control circuit automatically senses when 160 bits worth of data have been received, and automatically sends the enable signal, thus eliminating the need for a control signal from the control LSI.

Bi-directional Shift Register

This sends the control signal for writing the display data D0 – D7 to the data register. The order in which the display data is latched into the data register by the SHL input is returned (SIC?Reversed?).

Data Register

This is a 160 dot register which controls writing to the display RAM. It has 4 lines. At each falling edge of the LP signal it accepts display data from one line, and writes to the frame memory after it has stored 4 lines of data.

Frame Memory

This is static RAM (with peripheral circuits) that stores LC display data. It has a capacity of 160 segments by 240 lines.

MLS Decoder

This outputs the drive control signals necessary for the 4 MLS driving. The control signal is set by field information provided by the four lines of display data, FR, DOFF, and the control circuit.

LCD Driver

The LCD driver outputs the LC drive voltage. The driver voltage is selected by the control signal from the 5 levels V3, V2, VC, –V2 and –V3, determined by the MLS decoder.

Column Address Generating Circuit

When writing to or reading from frame memory, this outputs the column address corresponding to the location of the RAM in frame memory.

Level Shifter

This is a level interface circuit used to convert signal levels when signals are propagated from low-voltage parts to high-voltage parts.

Data Control

This accepts display data input when enabled, and sends it to the data register.

Control Circuit

This determines the self refresh rate, enables the data register to write to the display RAM, controls the output of the column address generator, and performs field control on the MLS decoder.

The Self Refresh Function

Setting the Self Refresh Mode

"Self refresh mode" refers to a situation where the transmission of display data from the display controller to the TP6410 is suspended when the content of the display does not change, and where the TP6410 automatically senses this and enters a power down display mode. To place the TP6410 in the self refresh mode maintain the shift clock XSCL at the "L" level during four horizontal display periods (4x the LP signal period) after the completion of the input of the display data of an n + 3 line.
When the XSCL is suspended, the power is reduced, so display data inputs D0 – D7 are suspended, as is transmission from the display controller, being set to "H" or "L". At this time the display controller must send LP, YD, or FR signals periodically to the TP6410 as it does when data is being sent. The TP6410 receives these signals, periodically reads display data from its internal RAM, and refreshes the display. The display off function is operational even when in the self refresh mode.

Getting Out of the Self Refresh Mode

In order to get out of the self refresh mode, the display controller inputs the shift clock XSCL to the TP6410 for four or more horizontal display periods with the timing of the data transmission from the falling edge of the LP signal at the time of an n + 3 line. With the falling edge of the LP signal after the fourth horizontal period after getting out of this mode, the display data transmitted during the four horizontal display intervals is written to frame memory.

When TP6410s are cascade connected, if the number of XSCL clocks input does not correspond to the cascade connections, then not all of the TP6410s will be released from self refresh mode.

Note : When the number of lines is 240:

n lines	1, 5, 9, ...233, 237 (1 + multiples of 4)
n + 1 lines	2, 6, 10,...234, 238 (2 + multiples of 4)
n + 2 lines	3, 7, 11,...235, 239 (3 + multiples of 4)
n + 3 lines	4, 8, 12,...236, 240 (Multiples of 4)

The Relationship Between Drive Output Voltages and Display Data

F20, F10, and the common drive voltage have the following relationships:

FR	L				H			
F1O F2O	1 1	0 1	1 0	0 0	1 1	0 1	1 0	0 0
n line	V1	V1	-V1	V1	-V1	-V1	V1	-V1
n + 1 line	-V1	V1	V1	V1	V1	-V1	-V1	-V1
n + 2 line	V1	-V1	V1	V1	-V1	V1	-V1	-V1
n + 3 line	V1	V1	V1	-V1	-V1	-V1	-V1	V1

Note:Voltage relationships: V1 > VC > –V1 (VC is the middle voltage level)

The transitions in (F2O, F1O) within each field when the drive pattern changes:

First field	In the order (1,1) → (1,0) → (0,1) → (0,0) → (1,1) → (1,0) → (0,1) → (0,0)
Second field	In the order (1,0) → (0,1) → (0,0) → (1,1) → (1,0) → (0,1) → (0,0) → (1,1)
Third field	In the order (0,1) → (0,0) → (1,1) → (1,0) → (0,1) → (0,0) → (1,1) → (1,0)
Fourth field	In the order (0,0) → (1,1) → (1,0) → (0,1) → (0,0) → (1,1) → (1,0) → (0,1)

This is determined by the values of the inputs (F2S, F1S) during the changeover interval. The relationship between F2S and F1S and the changeover interval is as follows:
When the changeover interval is selected for each field, the value stored in the field is the first value shown in the shown in the (F2O, F1O) change table above (the value on the left).

F2S	F1S	Changeover Interval
0	0	Field
0	1	8-line interval
1	0	2-line interval
1	1	4-line interval

The relationship between the display data, the LC AC signal FR, and the segment output voltage is as shown below. The output voltage changes in conjunction with the F20, F10 values that determine the common drive voltage.
Display data: 0= not lit, 1 = lit
WhenFR = “L”

Display Line	n line	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	n + 1 line	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	n + 2 line	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	n + 3 line	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Drive Voltage	(F2O, F1O)=(1,1)	V2	VC	VC	-V2	V3	V2	V2	VC	VC	-V2	-V2	-V3	V2	VC	VC	-V2
	(F2O, F1O)= 1,0)	V2	VC	V3	V2	VC	-V2	V2	VC	VC	-V2	V2	VC	-V2	-V3	VC	-V2
	(F2O, F1O)=(0,1)	V2	VC	VC	-V2	VC	-V2	-V2	-V3	V3	V2	V2	VC	V2	VC	VC	-V2
	(F2O, F1O)=(0,0)	V2	V3	VC	V2	VC	V2	-V2	VC	VC	V2	-V2	VC	-V2	VC	-V3	-V2

When FR = “H”

Display Line	n line	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	n + 1 line	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	n + 2 line	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	n + 3 line	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Drive Voltage	(F2O, F1O)=(1,1)	-V2	VC	VC	V2	-V3	-V2	-V2	VC	VC	V2	V2	V3	-V2	VC	VC	V2
	(F2O, F1O)=(1,0)	-V2	VC	-V3	-V2	VC	V2	-V2	VC	VC	V2	-V2	VC	V2	V3	VC	V2
	(F2O, F1O)=(0,1)	-V2	VC	VC	V2	VC	V2	V2	V3	-V3	-V2	-V2	VC	-V2	VC	VC	V2
	(F2O, F1O)=(0,0)	-V2	-V3	VC	-V2	VC	-V2	V2	VC	VC	-V2	V2	VC	V2	VC	V3	V2

When DOFF = “L”, all drive outputs are tied to the VC level.

LC Drive Output Voltages During

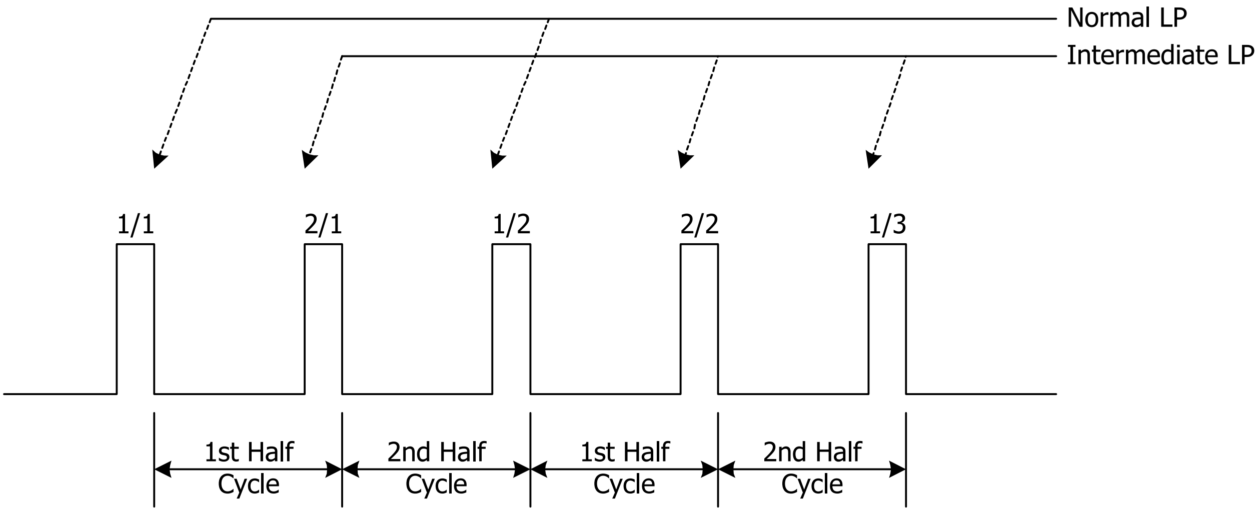
1/2 H Operation

When LSEL is set to “H” and twice the normal frequency is applied to the LP input terminal, then the chip functions in 1/2 mode. Each time LP is input the field data changes, thus the output changes at the center point of the 1H interval. However, the input of display data to the D1580, writing of display data to the frame memory, and read in display data from the frame memory is the same as in the normal drive.
The Y driver output changes according to the field data output by the X driver with each LP input, causing a transition at the center point of the 1H interval; however, the transition of the drive line occurs each 1H, just as in the normal drive.
During 1/2 H operation, the changes of the F20, F10 in each field are as shown in the table below. In this table the statuses of the F20 and F10 are represented as given below:

(F2O, F1O) = (1,1)	（1）
(F2O, F1O) = (1,0)	（2）
(F2O, F1O) = (0,1)	（3）
(F2O, F1O) = (0,0)	（4）

	First Half Cycle	Second Half Cycle	First Half Cycle	Second Half Cycle	
Field #1	（4）	（1）	（1）	（4）	This pattern is repeated hereafter.
Field #2	（1）	（4）	（4）	（1）	
Field #3	（3）	（2）	（2）	（3）	
Field #4	（2）	（3）	（3）	（2）	

During 1/2H operation, the values of F2S and F1S are ignored.

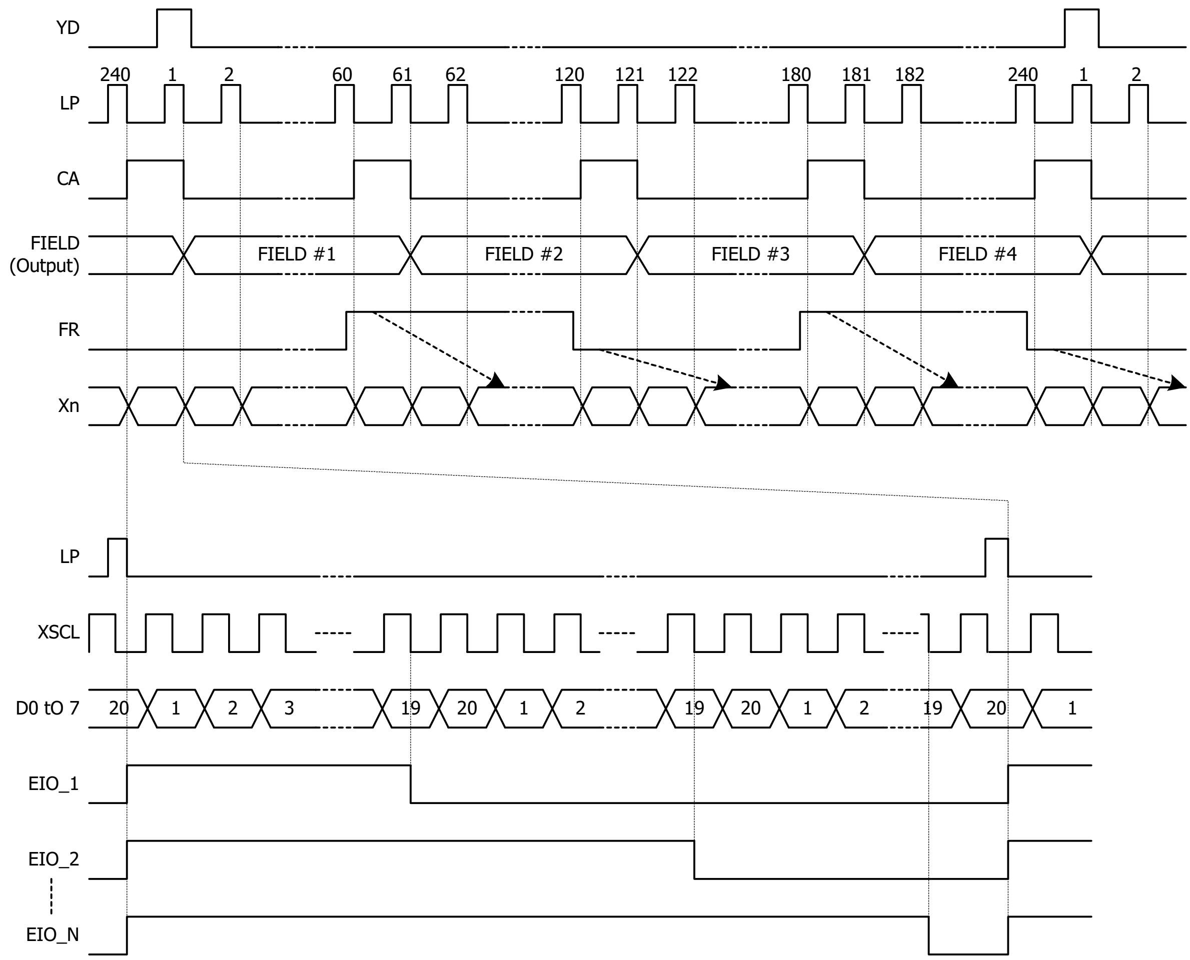


The segment output voltage during 1/2 H operation also follows the display data of 4.3 and the diagram showing the relationship between the LC AC signal FR and the segment output voltage. In the signal B/ A that indicates the number of the LP, the “A” in the figure indicates LP during a normal drive, and “B” differentiates between the normal LP and the intermediate LP (where B = 1 is normal and B = 2 is intermediate).

Timing diagram (assuming 1/240 duty)

(This diagram provided only as a reference.)

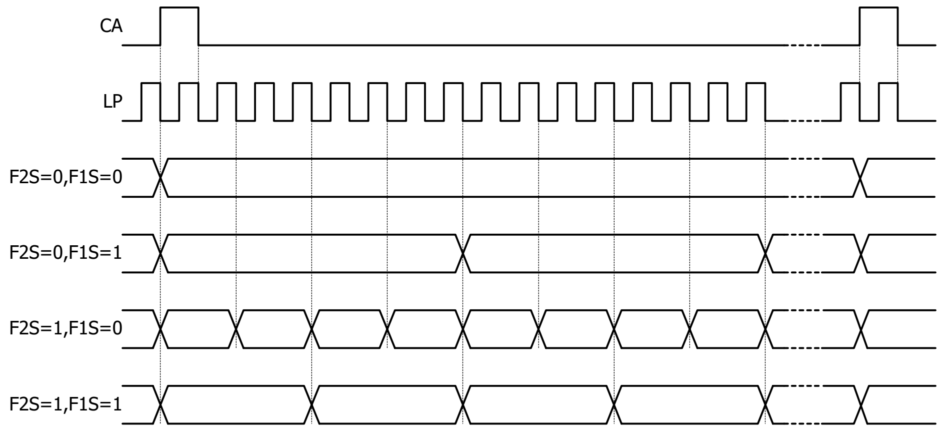
Normal Drive Timing



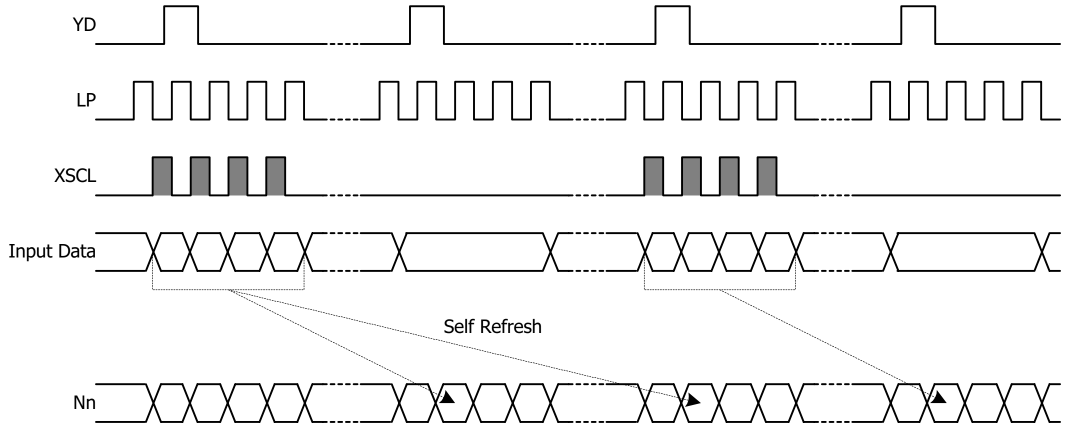
_1 to _n Indicate Driver Cascade Numbers

TOPRO CONFIDNETIAL

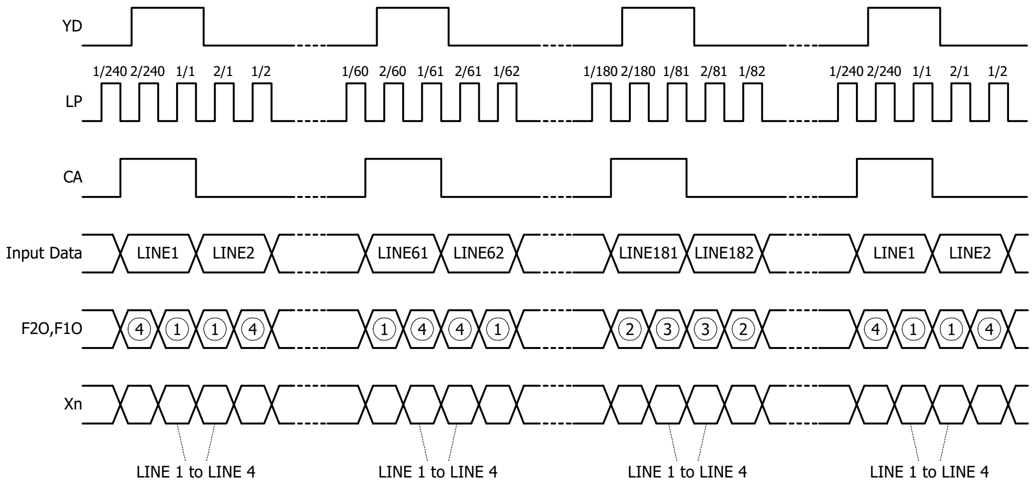
F2O, F1O Change Timing



Setting and Releasing Self Refresh



1/2 H Drive Timing



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

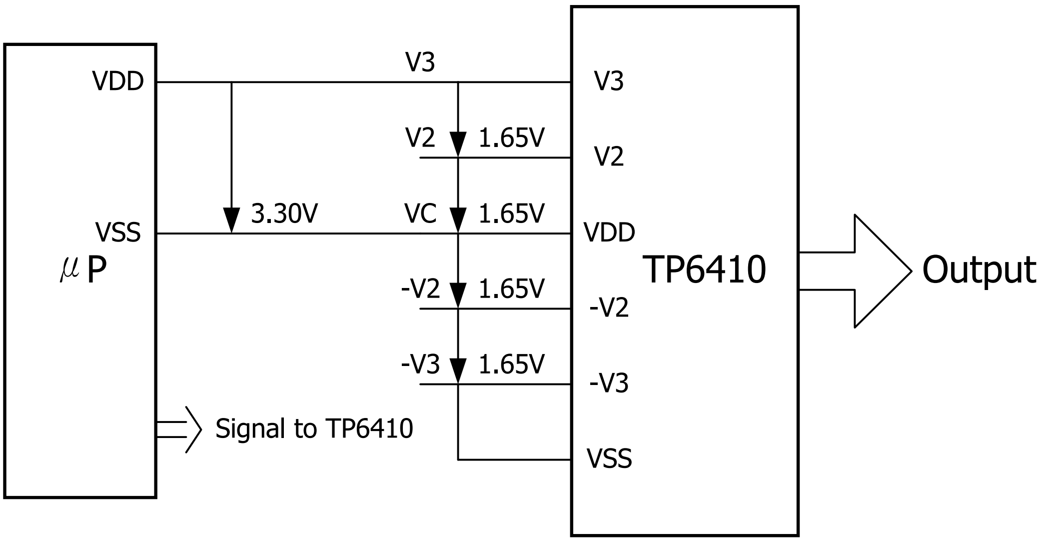
Parameter	Symbol	Rating	Units
Power voltage (1)	VSS	–7.0 to +0.3	V
Power voltage (2)	–V3	–8.0 to +0.3	V
Input voltage	VI	VSS –0.3 to VDD +0.3	V
Output voltage	VO	VSS –0.3 to VDD +0.3	V
EIO output current	IO1	20	mA
Operating temperature	Topr	–20 to +85	℃
Storage temperature 1	Tstg1	–65 to +150	℃
Storage temperature 2	Tstg2	–55 to +100	℃

Note 1: The voltages are all relative to VDD = 0V.

Note 2: Storage temperature 1 is the recommendation for the chip itself or for the chip and a plastic package, and storage temperature 2 is the recommendation for the chip mounted on TCP.

Note 3: Ensure that the relationship between V3, V2, VC, –V2 and –V3 is always as follows:

VDD ≥ V3 > V2 > VC > –V2 > –V3



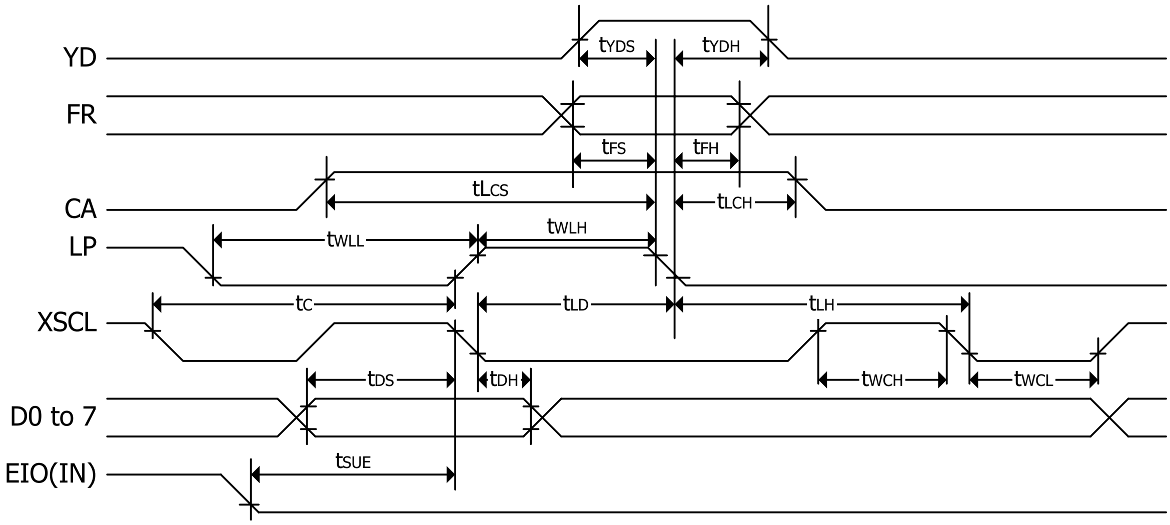
DC Characteristics

Unless otherwise specified, VDD = V3 = 0V, VSS = –3.3V ± 0.3V, Ta = –20 to 85°C

Parameter	Symbol	Conditions	Applicable terminals	Min	Typ	Max	Units
Power voltage (1)	VSS		VSS	-3.6	-3.3	-3.0	V
Power voltage (2)	-V3	VSS = –3.0V to –3.6V	-V3	-7.2	-6.4	-6.0	V
Power voltage (3)	-V2	VSS = –3.0V to –3.6V	-V2		(–V3)* 3/4		V
Power voltage (4)	VC	VSS = –3.0V to –3.6V	VC		(–V3)* 2/4		V
Power voltage (5)	V2	VSS = –3.0V to –3.6V	V2		(–V3)* 1/4		V
High-level input voltage	VIH	VSS =–3.3V to –3.6V	EIO1,EIO2,SHL,BSEL,LSEL,FR,YD,CA, LP,XSCL,D0 to D7, F1S, F2S, DOFF	0.2* VSS			V
Low-level input voltage	VIL					0.8* VSS	V
High-level output voltage	VOH	VSS =–3.3V to –3.6V; IOH =–0.6mA	EIO1, EIO2 F1O, F2O	VDD – 0.4			V
Low-level output voltage	VOL	IOL =0.6mA				VSS + 0.4	V
Input leakage current	ILI	VSS≦VIN≧VDD	SHL, BSEL, LSEL, FR, YD, CA, LP, XSCL, D0 to D7, F1S, F2S, DOFF			5.0	μA
I/O leakage current	ILI/O	VSS≦VIN≧VDD	EIO1, EIO2			5.0	μA
Static current (1)	ISSq	VIN= VDD or VSS	VSS			TBD	μA
Static current (2)	–I3T	–V3 = –6.6V	–V3			TBD	μA
Output resistance	RSEG	VON = 0.5V, VSS = –3.30V, V3 = VDD = 0V, V2 = –1.65V, VC = –3.30V, –V2 = –4.95V, V3 = 6.60V	X1 to X160		TBD	TBD	KΩ
Average operating consumption current (1) — Data Transfer Mode	ISST	VSS = –3.30V, V3 = VDD = 0V, V2 = –1.65V, VC = –3.30V –V2 = –4.95V, –V3 = –6.60V VIN = VDD or VSS, fXSCL = 480 kHz, fLP = 12kHz, fFR = 30Hz, Input Data: checker pattern, 8-bit, 320 200, no load	VSS		TBD	TBD	μA
Average operating consumption current (1) — Self Refresh Mode	ISSS	XSCL = VSS Other parameters are the same as for ISST	–V3		TBD	TBD	μA
Average operating consumption current (2)	–I3T	Parameters are the same as for ISST			TBD	TBD	μA
Input terminal capacitance	CI	Freq = 1 MHz Ta = 25C Chip alone	SHL,BSEL,LSEL,FR,YD,CA,LP,XSCL, D0 to D7, F1S, F2S, DOFF			8	pF
I/O terminal capacitance	CI/O		EIO1, EIO2			15	pF
Output terminal capacitance	CO		F1O, F2O			7	pF

AC Characteristics

Input Timing Characteristics



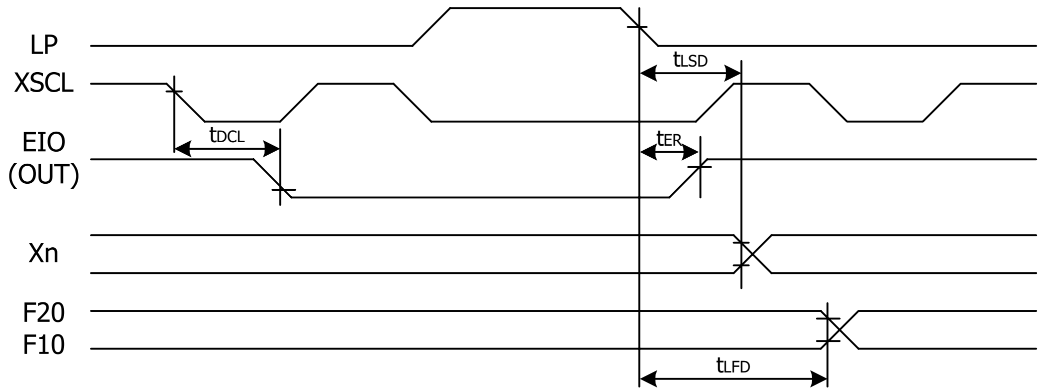
VSS = –3.3 V ± 0.3 V, VIH = 0.2 VSS, VIL = 0.8 VSS

Parameter	Symbol	Conditions	Min	Max	Units
XSCL period	t_C		TBD		ns
XSCL high level pulse width	t_{WCH}		TBD		ns
XSCL low level pulse width	t_{WCL}		TBD		ns
Data setup time	t_{DS}		TBD		ns
Data hold time	t_{DH}		TBD		ns
Time between XSCL and LP fall	t_{LD}		TBD		ns
Time between LP and XSCL fall	t_{LH}		TBD		ns
LPhigh level pulse width	t_{WLH}		TBD		ns
LP low level pulse width	t_{WLL}		TBD		ns
FR setup time	t_{FS}		TBD		ns
FR hold time	t_{FH}		TBD		ns
EIO setup time	t_{SUE}		TBD		ns
YD setup time	t_{YDS}		TBD		ns
YD hold time	t_{YDH}		TBD		ns
CA setup time	t_{LCS}		TBD		ns
CAhold time	t_{LCH}		TBD	TBD	ns
Input signal rise time and fall time	tr, tf			TBD	ns

Note: CA is only effective at the first LP in the field. Assuming 1/N duty, the “first LP” refers to 1 and 1+ (multiples of (N/4).

FR is accepted at the falling edge of LP, and its state is reflected into the output that changes at the falling edge the following 1H.

Output Timing Characteristics

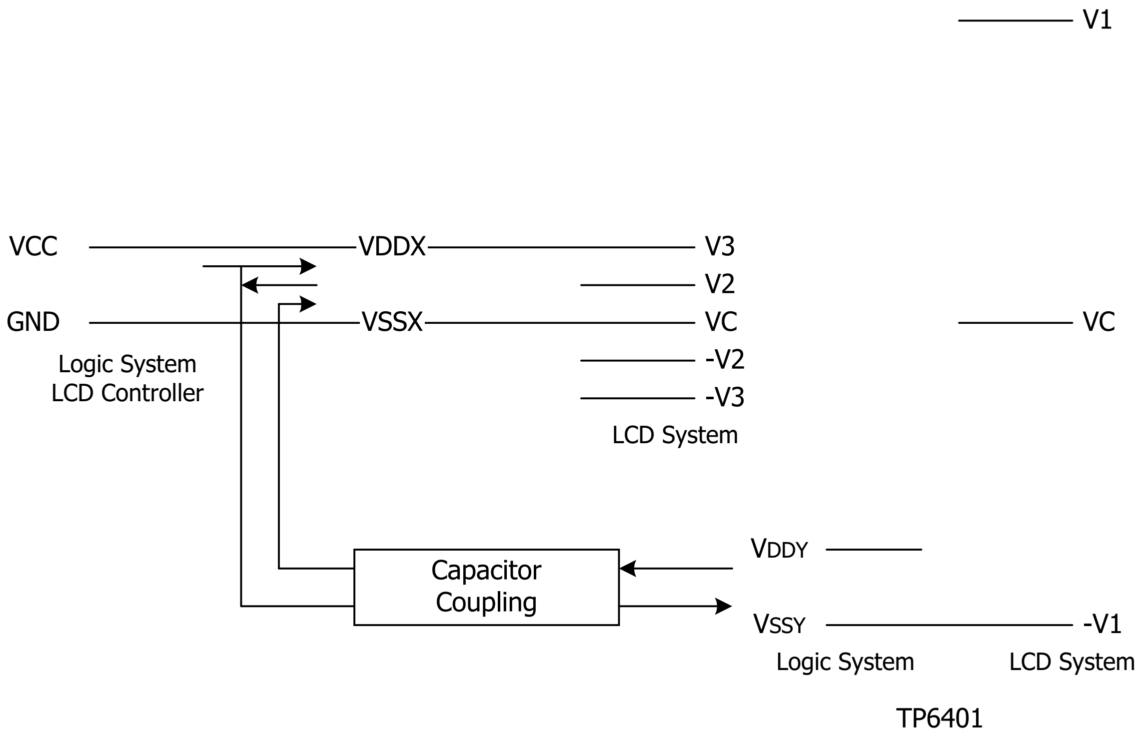


VSS = –3.3V ± 0.3V, VIH = 0.2 VSS, VIL = 0.8 VSS, –V3 = –6.6V ± 0.6V

Parameter	Symbol	Conditions	Min	Max	Units
EIO reset time	tER	CL = 15 pF (EI0)		TBD	ns
EIO output delay time	tDCL			TBD	ns
LP Õ Xn output delay time	tLSD	CL = 100 pF		TBD	ns
LP → F2O, F1O output delay time	tLFD			TBD	ns

POWER SOURCE

The Relationship Between Voltage Levels



When the TP6410 and TP6401 are used to structure an extremely low-power module system, the power supplies for the TP6410 logic systems and LCD systems, and the power supplies for the LCD controller should have the voltage relationships shown in the figure above.
In this case, caution is required when sending signals to the logic system. Specifically, use caution with the following:

LCD Controller	→	TP6410	Direct connection
LCD Controller	→	TP6401	Requires a capacitor coupling
TP6410	→	TP6401	Requires a capacitor coupling
TP6401	→	TP6410	Requires a capacitor coupling

Cautions During Power Up and Power Down

This LSI requires special attention to be paid to the sequence in which the power supplies are turned on. Ensure that the power supply ON sequence is always one of the sequences below:

Logic system ON → First LP cycle → LCD system ON

or

Logic system ON → DOFF = "L" → LCD system ON → First LP cycle (*2) → DOFF = "H"

After applying power to the TP6410, the 2 frame interval is not displayed correctly because the number of LP cycles input in the first frame is counted and used to determine an address in the frame memory. This requires the use of DOFF. Consequently, display data should be transmitted at the point marked with (*2).
For power down, use the LCD system OFF → Logic system OFF sequence, or power both down at the same time.

Notes

Regarding this development specification, take the followings into consideration.
1.The contents of this development specification may be revised without prior notice.
2.This development specification does not guarantee or grant the industrial property rights or any other rights.
The application examples contained in this development manual are given in order to help customers understand the product. Note that we shall not take any responsibility regarding problems on circuits.
Regarding the use of semiconductor elements, take the followings into consideration.

[Precautions on Handling Optical Parts]

Following the solar cell theory, the characteristics of a semiconductor element changes as it is exposed to the light. Therefore, if this IC is exposed to the light, malfunction may occur.
(1)Design and mount the IC so that it won't be exposed to the light when in use.
(2)Design and mount the IC so that it won't be exposed to the light in the inspection process.
(3)Be concerned about shading of all the surfaces (front, back and side) of the IC.