

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSVI)

## TPC8120

Lithium Ion Battery Applications  
Power Management Switch Applications

- Small footprint due to small and thin package
- Low drain-source ON-resistance:  $R_{DS(ON)} = 2.6 \text{ m}\Omega$  (typ.)
- High forward transfer admittance:  $|Y_{fs}| = 80 \text{ S}$  (typ.)
- Low leakage current:  $I_{DSS} = -10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = -30 \text{ V}$ )
- Enhancement mode:  $V_{th} = -0.8 \text{ to } -2.0 \text{ V}$  ( $V_{DS} = -10 \text{ V}$ ,  $I_D = -1 \text{ mA}$ )

### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

| Characteristics   |                | Symbol    | Rating     | Unit             |
|---|----------------|-----------|------------|------------------|
| Drain-source voltage  |                | $V_{DSS}$ | -30        | V                |
| Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )        |                | $V_{DGR}$ | -30        | V                |
| Gate-source voltage   |                | $V_{GSS}$ | -25/+20    | V                |
| Drain current   | DC (Note 1)    | $I_D$     | -18        | A                |
|   | Pulse (Note 1) | $I_{DP}$  | -72        |                  |
| Drain power dissipation ( $t = 10 \text{ s}$ )<br>(Note 2a) |                | $P_D$     | 1.9        | W                |
| Drain power dissipation ( $t = 10 \text{ s}$ )<br>(Note 2b) |                | $P_D$     | 1.0        | W                |
| Single pulse avalanche energy<br>(Note 3)                   |                | $E_{AS}$  | 211        | mJ               |
| Avalanche current   |                | $I_{AR}$  | -18        | A                |
| Repetitive avalanche energy<br>(Note 2a) (Note 4)           |                | $E_{AR}$  | 0.03       | mJ               |
| Channel temperature   |                | $T_{ch}$  | 150        | $^\circ\text{C}$ |
| Storage temperature range                                   |                | $T_{stg}$ | -55 to 150 | $^\circ\text{C}$ |

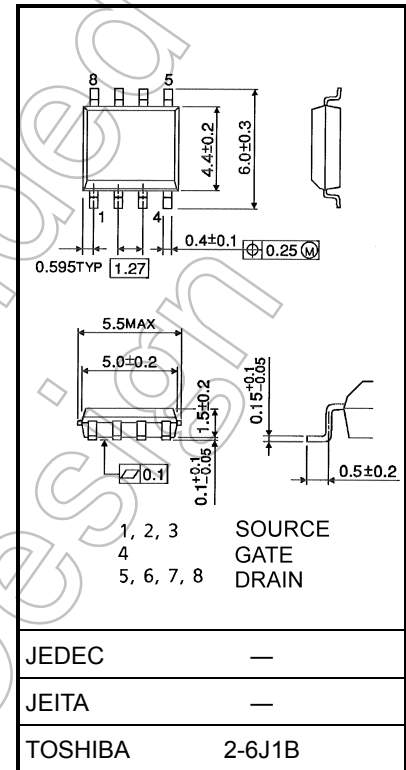
Note 1, Note 2, Note 3 and Note 4: See the next page.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

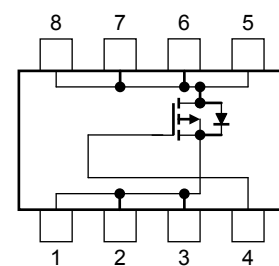
This transistor is an electrostatic-sensitive device. Handle with care.

Unit: mm



Weight: 0.080 g (typ.)

### Circuit Configuration

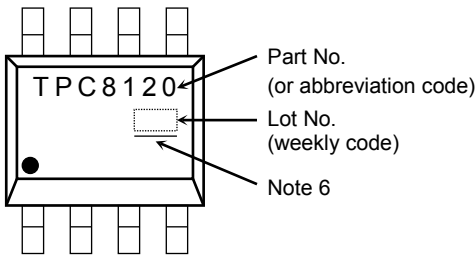


Start of commercial production  
2009-02

## Thermal Characteristics

| Characteristics   | Symbol         | Max  | Unit |
|---|----------------|------|------|
| Thermal resistance, channel to ambient<br>(t = 10 s)<br>(Note 2a) | $R_{th(ch-a)}$ | 65.8 | °C/W |
| Thermal resistance, channel to ambient<br>(t = 10 s)<br>(Note 2b) | $R_{th(ch-a)}$ | 125  | °C/W |

## Marking (Note 5)

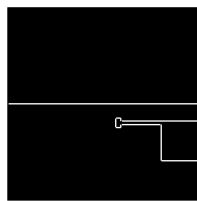


Note 6: A line under a Lot No. identifies the indication of product Labels [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

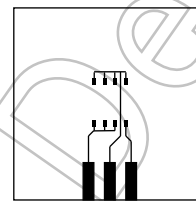
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



(a)



(b)

Note 3:  $V_{DD} = -24\text{ V}$ ,  $T_{ch} = 25^\circ\text{C}$  (initial),  $L = 500\ \mu\text{H}$ ,  $R_G = 25\ \Omega$ ,  $I_{AR} = -18\ \text{A}$

Note 4: Repetitive rating: pulse width limited by maximum channel temperature

Note 5: • on lower left of the marking indicates Pin 1.

※ Weekly code: (Three digits)



Week of manufacture

(01 for the first week of a year: sequential number up to 52 or 53)

Year of manufacture

(The last digit of a year)

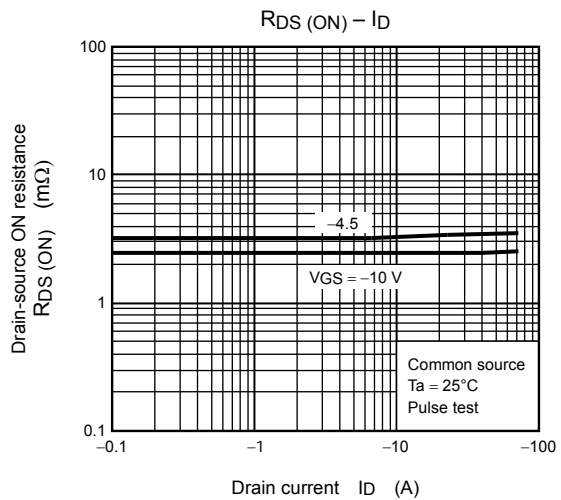
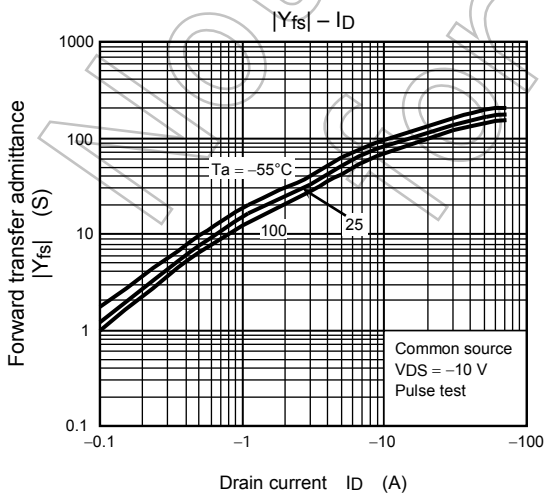
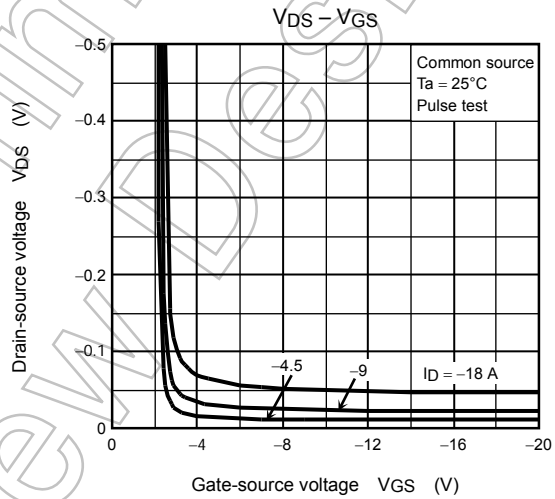
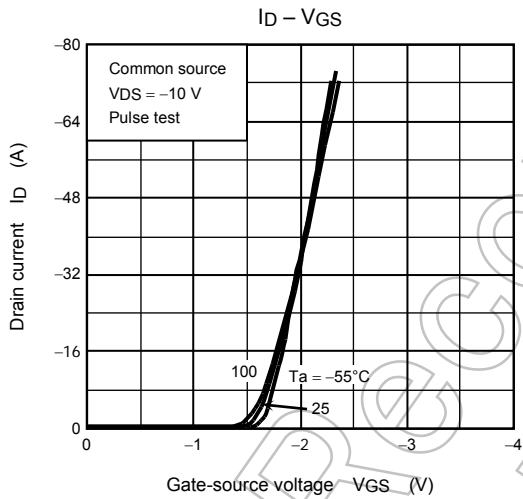
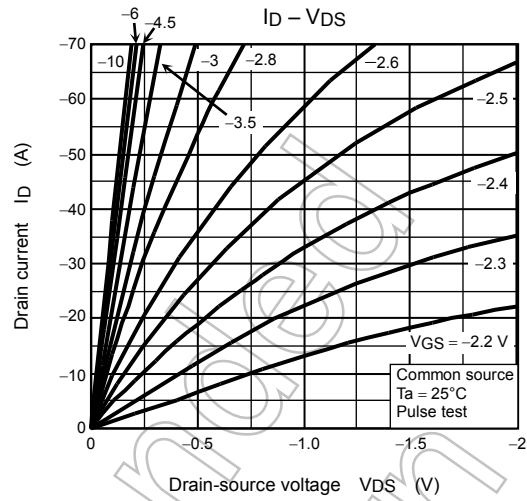
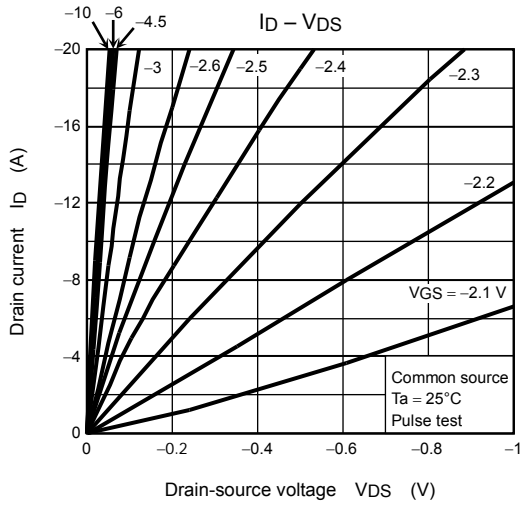
## Electrical Characteristics (Ta = 25°C)

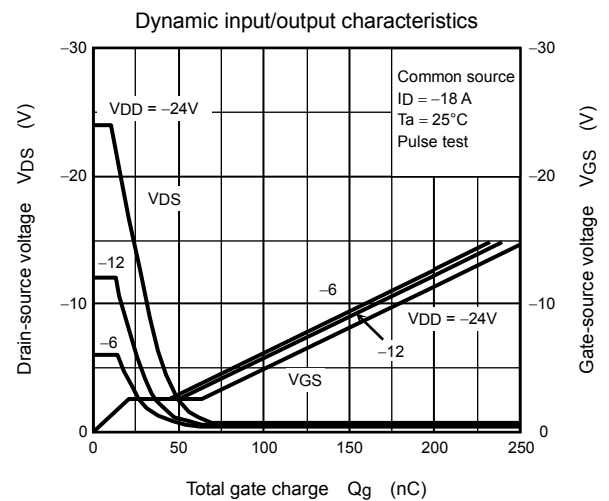
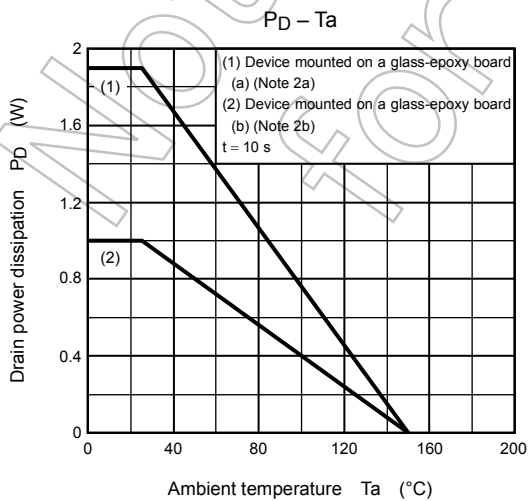
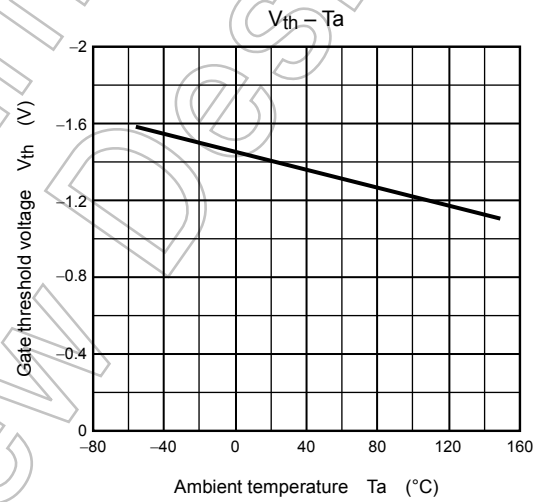
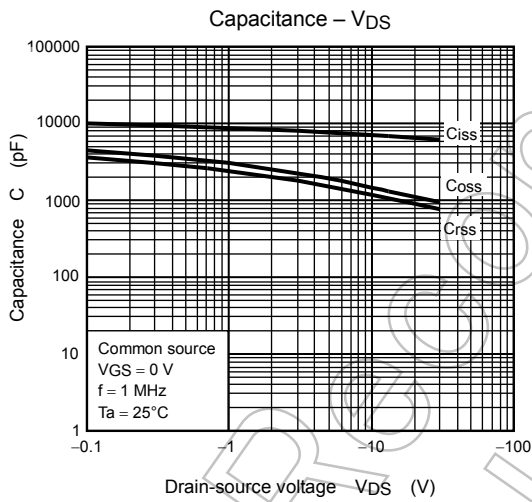
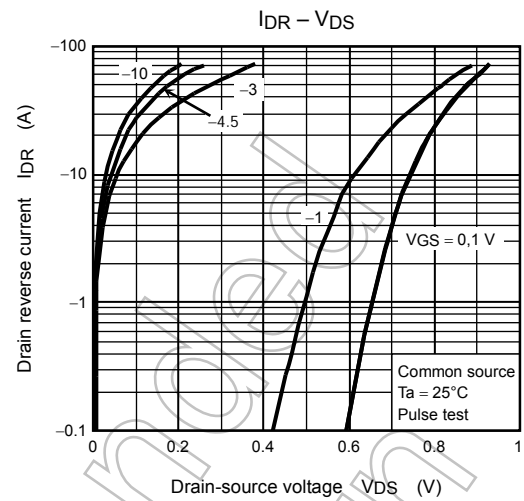
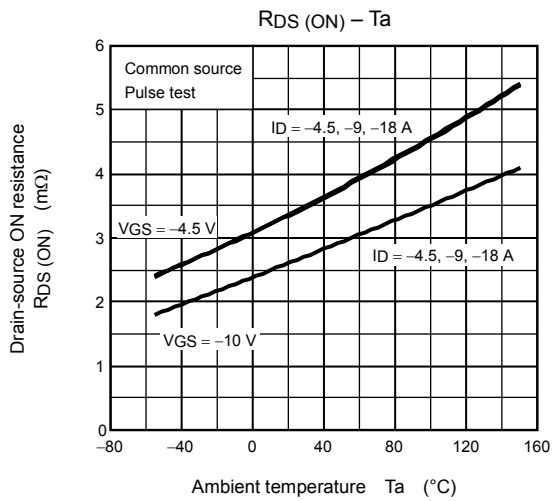
| Characteristics                                 |               | Symbol   | Test Condition                       | Min                   | Typ. | Max  | Unit |
|---|---------------|----------|--------------------------------------|-----------------------|------|------|------|
| Gate leakage current                            |               | IGSS     | VGS = ±20 V, VDS = 0 V               | —                     | —    | ±100 | nA   |
| Drain cut-OFF current                           |               | IDSS     | VDS = -30 V, VGS = 0 V               | —                     | —    | -10  | μA   |
| Drain-source breakdown voltage                  |               | V(BR)DSS | ID = -10 mA, VGS = 0 V               | -30                   | —    | —    | V    |
|   |               | V(BR)DSX | ID = -10 mA, VGS = 10V (Note 7)      | -21                   | —    | —    |      |
| Gate threshold voltage                          |               | Vth      | VDS = -10 V, ID = -1 mA              | -0.8                  | —    | -2.0 | V    |
| Drain-source ON-resistance                      |               | RDS(ON)  | VGS = -4.5 V, ID = -9 A              | —                     | 3.3  | 4.2  | mΩ   |
|   |               |          | VGS = -10 V, ID = -9 A               | —                     | 2.6  | 3.2  |      |
| Forward transfer admittance                     |               | Yfs      | VDS = -10 V, ID = -9 A               | 40                    | 80   | —    | S    |
| Input capacitance                               |               | Ciss     | VDS = -10 V, VGS = 0 V, f = 1 MHz    | —                     | 7420 | —    | pF   |
| Reverse transfer capacitance                    |               | Crss     |                                      | —                     | 1180 | —    |      |
| Output capacitance                              |               | Coss     |                                      | —                     | 1440 | —    |      |
| Switching time                                  | Rise time     | tr       |                                      | —                     | 10   | —    | ns   |
|   | Turn-ON time  | ton      |                                      | —                     | 18   | —    |      |
|   | Fall time     | tf       |                                      | —                     | 275  | —    |      |
|   | Turn-OFF time | toff     |                                      | Duty ≤ 1%, tw = 10 μs | —    | 790  |      |
| Total gate charge (gate-source plus gate-drain) |               | Qg       | VDD ≈ -24 V, VGS = -10 V, ID = -18 A | —                     | 180  | —    | nC   |
| Gate-source charge 1                            |               | Qgs1     |                                      | —                     | 20   | —    |      |
| Gate-drain ("miller") charge                    |               | Qgd      |                                      | —                     | 40   | —    |      |

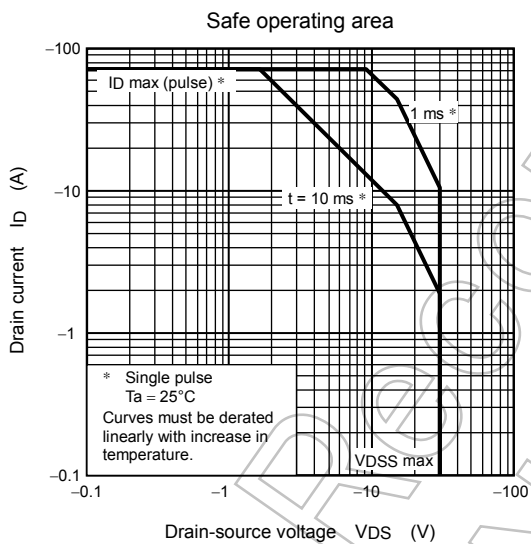
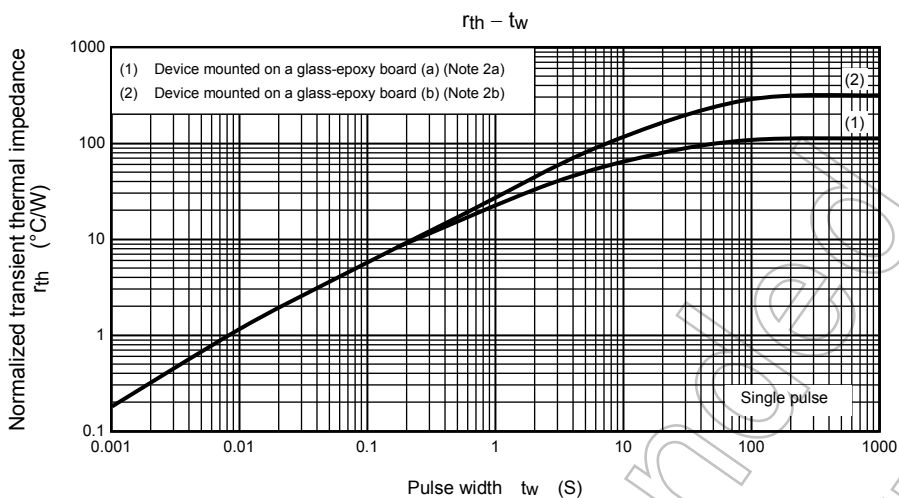
## Source-Drain Ratings and Characteristics (Ta = 25°C)

| Characteristics         |                | Symbol | Test Condition         | Min | Typ. | Max | Unit |
|-------------------------|----------------|--------|------------------------|-----|------|-----|------|
| Drain reverse current   | Pulse (Note 1) | IDRP   | —                      | —   | —    | -72 | A    |
| Forward voltage (diode) |                | VDSF   | IDR = -18 A, VGS = 0 V | —   | —    | 1.2 | V    |

Note 7: VDSX mode (the application of a plus voltage between gate and source) may cause decrease in maximum rating of drain-source voltage.







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