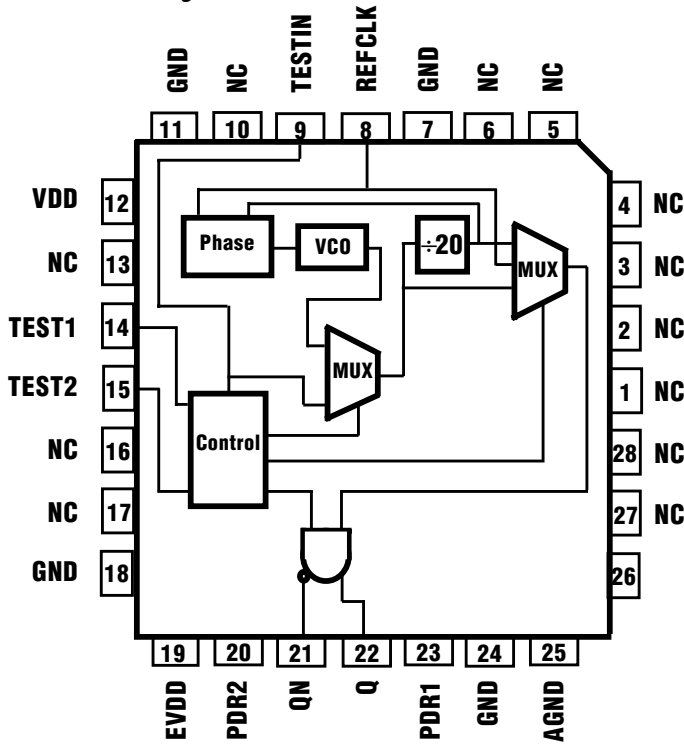


Figure 1. Pinout Diagram



TriQuint's TQ2061 is a high-frequency clock generator. It utilizes a 25 MHz to 35 MHz TTL input to generate a 500 MHz to 700 MHz PECL output. The TQ2061 has a completely self-contained Phase-Locked Loop (PLL) running at 500 MHz to 700 MHz. This stable PLL allows for a low period-to-period output jitter of 70 ps (max), and enables tight duty cycle control of 55% to 45% (worst case).

The TQ2061 provides optional 200-ohm on-chip pull-down resistors which are useful if the output is AC-coupled to the device being driven. In order to use these resistors, pin 20 (PDR2) should be connected to pin 21 (QN), and pin 23 (PDR1) should be connected to pin 22 (Q).

Various test modes on the chip simplify debug and testing of systems by slowing the clock output or by bypassing the PLL.

## TQ2061

### High-Frequency Clock Generator

#### Features

- Output frequency range:  
500 MHz to 700 MHz
- One differential PECL output:  
600 mV (min) swing
- Common-mode voltage:  
 $V_{DD} - 1.2\text{ V (max)}$ ,  
 $V_{DD} - 1.6\text{ V (min)}$
- Period-to-period output jitter:  
25 ps peak-to-peak (typ)  
70 ps peak-to-peak (max)
- Reference clock input:  
25 MHz to 35 MHz TTL-level  
crystal oscillator
- Self-contained loop filter
- Optional 200  $\Omega$  pull-down  
resistors for AC-coupled outputs
- +5 V power supply
- 28-pin J-lead surface-mount  
package
- Ideal for designs based on DEC  
Alpha AXP™ processors

Figure 2. Simplified Block Diagram

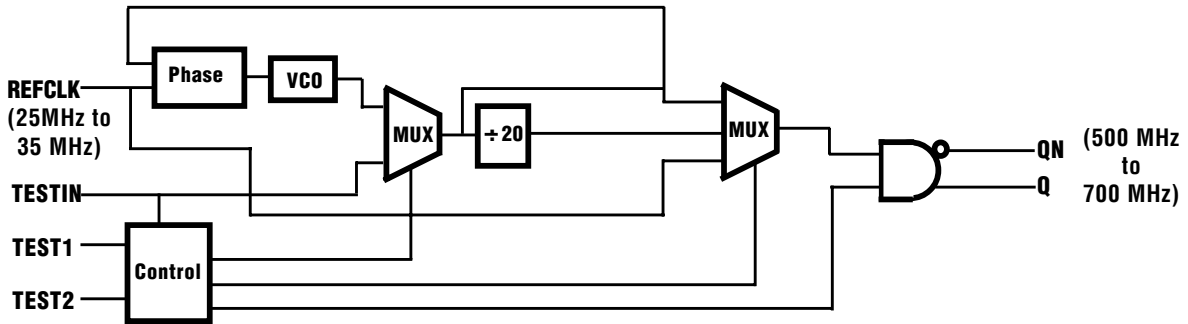
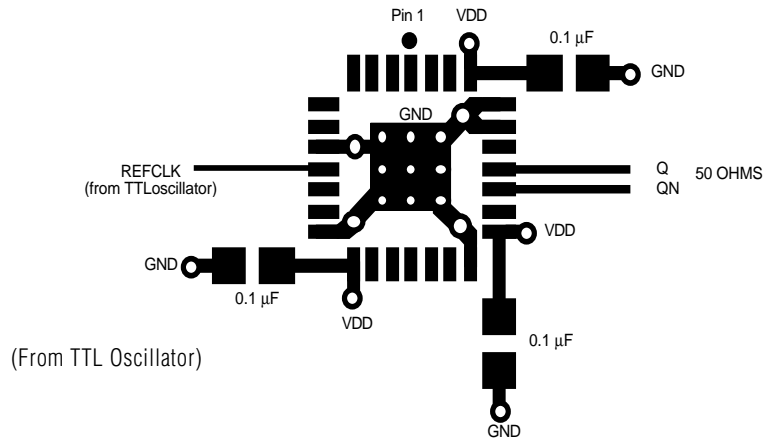


Table 1. Mode Selection

Mode	TEST1	TEST2	TESTIN <sup>1</sup>	REFCLK	Q, QN
1 (Test)	0	0	“don't care”	f <sub>REFCLK</sub>	f <sub>REFCLK</sub> <sup>2</sup>
2 (Test)	0	1	“don't care”	“don't care”	0, 1
3 (Test)	1	0	f <sub>TESTCLK</sub>	“don't care”	f <sub>TESTCLK</sub>
4 (Bypass)	1	1	0	f <sub>REFCLK</sub>	f <sub>REFCLK</sub>
5 (Normal)	1	1	1	f <sub>REFCLK</sub>	20 x f <sub>REFCLK</sub> <sup>3</sup>

Notes: 1. In mode 3, TESTIN may be used to bypass the PLL.  
 2. REFCLK = 25 MHz to 35 MHz.  
 3. Q, QN = 500 MHz to 700 MHz.

Figure 3. Recommended Layout  
 (Not to scale)



**Table 2. Absolute Maximum Ratings**

Storage Temperature	-65°C to +150°C
Ambient temperature with power applied	-55°C to +110°C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to ( $V_{DD} + 0.5$ ) V
DC input current	-30 mA to +5 mA
Package thermal resistance (MQuad)	$\theta_{JA} = 45^{\circ}\text{C/W}$
Die junction temperature	$T_J = 150^{\circ}\text{C}$

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. The device should be operated only under the DC and AC conditions shown below.

**Table 3. DC Characteristics ( $V_{DD} = +5\text{ V} \pm 5\%$ ,  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ )<sup>1</sup>**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min PECL load}$	$V_{CC} - 1.20$		$V_{CC} - 0.50$	V
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min PECL load}$	$V_{CC} - 2.00$		$V_{CC} - 1.60$	V
$V_{CMO}$	Output common mode voltage	PECL	$V_{CC} - 1.60$		$V_{CC} - 1.20$	V
$\Delta V_{OUT}$	Output differential voltage	PECL	0.6		1.2	V
$V_{IH}^2$	Input HIGH level	Guaranteed input logical HIGH Voltage for all inputs	2.0			V
$V_{IL}^2$	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
$I_{IL}$	Input LOW current	$V_{DD} = \text{Max } V_{IN} = 0.40\text{ V}$		-150	-400	$\mu\text{A}$
$I_{IH}$	Input HIGH current	$V_{DD} = \text{Max } V_{IN} = 2.7\text{ V}$		0	25	$\mu\text{A}$
$I_I$	Input HIGH current	$V_{DD} = \text{Max } V_{IN} = 5.3\text{ V}$		2	1000	$\mu\text{A}$
$I_{DDs}^3$	Power supply current	$V_{DD} = \text{Max}$		85	120	mA
$V_I$	Input clamp voltage	$V_{DD} = \text{Min } I_{IN} = -18\text{ mA}$		-0.70	-1.2	V

**Table 4. Capacitance**

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 2.0\text{ V}$ at $f = 1\text{ MHz}$		6		pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 2.0\text{ V}$ at $f = 1\text{ MHz}$		9		pF

Notes: 1. Typical limits are at  $V_{DD} = 5.0\text{ V}$  and  $T_A = 25^{\circ}\text{C}$ .

2. These are absolute values with respect to device ground and include all overshoots due to system or tester noise.

3. This parameter is measured with device not switching and unloaded.

# TQ2061

**Table 5. AC Characteristics** ( $V_{DD} = +5\text{ V} \pm 5\%$ ,  $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ )

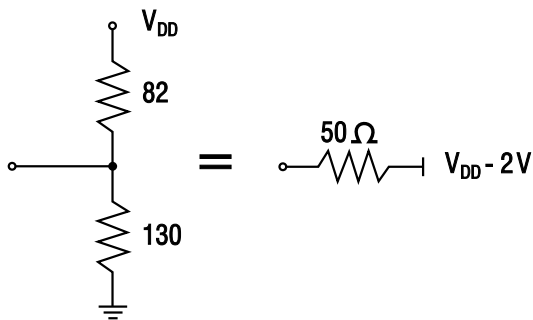
Symbol	Input Clock (REFCLK)	Test Conditions (Figure 5)	Min	Typ	Max	Unit
$t_{CPWH}$	CLK pulse width HIGH	Figure 5	4	—	—	ns
$t_{CPWL}$	CLK pulse width LOW	Figure 5	4	—	—	ns
$t_{IR}$	Input rise time (0.8 V – 2.0 V)		—	—	2.0	ns

Symbol	Output Clock (Q, QN)	Test Conditions (Figures 4 & 5) <sup>1</sup>	Min	Typ	Max	Unit
$t_{OR}, t_{OF}$	Rise/fall time (20% – 80%)	Figure 5	100	220	350	ps
$t_{CYC}$	Duty-cycle	Figure 5	45	50	55	%
$t_{JP}^2$	Period-to-Period Jitter		—	25	70	ps
$t_{SYNC}^3$	Synchronization Time		—	10	500	$\mu\text{s}$

- Notes: 1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).  
 2. Jitter specification is peak to peak. Period-to-Period jitter is the jitter on the output with respect to the output's previous crossing.  
 3.  $t_{SYNC}$  is the time required for the PLL to synchronize and assumes the presence of a CLK signal.

**Figure 4. PECL Test Load**



**Figure 5. REFCLK and Q-QN Timing**

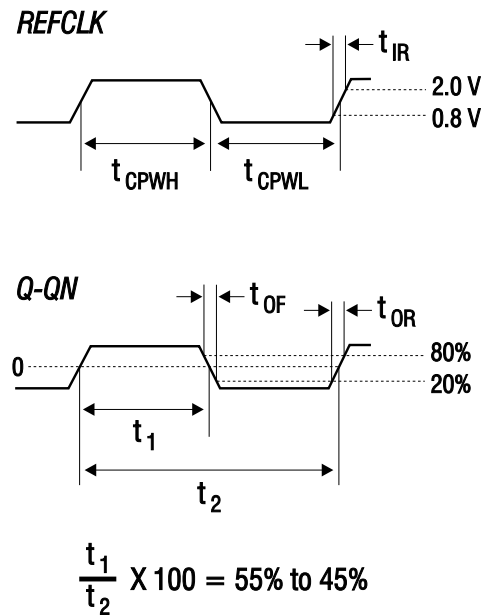
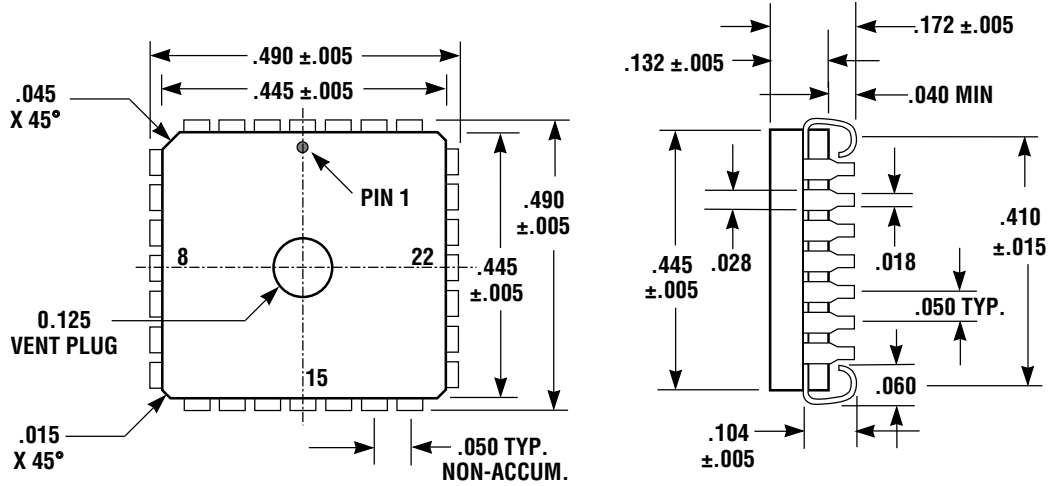


Figure 6. 28-Pin MQuad J-Leaded Package Mechanical Specification



(All dimensions in inches)

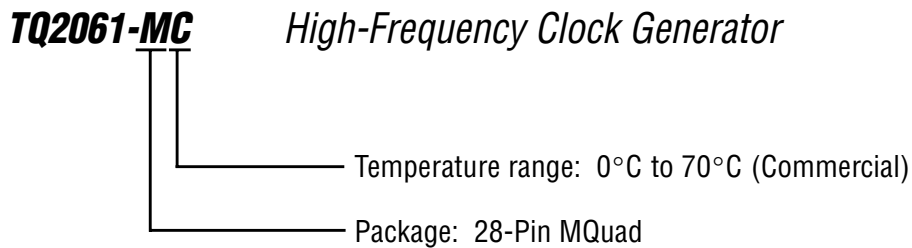
Table 6. 28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O	Pin #	Pin Name	Description	I/O
1	NC	No Connect	—	15	TEST2	Test Control 2	I
2	NC	No Connect	—	16	NC	No Connect	—
3	NC	No Connect	—	17	NC	No Connect	0
4	NC	No Connect	—	18	GND	Ground	—
5	NC	No Connect	—	19	EVDD	VDD for ECL Output (+5 V)	—
6	NC	No Connect	—	20	PDR2	Pull-down Resistor 2 (200 Ω)	I
7	GND	Ground	—	21	QN	Differential PECL Output (-)	0
8	REFCLK	Reference Clock	I	22	Q	Differential PECL Output (+)	0
9	TESTIN	Test Input	I	23	PDR1	Pull-down Resistor 1 (200 Ω)	I
10	NC	No Connect	—	24	GND	Ground	—
11	GND	Logic Ground	—	25	AGND	Analog Ground	—
12	VDD	Logic VDD (+5 V)	—	26	AVDD	Analog VDD (+5 V)	—
13	NC	No Connect	—	27	NC	No Connect	—
14	TEST1	Test Control 1	I				

SYSTEM TIMING PRODUCTS

***Ordering Information***

To order, please specify as shown below:



***Additional Information***

For latest specifications, additional product information,  
worldwide sales and distribution locations, and information about TriQuint:

**Web:** [www.triquint.com](http://www.triquint.com)      **Tel:** (503) 615-9000  
**Email:** [sales@tqs.com](mailto:sales@tqs.com)      **Fax:** (503) 615-8900

For technical questions and additional information on specific applications:

**Email:** [applications@tqs.com](mailto:applications@tqs.com)

The information provided herein is believed to be reliable; TriQuint assumes no liability for inaccuracies or omissions. TriQuint assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. TriQuint does not authorize or warrant any TriQuint product for use in life-support devices and/or systems.

Copyright © 1997 TriQuint Semiconductor, Inc. All rights reserved.

Revision 1.0.A      October 1997