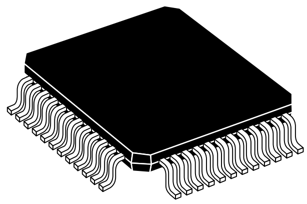
TSL1014

14 + 1 channel buffers for TFT-LCD panels

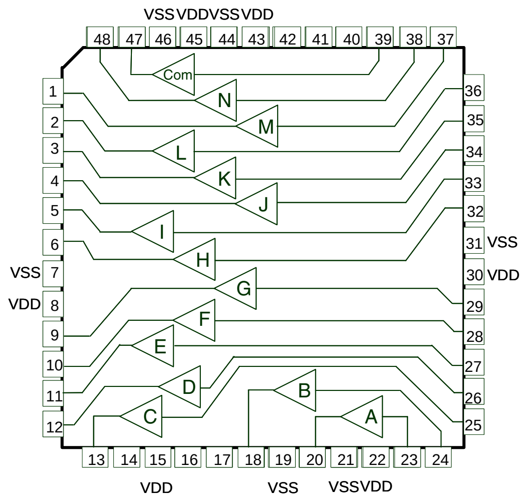
Features

- Wide supply voltage: 5.5 V to 16.8 V
- Low operating current: 6 mA typical at 25° C
- Gain bandwidth product: 1 MHz
- High current com amplifier: ±100 mA output current
- Industrial temperature range: -40° C to +85° C
- Small package: TQFP48
- Automotive qualification



7 x 7mm TQFP48

Pin connections (top view)



Application

- TFT liquid crystal display (LCD)

Description

The TSL1014 is composed of 14 + 1 channel buffers which are used to buffer the reference voltage for gamma correction in thin film transistor (TFT) liquid crystal displays (LCD).

One "COM" amplifier is able to deliver high output current value, up to ±100mA. Amplifiers A and B feature positive single supply inputs for common mode voltage behavior. The amplifiers C to N inclusive, and the COM amplifier, feature negative single-supply inputs and are dedicated to the highest and lowest gamma voltages.

The TSL1014 is fully characterized and guaranteed over a wide industrial temperature range (-40 to +85° C).

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (V_{DD}-V_{SS})	18	V
V_{IN}	Input voltage	V_{SS} -0.5V to V_{DD} +0.5V	V
I_{OUT}	Output current (A to N buffers) Output current (Com buffer)	30 100	mA
I_{SC}	Short circuit current (A to N buffers) Short circuit current (Com buffer)	±120 ±300	mA
P_D	Power dissipation(1) for TQFP48	1470	mW
R_{THJA}	Thermal resistance junction to ambient for TQFP48	85	°C/W
T_{LEAD}	Lead temperature (soldering 10 seconds)	260	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
ESD	Human body model (HBM) (2)	2000	V
	Machine model (MM) (3)	200	
	Charged device model (CDM) (4)	1500	

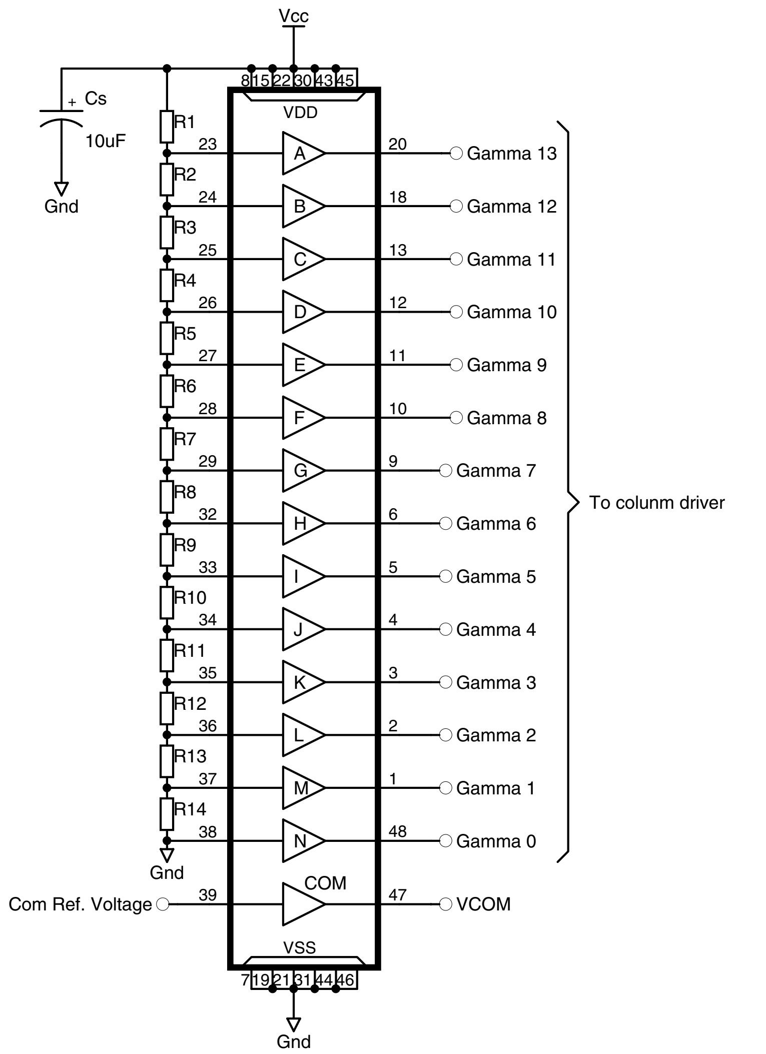
1. P_D is calculated with T_{amb} = 25° C, T_J = 150° C and R_{THJA} = 85° C/W for the TQFP48 package.
2. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
3. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
4. Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to the ground through only one pin.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (V_{DD}-V_{SS})	5.5 to 16.8	V
T_{amb}	Ambient temperature	-40 to +85	°C
V_{IN}	Input voltage (Buffers A & B)	V_{SS} +1.5V to V_{DD}	V
	Input voltage (Buffers C to N + COM)	V_{SS} to V_{DD} -1.5V	

2 Typical application schematics

Figure 1. A typical application schematic for the TSL1014



Note that:

- Amplifiers **A** & **B** have their input voltage in the range V_{SS}+1.5 V to V_{DD}. This is why they must be used for high level gamma correction voltages.
- Amplifiers **C to N** have their input voltage in the range V_{SS} to V_{DD}-1.5 V. This is why they must be used for medium-to-low level gamma correction voltages.
- Amplifier COM has its input voltage range from V_{SS} to V_{DD}-1.5 V.

3 Electrical characteristics

Table 3. Electrical characteristics for TSL1014IF/TSL1014IFT
T_{amb} = 25°C, V_{DD} = +5V, V_{SS} = -5V, R_L = 10kΩ, C_L = 10pF (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IO}	Input offset voltage	V_{ICM} = 0V			12	mV
ΔV_{IO}	Input offset voltage drift	$T_{Min} < T_{amb} < T_{Max}$		5		µV/°C
I_{IB}	Input bias current	V_{ICM} = 0V, buffers A & B V_{ICM} = 0V, buffers C to N & COM			140 70	nA
R_{IN}	Input impedance			1		GΩ
C_{IN}	Input capacitance			1.35		pF
V_{OL}	Output voltage low	I_{OUT} = -5mA Buffers C to L Buffers M, N & COM		-4.85 -4.92	-4.80 -4.85	V
V_{OH}	Output voltage high	I_{OUT} = 5mA for positive single-supply buffers (A & B)	4.82	4.87		V
I_{OUT}	Output current	(A to N buffers)		±30		mA
		Com buffer		±100		
PSRR	Power supply rejection ratio	V_{CC}= 6.5 to 15.5V	80	100		dB
I_{CC}	Supply current	No load		6	8.4	mA
SR	Slew rate (rising & falling edge)	-4V < V_{OUT} < +4V 20% to 80%		1		V/µs
t_s	Settling time	Settling to 0.1%, V_{OUT}=2V step		5		µs
BW	Bandwidth at -3dB	R_L=10kΩ, C_L=10pF		2		MHz
G_m	Phase margin	R_L=10kΩ, C_L=10pF		60		degrees
C_s	Channel separation	f=1MHz		75		dB

Note: Limits are 100% production tested at 25°C. Behavior at the temperature range limits is guaranteed through correlation and by design.

Table 4. Electrical characteristics for TSL1014IYF/TSL1014IYFT (automotive grade)
T_{amb} = 25°C, V_{DD} = +5V, V_{SS} = -5V, R_L = 10kΩ, C_L = 10pF (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IO}	Input offset voltage	V_{ICM} = 0V $T_{Min} < T_{amb} < T_{Max}$			12	mV
ΔV_{IO}	Input offset voltage drift	$T_{Min} < T_{amb} < T_{Max}$		5		µV/°C
I_{IB}	Input bias current	V_{ICM} = 0V, buffers A & B $T_{Min} < T_{amb} < T_{Max}$ V_{ICM} = 0V, buffers C to N & COM $T_{Min} < T_{amb} < T_{Max}$			140 280 70 140	nA
R_{IN}	Input impedance			1		GΩ
C_{IN}	Input capacitance			1.35		pF
V_{OL}	Output voltage low	I_{OUT} = -5mA Buffers C to L $T_{Min} < T_{amb} < T_{Max}$ Buffers M, N & COM $T_{Min} < T_{amb} < T_{Max}$		-4.85 -4.92	-4.80 -4.76 -4.85 -4.83	V
V_{OH}	Output voltage high	I_{OUT} = 5mA for positive single-supply buffers (A & B) $T_{Min} < T_{amb} < T_{Max}$	4.82 4.80	4.87		V
I_{OUT}	Output current	(A to N buffers)		±30		mA
		Com buffer		±100		
PSRR	Power supply rejection ratio	V_{CC}= 6.5 to 15.5V $T_{Min} < T_{amb} < T_{Max}$	 80	100		dB
I_{CC}	Supply current	No load $T_{Min} < T_{amb} < T_{Max}$		6	8.4 9	mA
SR	Slew rate (rising & falling edge)	-4V < V_{OUT} < +4V 20% to 80%		1		V/µs
t_s	Settling time	Settling to 0.1%, V_{OUT}=2V step		5		µs
BW	Bandwidth at -3dB	R_L=10kΩ, C_L=10pF		2		MHz
G_m	Phase margin	R_L=10kΩ, C_L=10pF		60		degrees
C_s	Channel separation	f=1MHz		75		dB

Note: *Limits are 100% production tested at 25°C. Behavior at the temperature range limits is guaranteed through correlation and by design.*

Figure 2. Supply current vs. supply voltage for various temperatures

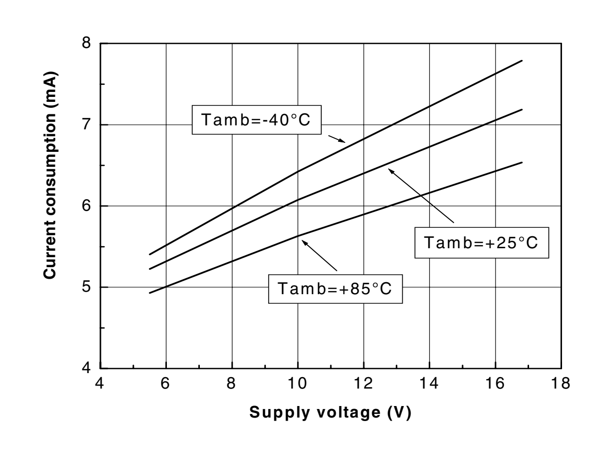


Figure 3. Output offset voltage (eq. V_{IO}) vs. temperature

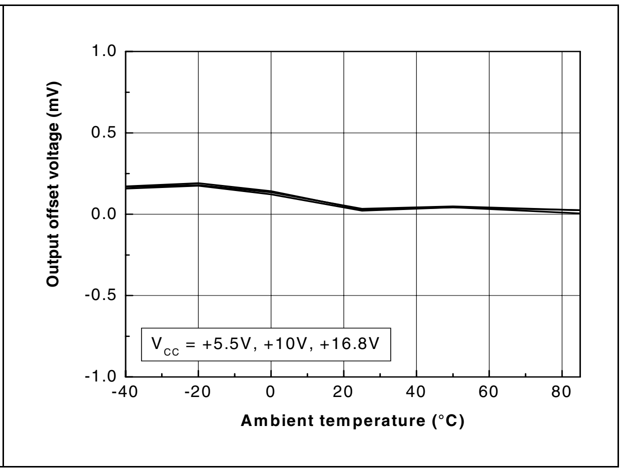


Figure 4. Input current (I_{IB}) vs. temperature

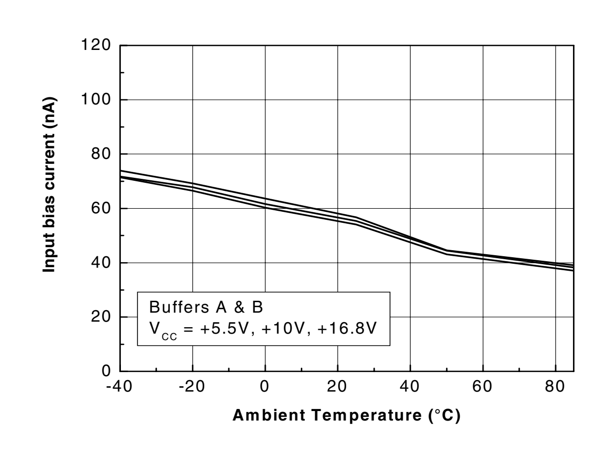


Figure 5. Input current (I_{IB}) vs. temperature

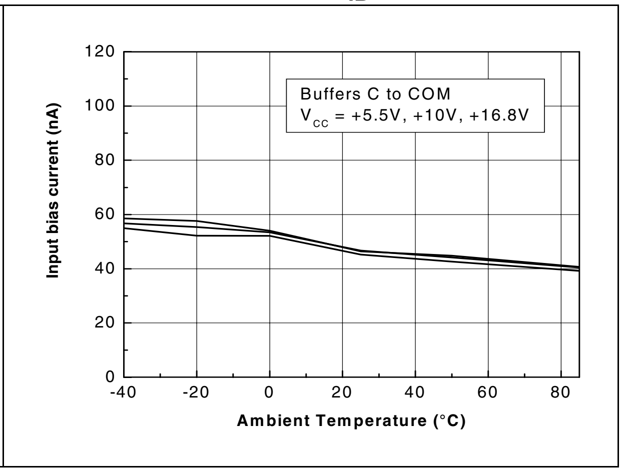


Figure 6. Output current capability vs. temperature

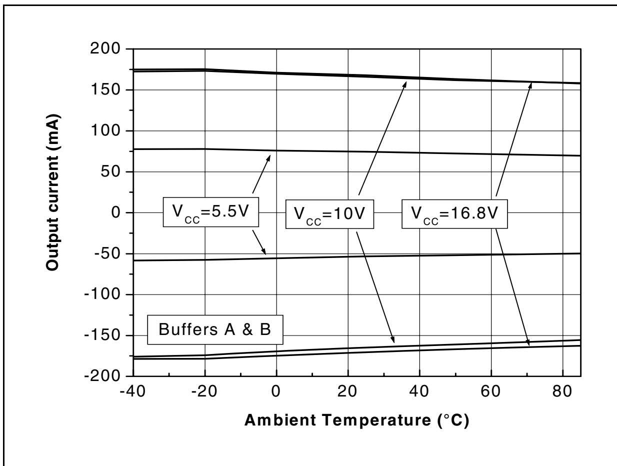


Figure 7. Output current capability vs. temperature

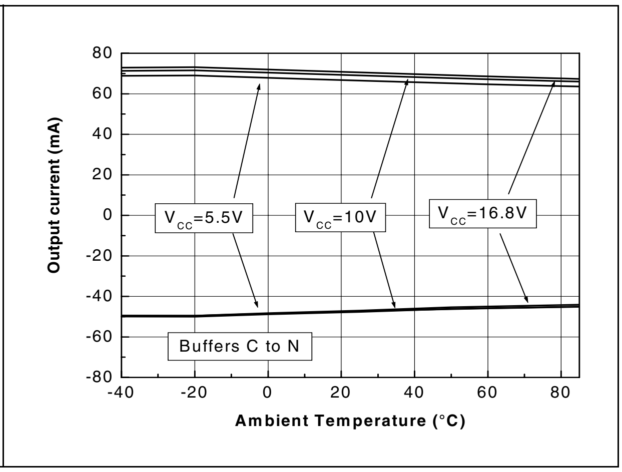


Figure 8. Output current capability vs. temperature

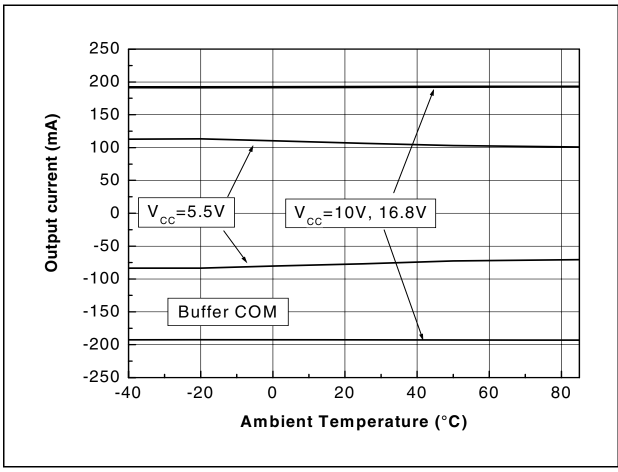


Figure 9. High level voltage drop vs. temperature

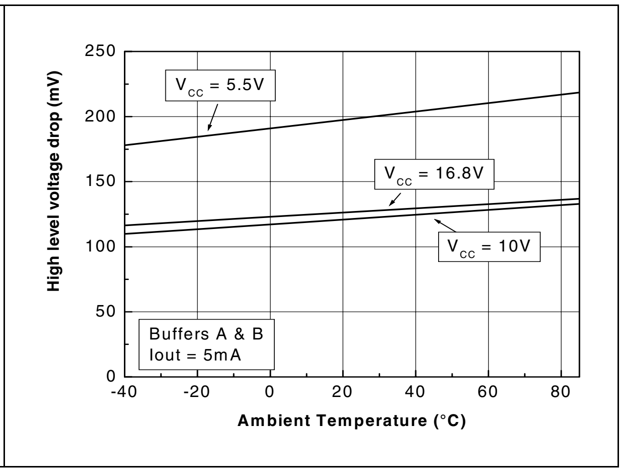


Figure 10. Low level voltage drop vs. temperature

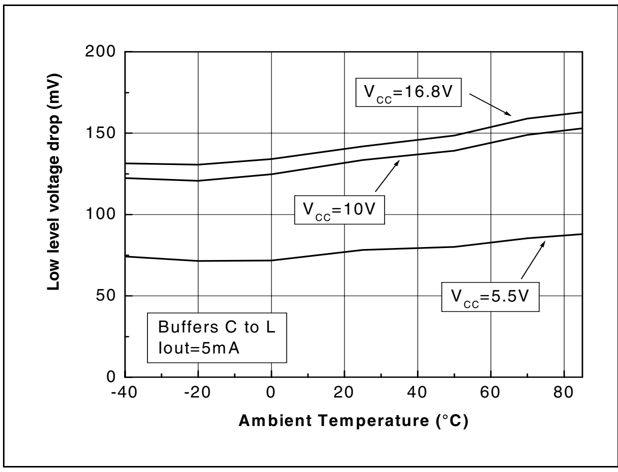


Figure 11. Low level voltage drop vs. temperature

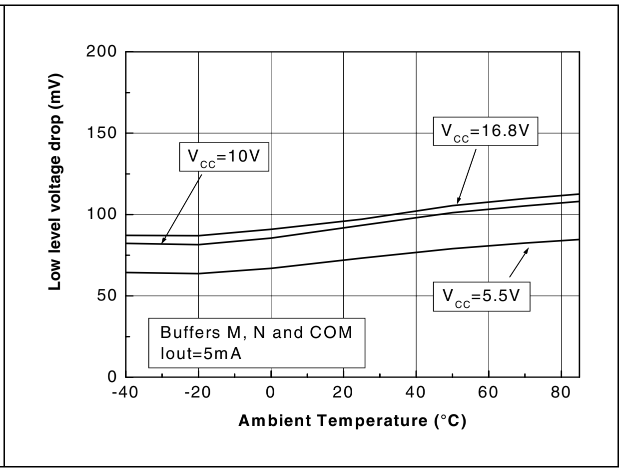


Figure 12. Voltage output high (V_{OH}) vs. output current - Buffers A & B

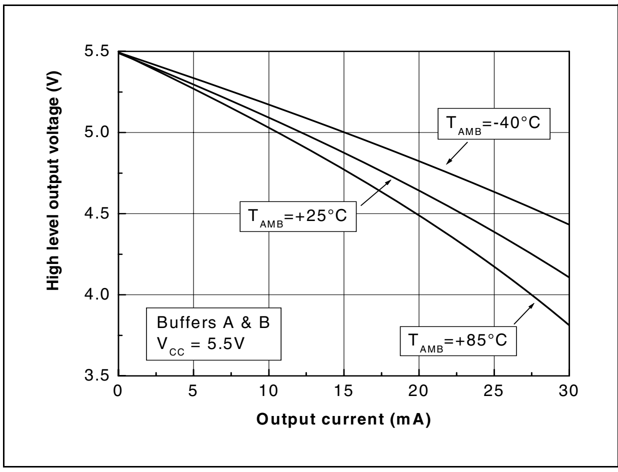


Figure 13. Voltage output high (V_{OH}) vs. output current - Buffers A & B

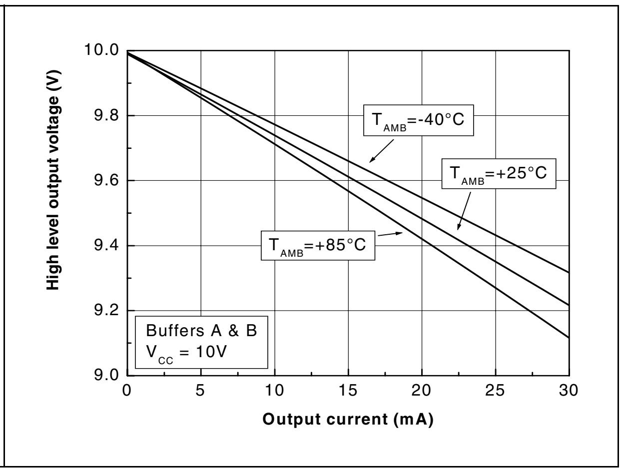


Figure 14. Voltage output high (V_{OH}) vs. output current - Buffers A & B

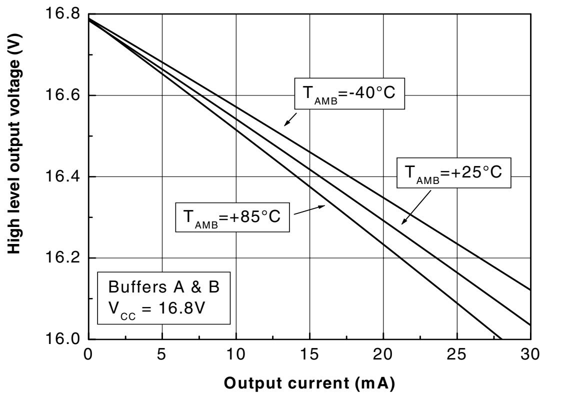


Figure 15. Voltage output low (V_{OL}) vs. output current - Buffers C to L

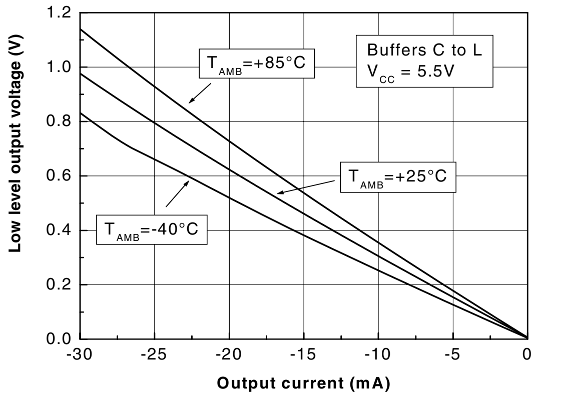


Figure 16. Voltage output low (V_{OL}) vs. output current - Buffers C to L

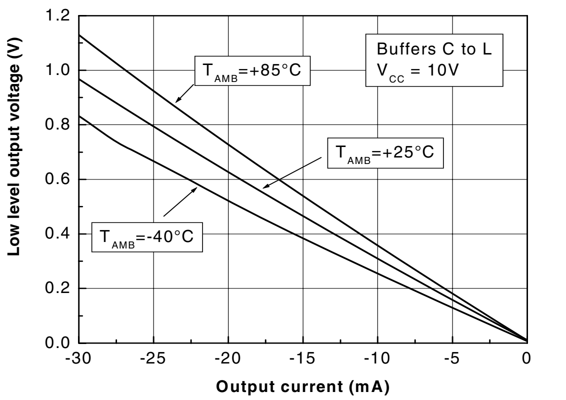


Figure 17. Voltage output low (V_{OL}) vs. output current - Buffers C to L

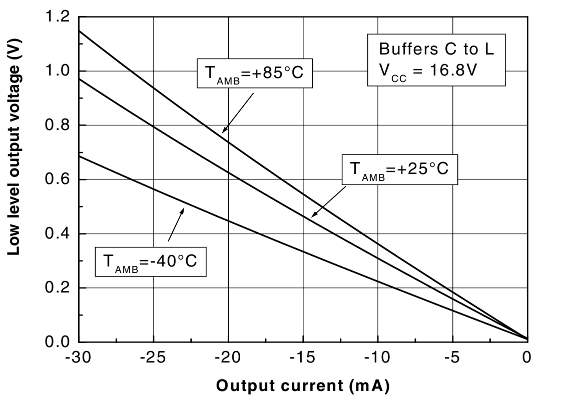


Figure 18. Voltage output low (V_{OL}) vs. output current - Buffers M, N & COM

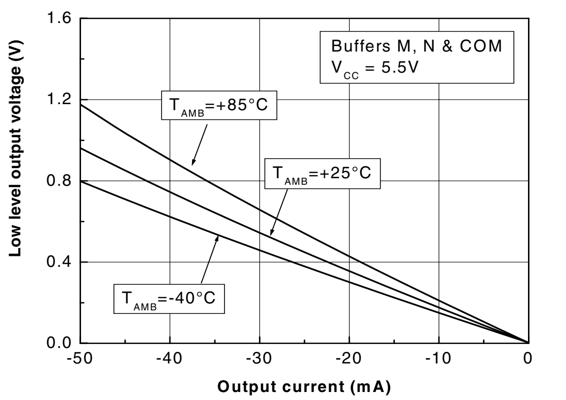


Figure 19. Voltage output low (V_{OL}) vs. output current - Buffers M, N & COM

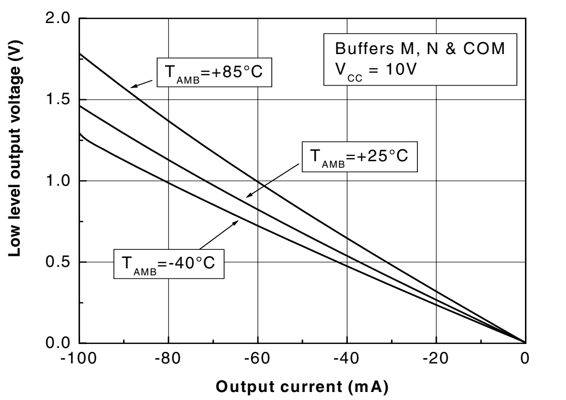


Figure 20. Voltage output low (V_{OL}) vs. output current - Buffers M, N & COM

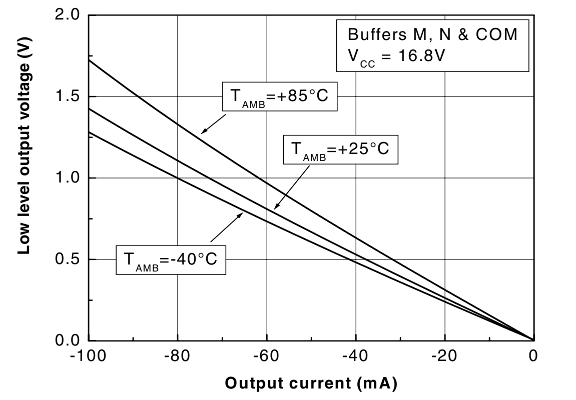


Figure 21. Positive slew rate vs. temperature

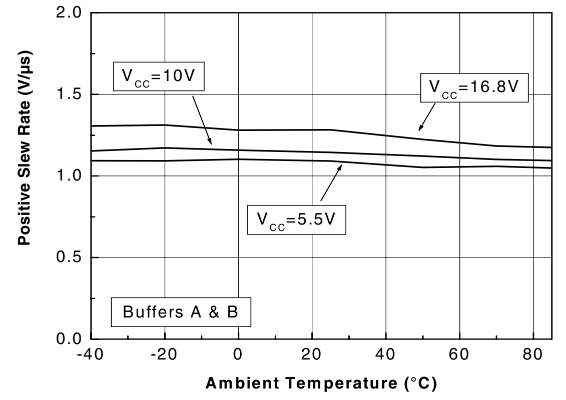


Figure 22. Positive slew rate vs. temperature

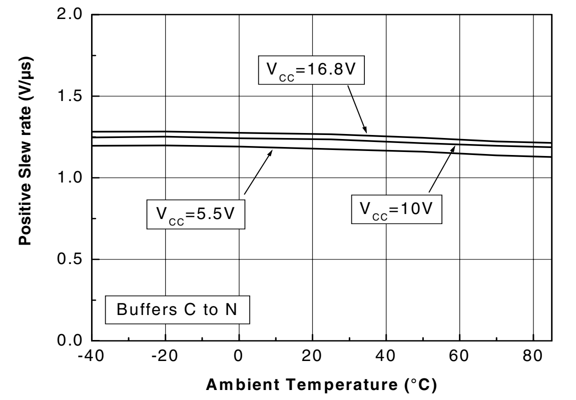


Figure 23. Positive slew rate vs. temperature

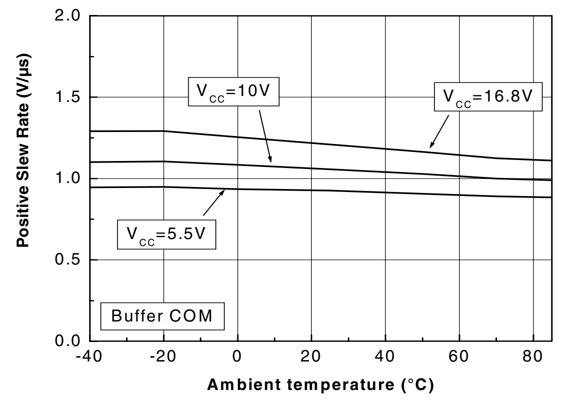


Figure 24. Negative slew rate vs. temperature

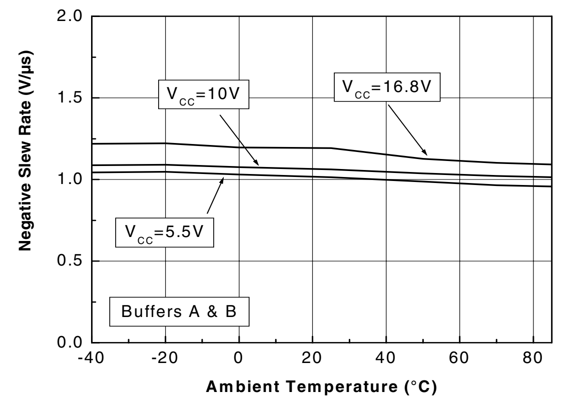


Figure 25. Negative slew rate vs. temperature

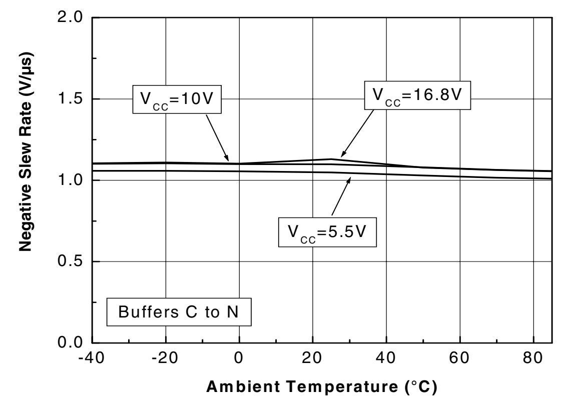


Figure 26. Negative slew rate vs. temperature

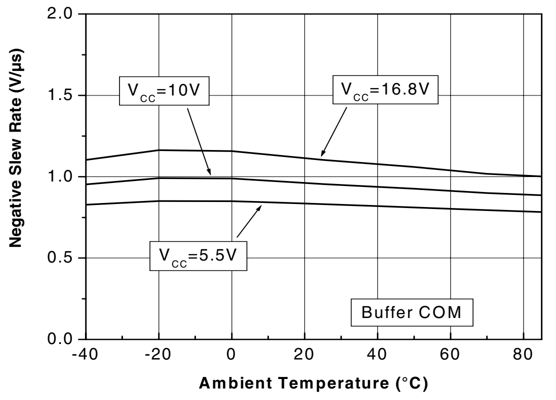


Figure 27. Large signal response - buffers A & B

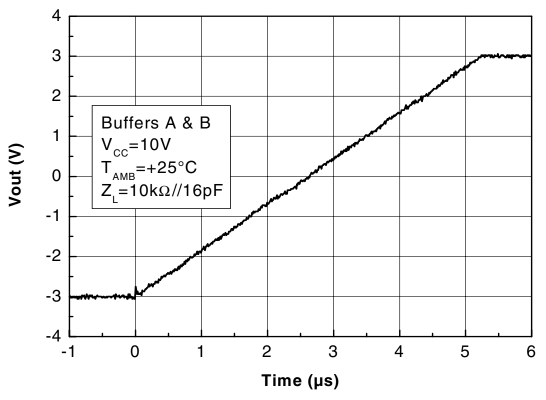


Figure 28. Large signal response - buffers A & B

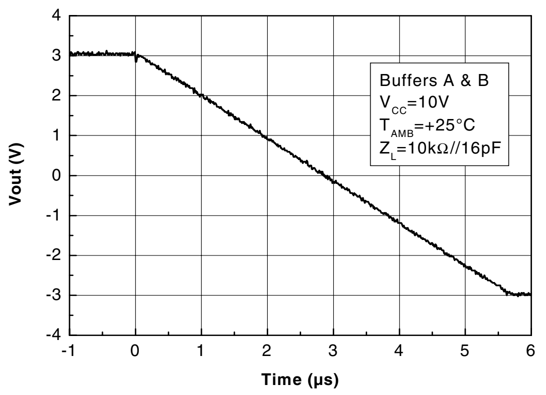


Figure 29. Large signal response - buffers C to N

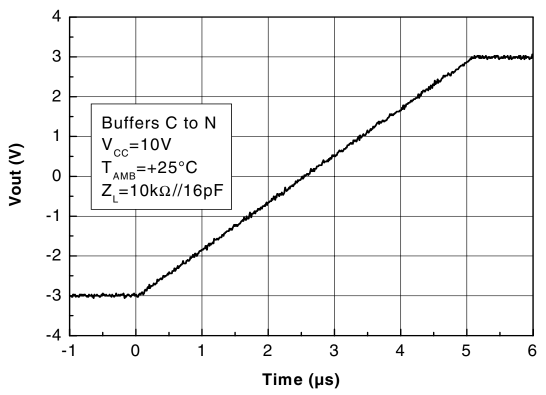


Figure 30. Large signal response - buffers C to N

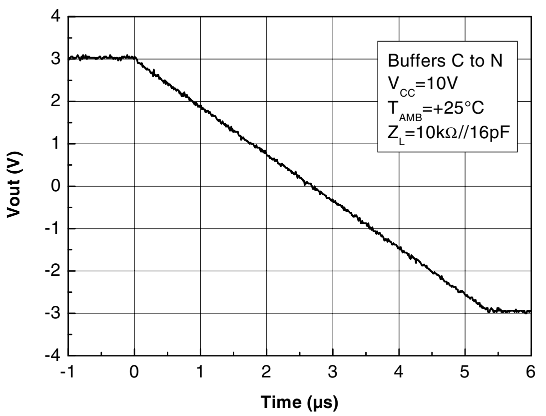


Figure 31. Large signal response - buffer COM

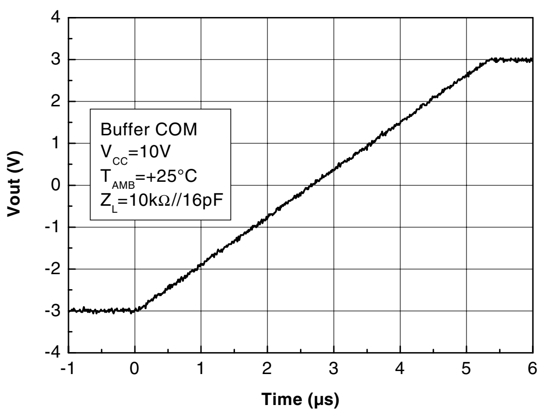


Figure 32. Large signal response - buffer COM

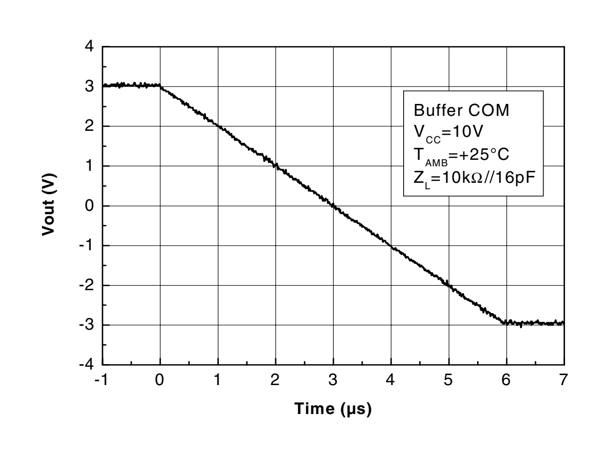


Figure 33. Small signal response - buffers A & B

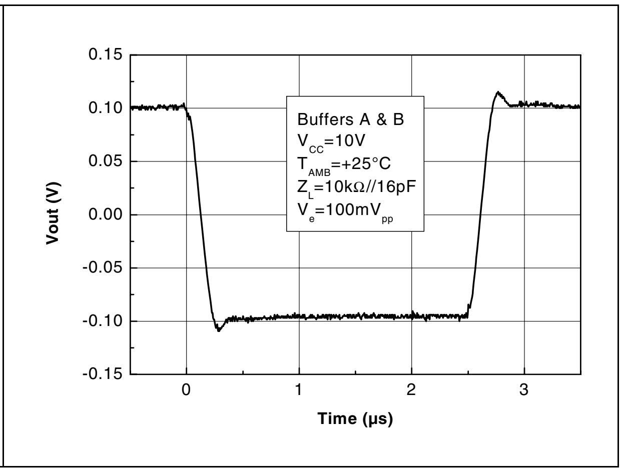


Figure 34. Small signal response - buffers C to N

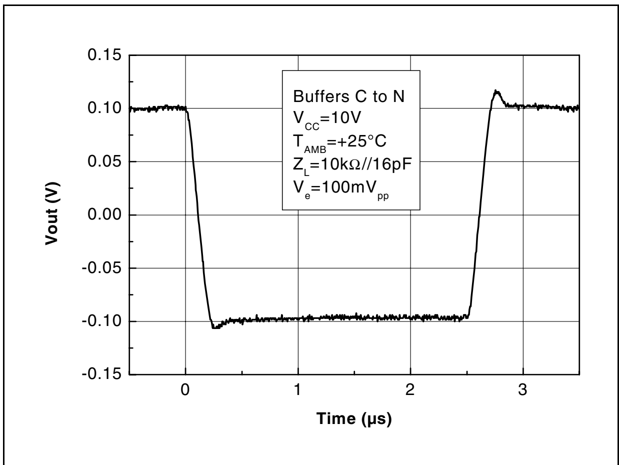


Figure 35. Small signal response - buffer COM

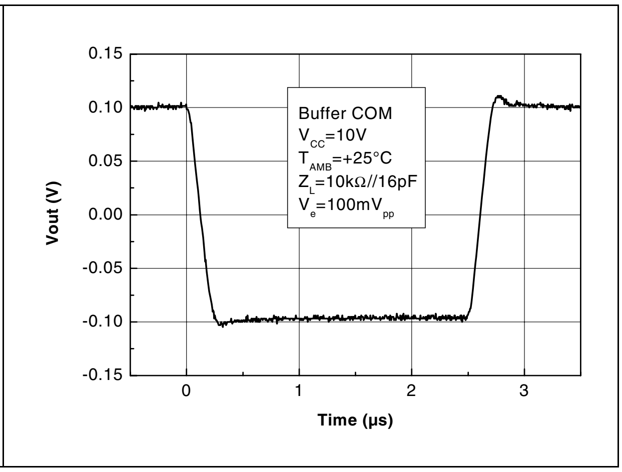


Figure 36. Output voltage response to current transient - buffers A & B

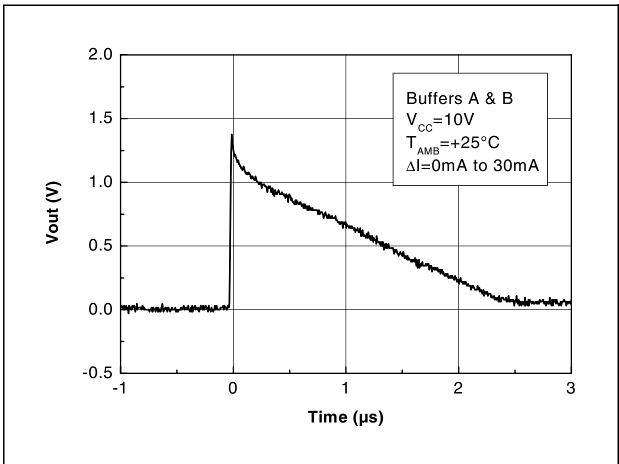


Figure 37. Output voltage response to current transient - buffers A & B

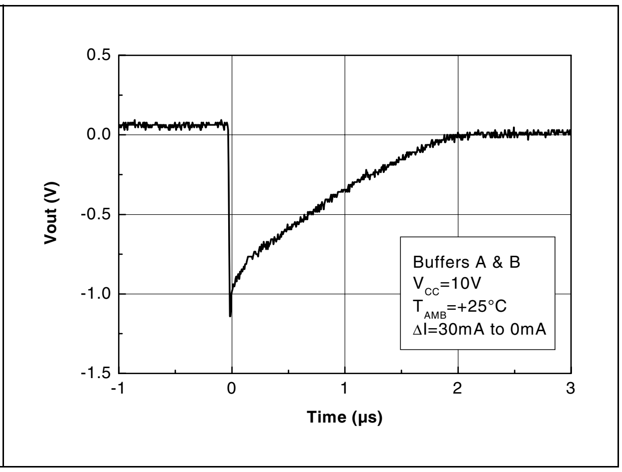


Figure 38. Output voltage response to current transient - buffers C to N

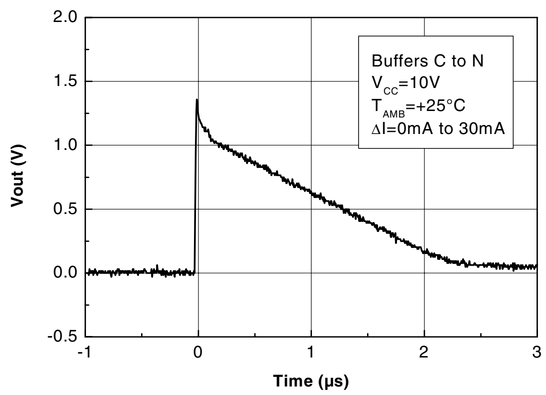


Figure 39. Output voltage response to current transient - buffers C to N

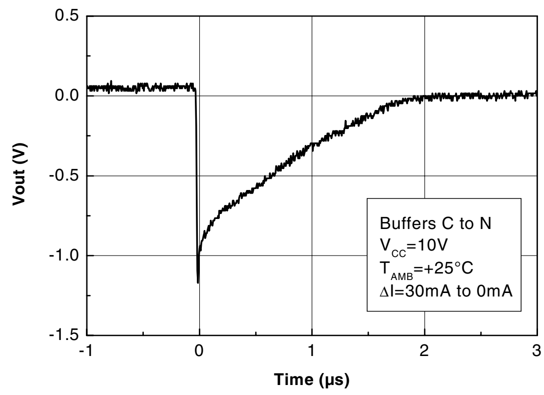


Figure 40. Output voltage response to current transient - buffer COM

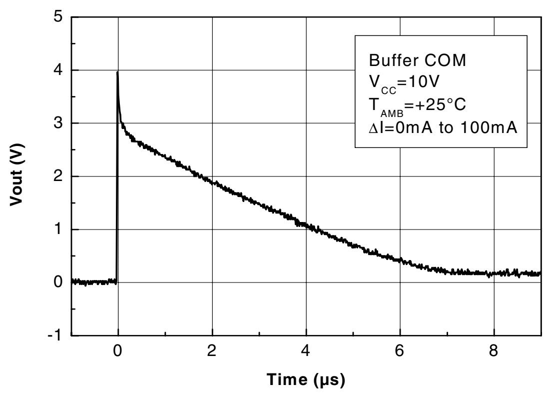


Figure 41. Output voltage response to current transient - buffer COM

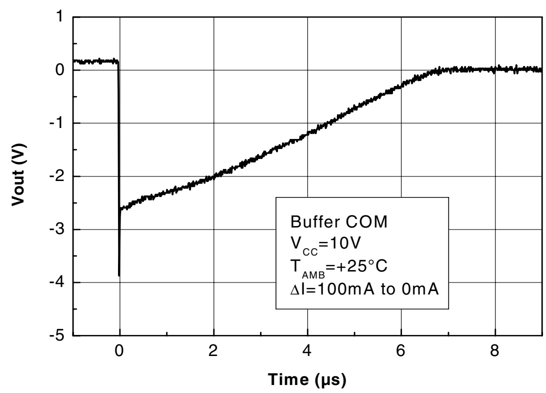


Figure 42. Output voltage response to current transient - buffer COM

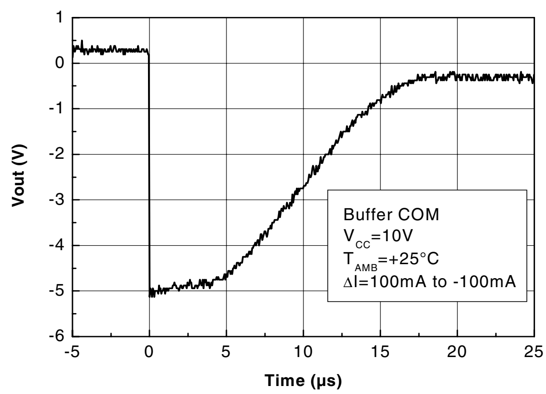
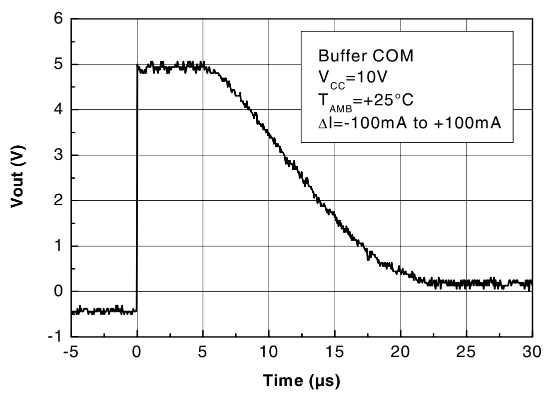


Figure 43. Output voltage response to current transient - buffer COM

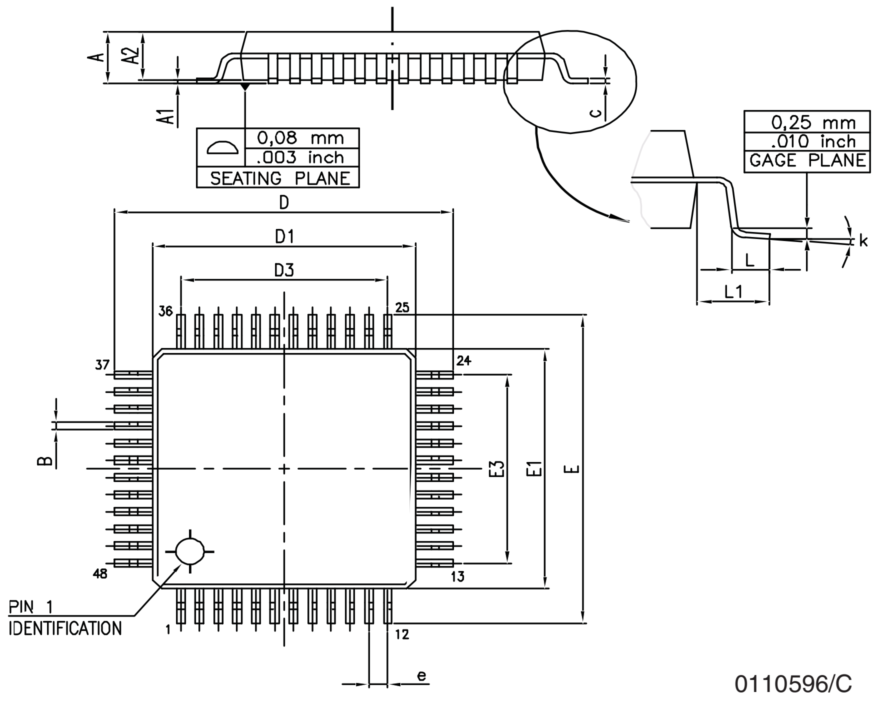


4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Table 5. TQFP48 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.6			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.0035		0.0079
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.020	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°	3.5°	7°	0°	3.5°	7°



5 Ordering information

Table 6. Order codes

Order code	Temperature range	Package	Packing	Marking
TSL1014IF	-40°C to +85°C	TQFP48	Tray	SL1014I
TSL1014IFT			Tape & reel	
TSL1014IYF(1)			Tray	SL1014Y
TSL1014IYFT(1)			Tape & reel	

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
01-Jul-2005	1	Initial release - Product in full production.
01-Sep-2005	2	Lead temperature corrected in *Table 1 on page 2*. Electrical characteristics graphs re-ordered from *Figure 2 on page 6* to *Figure 43 on page 12*.
07-Mar-2007	3	Notes added on ESD in *Table 1 on page 2*. Maximum operating supply voltage increased in *Table 2 on page 2*. Input voltage parameters added in *Table 2 on page 2*. V_{OL} limits changed for Buffers C to L in *Table 4 on page 5*.
09-Jun-2008	4	Electrical characteristics table added for automotive parts. Order codes added for automotive parts.
19-Aug-2008	5	Modified I_{CC} typical and maximum values for standard parts in *Table 3*. Updated all curves (*Figure 2* to *Figure 43*). Added ESD charged device model value in *Figure 1*.