

## PWM Power Control for DC Loads

### Description

The U2352B bipolar circuit is a PWM device for controlling logic level Power MOSFETs and IGBTs. It allows simple power control for dc loads. Integrated load current monitoring with adjustable switch-off threshold also

gives the option of measuring the load current via the MOS transistor's on-state resistance,  $R_{DS(on)}$ , or via a shunt resistor.

### Special Features

- Pulse width control up to 50 kHz clock frequency
- Load current monitoring via the on-state resistance,  $R_{DS(on)}$ , of the FET or via shunt resistor (optional)
- 100 mA push-pull output stage
- Voltage monitoring
- Temperature-compensated supply voltage limitation
- Chip temperature monitoring

### Applications

- Battery-operated screwdrivers
- Battery-operated machine tools
- Halogen lamp controllers
- Dimmers
- Electronic fuses
- High-performance clock generators

**Package:** DIP8, SO8

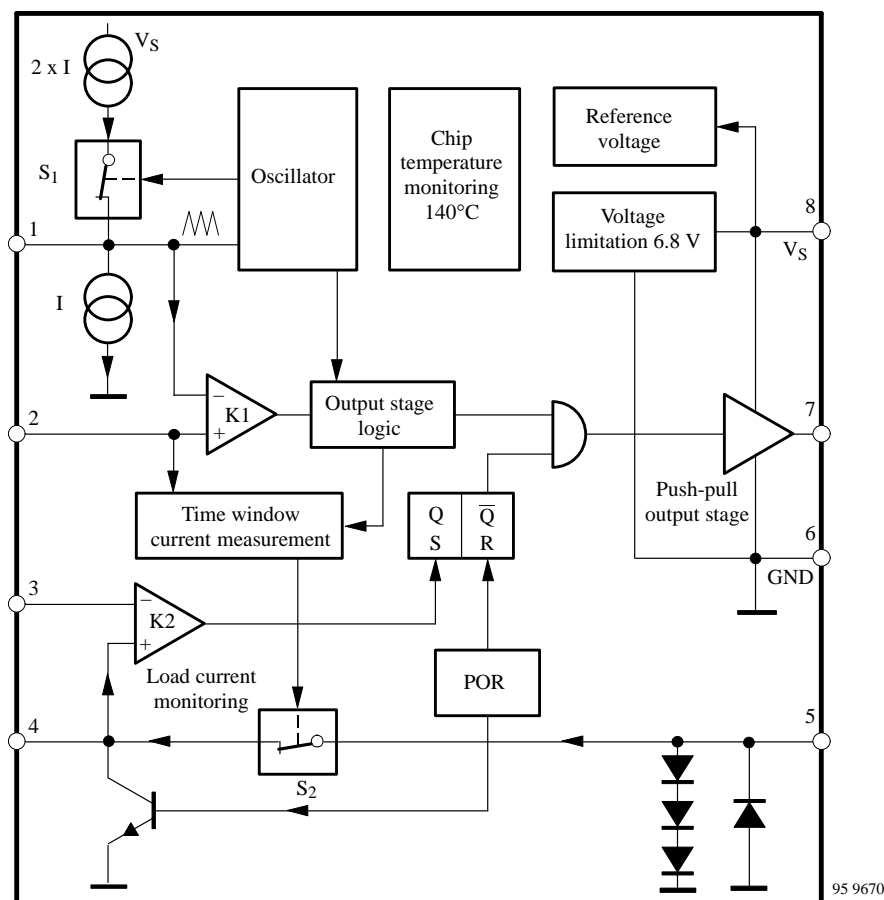
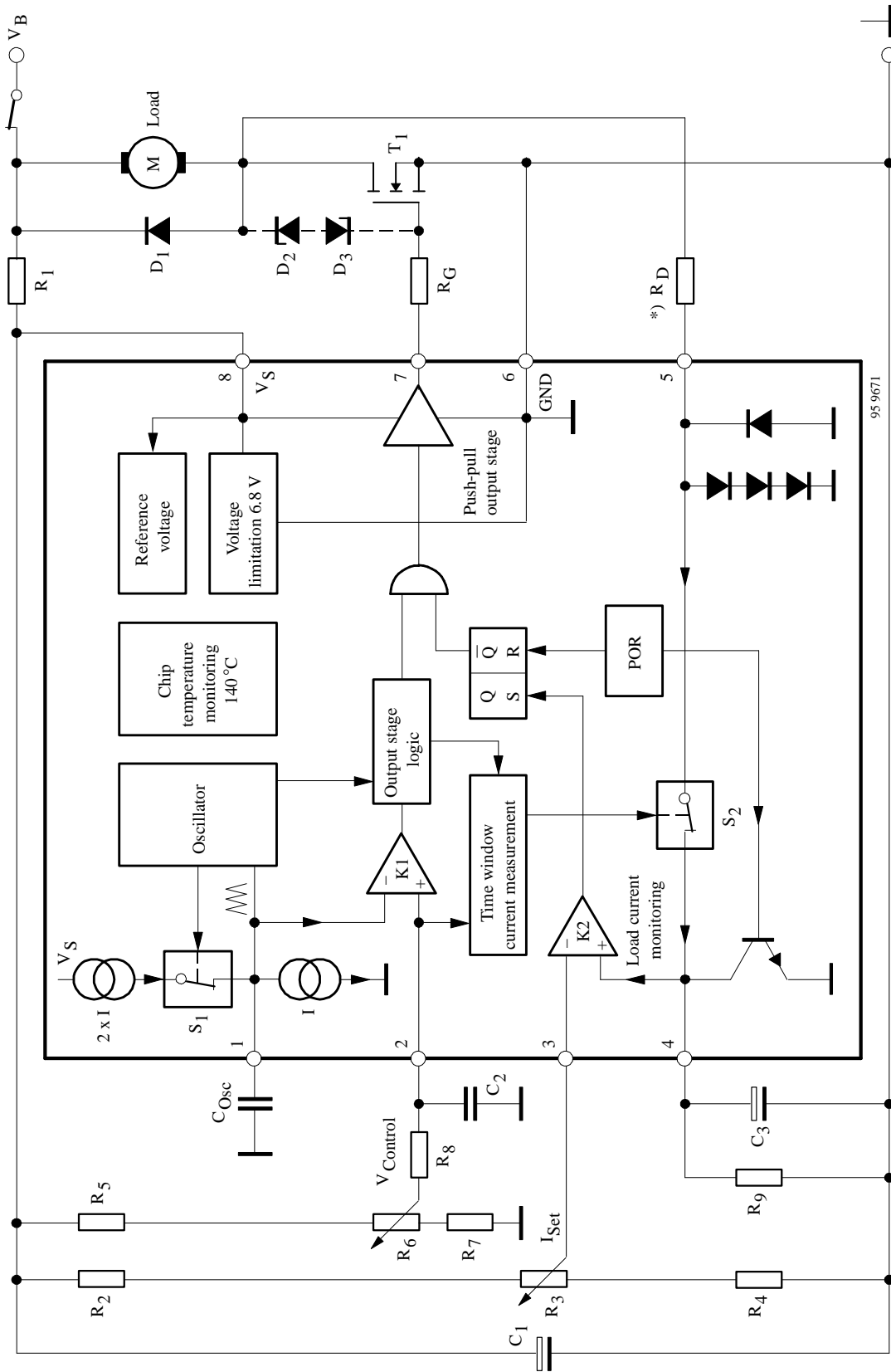


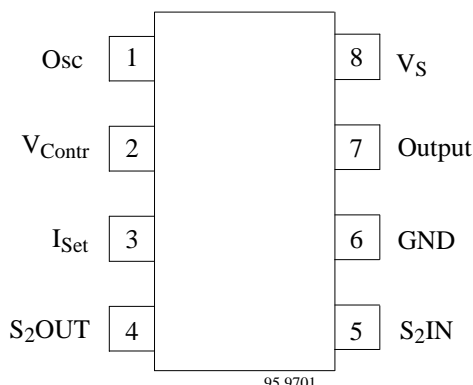
Figure 1. Block diagram



\* Load current can also optionally be measured via shunt resistor

Figure 2. Block diagram with typical circuit

## Pin Description



Pin	Symbol	Function
1	Osc	Oscillator
2	V <sub>Contr</sub>	Control voltage input
3	I <sub>Set</sub>	Setpoint value current monitoring
4	S <sub>2</sub> OUT	Output, current switch S <sub>2</sub>
5	S <sub>2</sub> IN	Input, current switch S <sub>2</sub>
6	GND	Ground
7	Output	Output
8	V <sub>S</sub>	Supply voltage

## Supply, Pin 8

Internal voltage limitation in the U2352B allows a simple supply via a series resistor R<sub>1</sub>. This enables operation of the circuit under different operating voltages. Supply voltage between Pin 8 (V<sub>S</sub>) and Pin 6 (GND) builds up via R<sub>1</sub> and is smoothed by C<sub>1</sub>.

The series resistor R<sub>1</sub> is calculated as follows:

$$R_{1\max} = \frac{V_{B\min} - V_{S\max}}{I_{\text{tot}}}$$

where

V<sub>Bmin</sub> = Minimum operating voltage

V<sub>Smax</sub> = Maximum supply voltage

I<sub>tot</sub> = I<sub>Smax</sub> + I<sub>X</sub>

I<sub>Smax</sub> = Maximum current consumption of the IS

I<sub>X</sub> = Current consumption of the external elements

Various thresholds are derived from an internal reference voltage source.

## Voltage Monitoring

During build-up and reduction of the operating voltage, uncontrolled output pulses with excessively low amplitude are suppressed by the internal monitoring circuit. All latches are reset and the output of the load current detection Pin 4 is switched to ground.

## Chip Temperature Monitoring

U2352B has integrated chip temperature monitoring which switches off the output stage when a temperature of approximately 140°C is reached. The device is not enabled again until cooling has taken place and the supply voltage has been switched off and then back on again.

## Pulse Width Control, Pins 1 and 2

At the frequency-determining capacitor, C<sub>osc</sub>, at Pin 1, switching over of two internal current sources gives rise to a triangular voltage which comparator, K<sub>1</sub>, compares with the control voltage at Pin 2. If the voltage, V<sub>1</sub>, is more negative than the control voltage V<sub>2</sub>, the output stage is switched on via the output stage logic. When C<sub>osc</sub> is charged, the whole process then runs in reverse order (see figure 3).

## Load Current Monitoring, Pins 3, 4, 5

Load current can be measured with the aid of an external shunt resistor, but this is only appropriate for decreased loads due to additional power loss and component size and costs. This involves the shunt voltage being fed directly to Pin 4 via a protective resistor (see figure 5).

In order to save component costs and additional power loss, the integrated load current monitoring allows the load current to be directly measured via the voltage drop at the on-state resistance, R<sub>DS(on)</sub>, of the FET, without an additional shunt resistor. The drain voltage of the FET is supplied via an external protective resistor to Pin 5. During the off-state of the FET, a diode clamp circuit protects the detection input, Pin 5. In the on state, the load current flowing through the FET generates a corresponding voltage drop at its R<sub>DS(on)</sub>, which is in turn converted into a current at Pin 5 by the protective resistor. This current reaches the integration element at Pin 4 via the switch S<sub>2</sub>, which is only closed in the on-state of the FET. If the voltage at Pin 4 exceeds the setpoint value set at Pin 3, as a result of a high load current, the shutdown latch is set and the output stage is blocked. To enable the circuit again, it is necessary to switch the operating voltage off and then back on again.

Switch-off behavior is adjusted with the resistors at Pin 4 and Pin 5 and also with the capacitor at Pin 4.

A time space,  $\Delta t$ , must be observed between switching the output stage off and on and switching  $S_2$  (current measurement enable switch) in order to avoid incorrect measurement and incorrect switching-off. To create this

time window, the control voltage  $V_2$  is reduced internally about  $\Delta V_2 =$  approximately 300 mV and the resulting voltage,  $V_2^*$ , is compared with the triangular voltage,  $V_1$  (see figure 3).

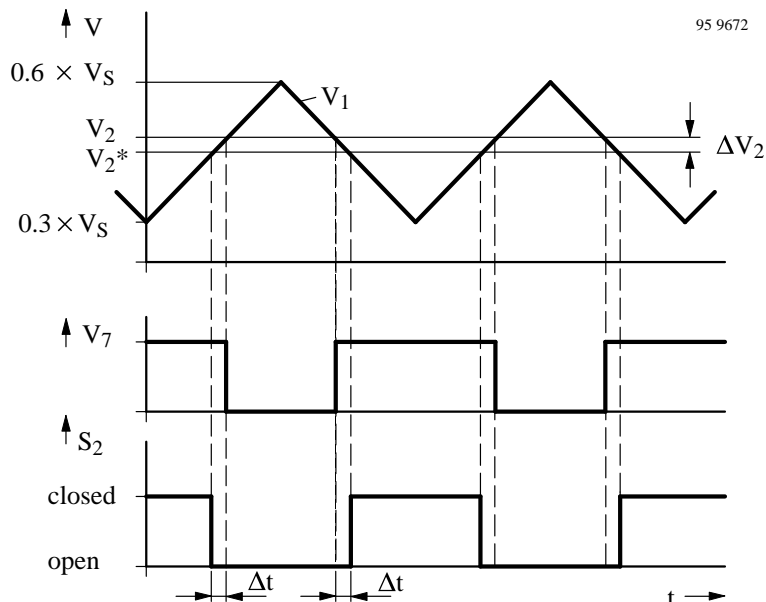


Figure 3. Signal characteristics of pulse width control with time window generation

## Absolute Maximum Ratings

Reference point Pin 6, unless otherwise specified

Parameters	Symbol	Value	Unit
Power supply current			
Pin 8	$I_S$	40	mA
Pin 8	$i_s$	400	
Push-pull output stage			
Output current			
Pin 7	$\pm I_O$	20	mA
Pin 7	$\pm i_O$	100	
Input currents			
Pins 4 and 5	$\pm I_I$	10	mA
Pins 1 and 3	$I_I$	2	
Input voltages			
Pins 1, 2 and 3	$V_I$	0 to $V_8$	V
Storage temperature range	$T_{stg}$	-40 to +125	°C
Junction temperature	$T_j$	+125	°C
Ambient temperature	$T_{amb}$	-10 to +100	°C

## Thermal Resistance

Parameters	Symbol	Maximum	Unit
Junction ambient			
DIP8		110	
SO8 on PC board		220	
SO8 on ceramic	$R_{thJA}$	140	K/W

## Electrical Characteristics

$V_S = 6\text{ V}$ ,  $T_{\text{amb}} = 25^\circ\text{C}$ , reference point Pin 6, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
<b>Supply voltage limitation</b>	$I_S = 5\text{ mA}$ Pin 8	$V_S$	6.4	6.8	7.2	V
	$I_S = 20\text{ mA}$		6.5	6.9	7.3	
<b>Current consumption</b>	$V_S = 6\text{ V}$ Pin 8	$I_S$		2.7	3.5	mA
<b>Voltage monitoring</b>						
Switch-on threshold	Pin 8	$V_{\text{SON}}$	5.2	5.6	6.0	V
Switch-off threshold	Pin 8	$V_{\text{SOFF}}$	4.7	5.1	5.5	
<b>Oscillator</b>						
	$f_{\text{osc}} [\text{kHz}] \approx \frac{55}{C_{\text{osc}} [\text{nF}] \times V_s [\text{V}]}$ Pin 1					
Upper threshold ( $0.6 \times V_S$ )		$V_{\text{TU}}$	3.4	3.6	3.8	V
Lower threshold ( $0.3 \times V_S$ )		$V_{\text{TL}}$	1.7	1.8	1.9	V
Charge current		$-I_{\text{ch}}$	26	33	40	$\mu\text{A}$
Discharge current		$I_{\text{dis}}$	26	33	40	$\mu\text{A}$
<b>Control voltage input</b>						
Input voltage range	Pin 2	$V_I$	0		$V_8$	V
Input current,	$0\text{ V} \leq V_2 \leq V_8$ Pin 2	$\pm I_i$			500	nA
Offset voltage $K_1$	Pin 2-1	$\pm V_{\text{Offs}}$			15	mV
Window, current measurement	Pin 2-1	$-\Delta V_2$	260	300	340	mV
<b>Load current monitoring</b>						
Setpoint value input:						
Input voltage range	Pin 3	$V_I$	0		6	V
Input current	$0\text{ V} \leq V_3 \leq 6\text{ V}$ Pin 3	$\pm I_i$			500	nA
Offset voltage $K_2$	Pin 4-3	$\pm V_{\text{Offs}}$			15	mV
Load current detection:						
Voltage limitation	$I_5 = 1\text{ mA}$ Pin 5	$V_L$		2.3		V
Voltage limitation	$I_5 = -1\text{ mA}$ Pin 5	$-V_L$		0.7		
Discharge current at POR	Pin 4	$I_{\text{dis}}$	1			mA
<b>Switch <math>S_2</math></b> Pin 5-4						
Residual voltage at closed switch	$V_4 = 0\text{ V}, I_5 = 50\text{ }\mu\text{A}$ $V_4 = 0.1\text{ V}, I_5 = 50\text{ }\mu\text{A}$ $V_4 = 0.3\text{ V}, I_5 = 50\text{ }\mu\text{A}$ $V_4 = 0.3\text{ V}, I_5 = 100\text{ }\mu\text{A}$	$V_{\text{Sat}}$		175 150 125 200		mV
<b>Push-pull output stage</b> Pin 7						
Upper saturation voltage	$I_7 = -2\text{ mA}$ Pin 7-8	$-V_{\text{Satu}}$			1	V
Lower saturation voltage	$I_7 = 10\text{ mA}$ Pin 7	$V_{\text{Satl}}$			0.3	V
Output current						
ON state	$t \leq 2\text{ }\mu\text{s}$	$-i_o$	100			mA
OFF state	$t \leq 2\text{ }\mu\text{s}$	$i_o$	100			

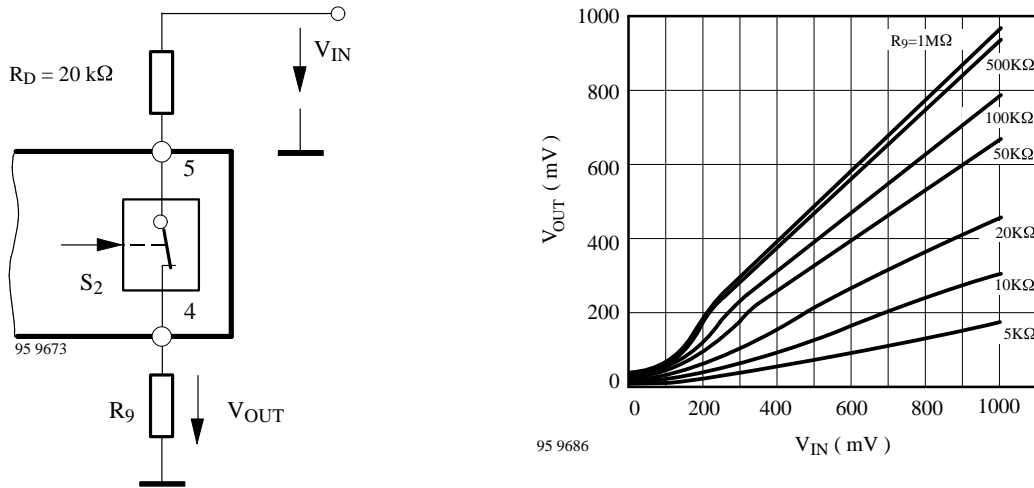


Figure 4. Typical circuitry of the current switch  $S_2$  with associated transfer characteristics ( $S_2$  closed)

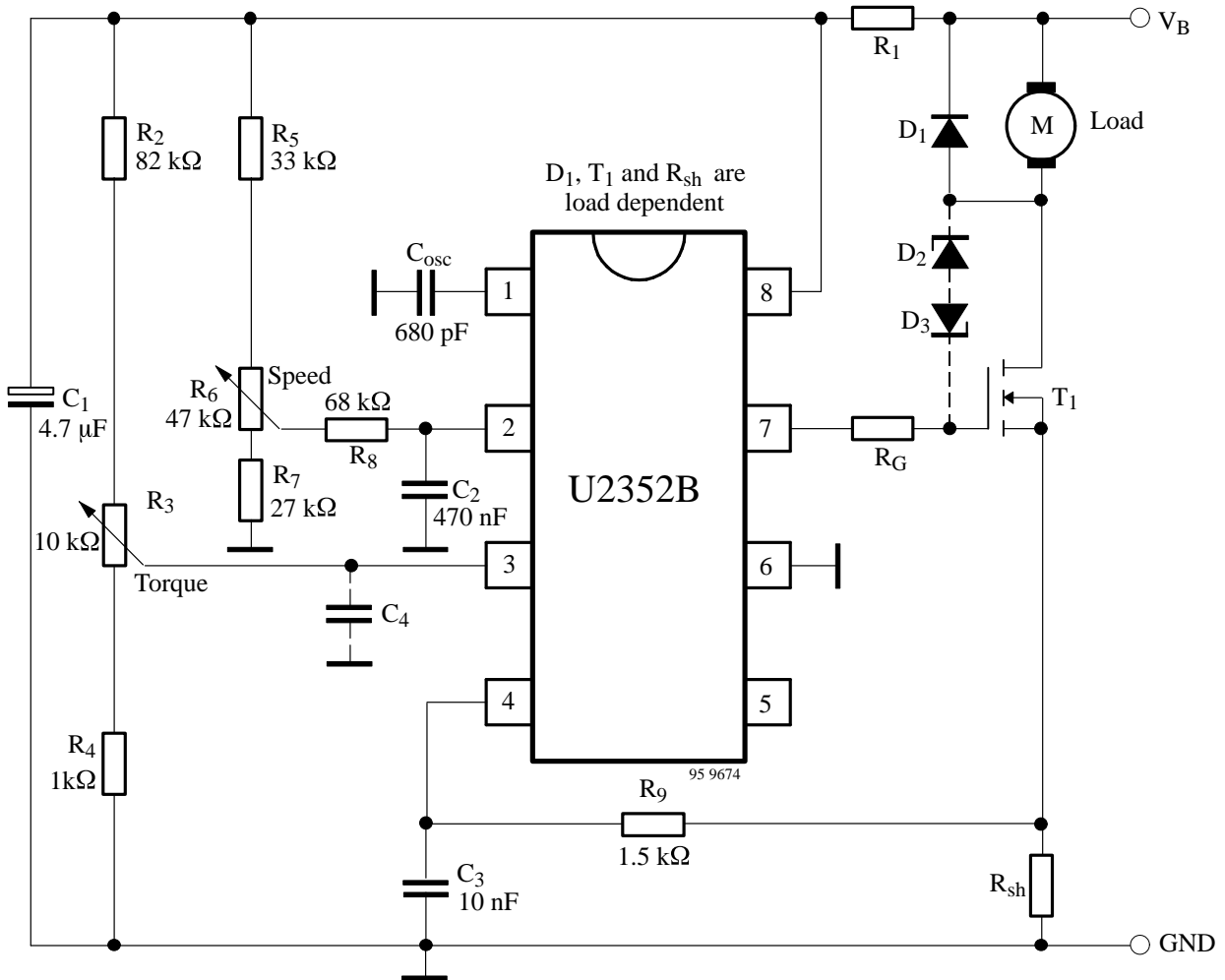
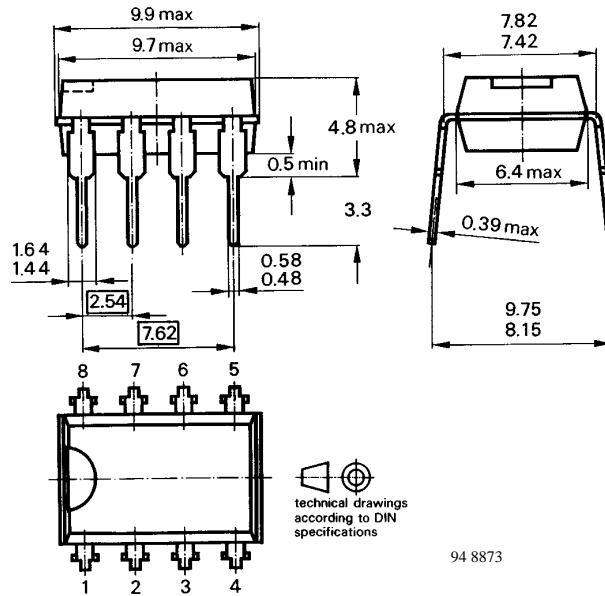


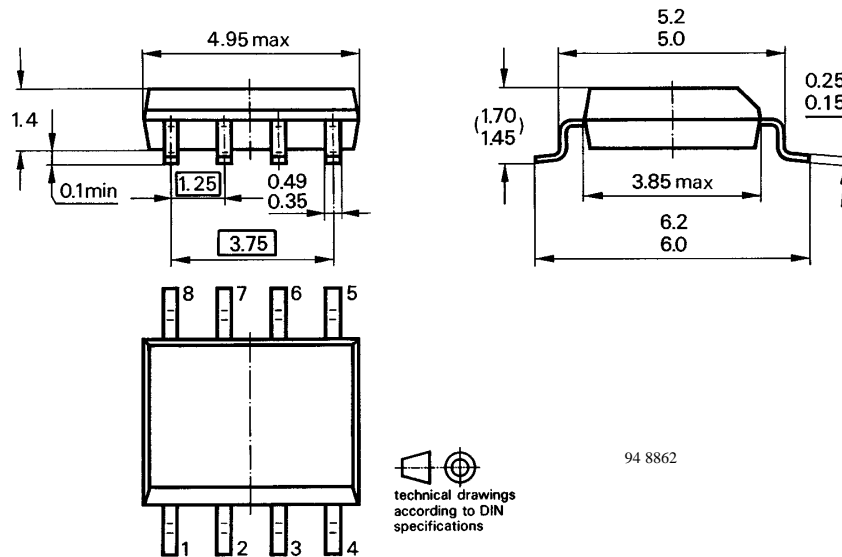
Figure 5. Speed control with load current monitoring (load current detection via shunt resistor)

## Dimensions in mm

Package: DIP8



Package: SO8



## Ozone Depleting Substances Policy Statement

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1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**TEMIC TELEFUNKEN microelectronic GmbH** semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

**TEMIC** can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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