DATA SHEET

UAA1570HL
Global Positioning System (GPS) front-end receiver circuit

Product specification
File under Integrated Circuits, IC18

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CONTENTS

Global Positioning System (GPS) front-end receiver circuit

UAA1570HL

1 FEATURES

- Complete single-chip programmable double-superheterodyne C/A-code GPS receiver
- Programmable high IF frequencies supporting wideband/P-code GPS and Global Navigation Satellite System (GLONASS) applications
- Supports frequency plans with a 2nd IF of $4 \times f_0$(1.023 MHz) = 4.092 MHz
- 48-pin LQFP package
- –40 to +85 °C operating temperature range
- 2.7 V minimum supply voltage
- Low DC power consumption [57 mA typical with both Low-Noise Amplifiers (LNAs) active]
- Power-down mode (<900 μA)
- Typical receiver noise figure at 1.57542 GHz: 4.5 dB
- Typical phase noise –72 dBc/Hz at 10 kHz offset
- Simple microstrip LNA1/2 and first mixer matching
- Single pin VCO with external varactor and resonator
- Digital Phase Locked Loop (DPLL) synthesizer with programmable VCO, 2nd Local Oscillator (LO) and reference dividers
- 3-bit synthesizer and power-down control input
- Reference and independent sample clock input with internal squaring
- 1-bit amplitude quantized and time sampled TTL/CMOS compatible output driver
- High active gain supporting SAW filter applications
- Configurable for external first LNA applications.

2 GENERAL DESCRIPTION

The UAA1570HL is a complete single-chip double-superheterodyne receiver front-end intended for GPS and GLONASS navigation systems. The IC includes a programmable on-chip DPLL synthesizer, VCO with external varactor and resonator, a 1-bit amplitude quantizer and a time sampled TTL/CMOS compatible SIGN output bit driver. It can be used with either an active or passive antenna system by disabling or enabling the on-chip LNAs and is ideally suited for low power GPS receiver applications because of its 3 V supply and the power management features through control pins.

Programmable prescaler controls provide the flexibility of using different frequency schemes.

The UAA1570HL is optimized to provide SIGN bit data to the companion Philips part, the SAA1575HL baseband digital signal processor. The SAA1575HL can provide the sample clock input to the UAA1570HL by dividing a TTL/CMOS level reference clock signal down to a programmable sampling clock output frequency. Both ICs can also be used independently.

The UAA1570HL is supplied in a low profile, 48-pin LQFP package for excellent Radio Frequency (RF) performance and small size.

3 ORDERING INFORMATION

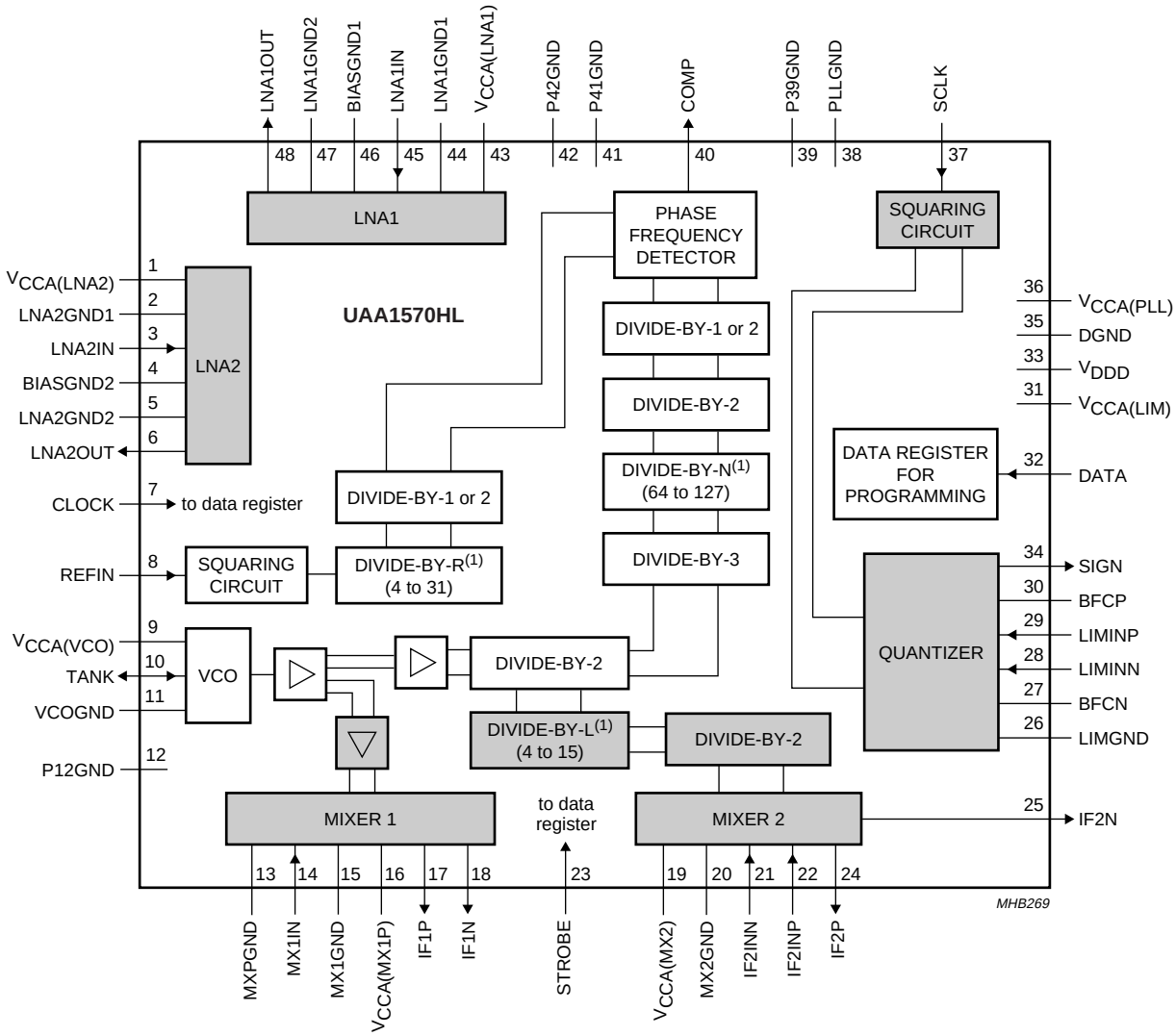
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA1570HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

4 QUICK REFERENCE DATA

V_{CCA} = V_{DDD} = 3 V; T_{amb} = 25 ±2 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		2.7	3	5	V
V_{DDD}	digital supply voltage		2.7	3	5	V
$I_{VCCA} + I_{VDDD}$	analog supply current plus digital supply current	V_{CCA} and V_{DDD} = 2.7 V	–	55.1	62.3	mA
		V_{CCA} and V_{DDD} = 5 V	–	61	69.3	mA
G_{RF}	available RF power gain	LNAs at 1.57542 GHz	–	31	–	dB
G_{IF1}	available 1st mixer power gain	MX1 at 1.57542 GHz	–	17.7	–	dB
G_{IF2}	available 2nd mixer power gain	MX2 at 41.8 MHz	–	21.4	–	dB
$G_{v(lim)}$	limiter voltage gain to 1st latch	limiter at 3.48 MHz	–	78	–	dBV
$\Delta V_{lim(M)}$	differential limiter sensitivity (peak value)	f = 3.48 MHz	–	100	–	μV
F_{RX}	receiver noise figure	f = 1.57542 GHz	–	4.5	5.2	dB
T_{amb}	operating ambient temperature	V_{CCA} and V_{DDD} = 3.3 to 5 V	–40	+25	+85	°C
		V_{CCA} and V_{DDD} = 3 to 5 V	–30	+25	+85	°C
		V_{CCA} and V_{DDD} = 2.7 to 5 V	0	+25	+85	°C

5 BLOCK DIAGRAM



Shaded blocks are NOT active during synthesizer state.

(1) The default values are: L = 10, N = 71 and R = 4.

Fig.1 Block diagram.

6 PINNING INFORMATION

SYMBOL	PIN	PIN VOLTAGE TYPICAL VALUES (V)		DESCRIPTION
		V_{CC} = 2.7 V	V_{CC} = 5 V	
$V_{CCA(LNA2)}$	1	2.7	5	**LNA2 power supply:** DC operation range 2.7 to 5 V; use close proximity RF decoupling to pins 2, 4 and 5
LNA2GND1	2	0	0	**LNA2 ground 1:** minimize RF ground inductance
LNA2IN	3	0.815	0.807	**LNA2 input:** use external RF AC coupling
BIASGND2	4	0	0	**LNA2 bias circuit ground:** minimize RF ground inductance
LNA2GND2	5	0	0	**LNA2 ground 2:** minimize RF ground inductance
LNA2OUT	6	1.48	3.629	**LNA2 output:** use external RF AC coupling. The DC voltage is approximately 1.3 V below the $V_{CCA(LNA2)}$ supply on pin 1.
CLOCK	7	CMOS level	CMOS level	**Serial interface clock input:** this DC coupled CMOS **CLOCK** input moves 20-bit programming words into the synthesizer **DATA** input register while the **STROBE** is LOW. A DC short-circuit to ground is recommended with the default frequency plan.
REFIN	8	1.69	3.99	**Reference input:** use external AC coupling. The DC voltage is approximately 1 V below the $V_{CCA(PLL)}$ supply on pin 36.
$V_{CCA(VCO)}$	9	2.7	5	**VCO power supply:** DC operation range 2.7 to 5 V; use **critical** close proximity RF decoupling to pin 11
TANK	10	1.92	1.92	**VCO negative impedance resonator port:** use the absolute minimum trace lengths and widths and keep the loop to the VCO ground pin 11 as short as possible, while centring the COMP output voltage at pin 40 within the charge pump output voltage range given in Chapter 11 by adjusting the resonator inductance and/or required AC coupling component.
VCOGND	11	0	0	**VCO ground:** minimize RF ground inductance; use **critical** close proximity RF decoupling to VCO supply pin 9
P12GND	12	0	0	this pin provides additional RF shielding and has to be connected to ground
MXPGND	13	0	0	**RF mixer preamplifier ground:** minimize RF ground inductance
MX1IN	14	0.82	0.81	**RF mixer preamplifier input:** use external AC coupling and RF matching
MX1GND	15	0	0	**RF mixer ground:** minimize RF ground inductance; use **critical** close proximity RF decoupling to $V_{CCA(MX1P)}$ supply pin 16
$V_{CCA(MX1P)}$	16	2.7	5	**RF preamplifier/mixer power supply:** DC operation range 2.7 to 5 V; use **critical** close proximity RF decoupling to pin 15
IF1P	17	2.7	5	**RF mixer IF positive output:** DC couple this output pin to the $V_{CCA(MX1P)}$ supply through first IF filter inductors or RF chokes. Capacitively decouple the supply near the output inductors. Balanced first mixer IF1 outputs are recommended. Prevent externally squared reference harmonics from entering the first IF signal path or components.

SYMBOL	PIN	PIN VOLTAGE TYPICAL VALUES (V)		DESCRIPTION
		V_{CC} = 2.7 V	V_{CC} = 5 V	
IF1N	18	2.7	5	**RF mixer IF negative output:** DC couple this output pin to the $V_{CCA(MX1P)}$ supply through first IF filter inductors or RF chokes. Capacitively decouple the supply near the output inductors. Balanced first mixer IF1 outputs are recommended. Prevent externally squared reference harmonics from entering the first IF signal path or components.
$V_{CCA(MX2)}$	19	2.7	5	**IF mixer power supply:** if present, decouple the common V_{CC} line sourcing the first and second mixer by placing a large decoupling capacitor between the two
MX2GND	20	0	0	**IF mixer ground:** minimize IF ground inductance; use close proximity IF decoupling to the $V_{CCA(MX2)}$ supply pin 19
IF2INN	21	0.983	0.98	**IF mixer negative input:** use external AC coupling. Balanced IF1 second mixer inputs are recommended. Prevent externally squared reference harmonics from entering the first IF signal path or components.
IF2INP	22	0.983	0.98	**IF mixer positive input:** use external AC coupling. Balanced IF1 second mixer inputs are recommended. Prevent externally squared reference harmonics from entering the first IF signal path or components.
STROBE	23	CMOS level	CMOS level	**Serial interface strobe input:** a LOW level on this DC-coupled CMOS **STROBE** input enables the **CLOCK** input to load the 20-bit programming word into the synthesizer input **DATA** register. A mandatory DC short-circuit to ground is required to ensure that the default frequency plan is invoked on power-up.
IF2P	24	2.7	5	**IF mixer second IF positive output:** DC couple this output pin to the $V_{CCA(MX2)}$ supply through second IF filter inductors or RF chokes. Capacitively decouple the supply near the output inductors. Balanced second mixer IF2 outputs are optional for many applications. Short the unused IF2P or IF2N output directly to the supply in single-ended applications.
IF2N	25	2.7	5	**IF mixer second IF negative output:** DC couple this output pin to the $V_{CCA(MX2)}$ supply through second IF filter inductors or RF chokes. Capacitively decouple the supply near the output inductors. Balanced second mixer IF2 outputs are optional for many applications. Short the unused IF2P or IF2N output directly to the supply in single-ended applications.
LIMGND	26	0	0	**Limiter ground:** minimize ground inductance
BFCN	27	1.696	3.999	**Negative limiter input DC feedback loop decoupling:** AC couple this pin to ground in close proximity to the pin. The DC voltage is approximately 1 V below the $V_{CCA(LIM)}$ supply on pin 31. **No DC coupling.**
LIMINN	28	1.696	3.999	**Negative limiter input:** AC couple this pin to the second IF filter output or to ground if unused with single-ended filter applications. The DC voltage is approximately 1 V below the $V_{CCA(LIM)}$ supply on pin 31. **No DC coupling.**

SYMBOL	PIN	PIN VOLTAGE TYPICAL VALUES (V)		DESCRIPTION
		V_{CC} = 2.7 V	V_{CC} = 5 V	
LIMINP	29	1.696	3.999	**Positive limiter input:** AC couple this pin to the second IF filter output or to ground if unused with single-ended filter applications. The DC voltage is approximately 1 V below the $V_{CCA(LIM)}$ supply on pin 31. **No DC coupling.**
BFCP	30	1.696	3.999	**Positive limiter input DC feedback loop decoupling:** AC couple this pin to ground in close proximity to the pin. The DC voltage is approximately 1 V below the $V_{CCA(LIM)}$ supply on pin 31. **No DC coupling.**
$V_{CCA(LIM)}$	31	2.7	5	**Limiter, sample clock squaring and sampler Emitter Coupled Logic (ECL) circuits power supply:** decouple in close proximity to pins 26 and 31. If present, isolate from the common V_{CC} line sourcing the first and second mixer by placing a large decoupling capacitor between this block and the mixers.
DATA	32	CMOS level	CMOS level	**Serial interface data input:** this DC-coupled CMOS **DATA** input accepts 20-bit programming words into the synthesizer data input register, while the **STROBE** is LOW, on the rising edge of the **CLOCK** input. A DC short-circuit to ground is recommended with the default frequency plan.
V_{DDD}	33	2.7 (independent of V_{CC} level)	5 (independent of V_{CC} level)	**SIGN bit TTL output driver power supply:** critically isolate and separately decouple this digital V_{DDD} supply from all other analog (V_{CCA}) supplies. Maintain minimum trace lengths to decoupling components. Particular attention should be applied to prevent coupling into $V_{CCA(LIM)}$ pin 31. If SAA1575HL is used, use the digital supply from the back-end.
SIGN	34	TTL output	TTL output	**Amplitude and time quantized second IF output signal:** extreme care should be taken to isolate this sampled TTL output signal from all analog traces and components, particularly the second IF filter components at the limiter input. Avoid coupling into the reference oscillator signal trace.
DGND	35	0	0	**SIGN bit TTL output driver sink ground:** critically isolate this digital supply ground from all other analog supplies and grounds. Maintain minimum trace lengths to decoupling components.
$V_{CCA(PLL)}$	36	2.7	5	**Synthesizer power supply:** decouple in close proximity to pin 38
SCLK	37	1.34	2.5	**Sample clock squaring input:** accepts LOW-level AC coupled sample clock inputs directly from the PLL reference oscillator or DC-coupled externally squared digital clocks derived from the PLL reference oscillator after external frequency division. The maximum DC-coupled input level at pin 37 should not exceed 75% of the $V_{CCA(LIM)}$ supply value. The threshold level is set at half the supply value on $V_{CCA(LIM)}$ pin 31.
PLLGND	38	0	0	**PLL ground:** minimize ground inductance; use close proximity decoupling to the $V_{CCA(PLL)}$ supply pin 36
P39GND	39	0	0	this pin provides additional RF/IF shielding and has to be connected to ground

SYMBOL	PIN	PIN VOLTAGE TYPICAL VALUES (V)		DESCRIPTION
		V_{CC} = 2.7 V	V_{CC} = 5 V	
COMP	40	depends on VCO application	depends on VCO application	**Charge pump phase frequency detector output:** the PLL loop filter is connected in shunt and close proximity to this pin. The PLL loop filter tuning control voltage should be routed to the external VCO varactor circuit using minimal trace lengths in complete isolation from all potential coupling sources.
P41GND	41	0	0	this pin provides additional RF/IF shielding and has to be connected to ground
P42GND	42	0	0	this pin provides additional RF/IF shielding and has to be connected to ground
$V_{CCA(LNA1)}$	43	2.7	5	**LNA1 power supply:** DC operation range 2.7 to 5 V; use close proximity RF decoupling to pins 44, 46 and 47.
LNA1GND1	44	0	0	**LNA1 ground 1:** minimize RF ground inductance
LNA1IN	45	0.815	0.807	**LNA1 input:** use external RF AC coupling
BIASGND1	46	0	0	**LNA1 bias circuit ground:** minimize RF ground inductance
LNA1GND2	47	0	0	**LNA1 ground 2:** minimize RF ground inductance
LNA1OUT	48	1.48	3.629	**LNA1 output:** use external RF AC coupling. The DC voltage is approximately 1.3 V below the $V_{CCA(LNA1)}$ supply on pin 43.

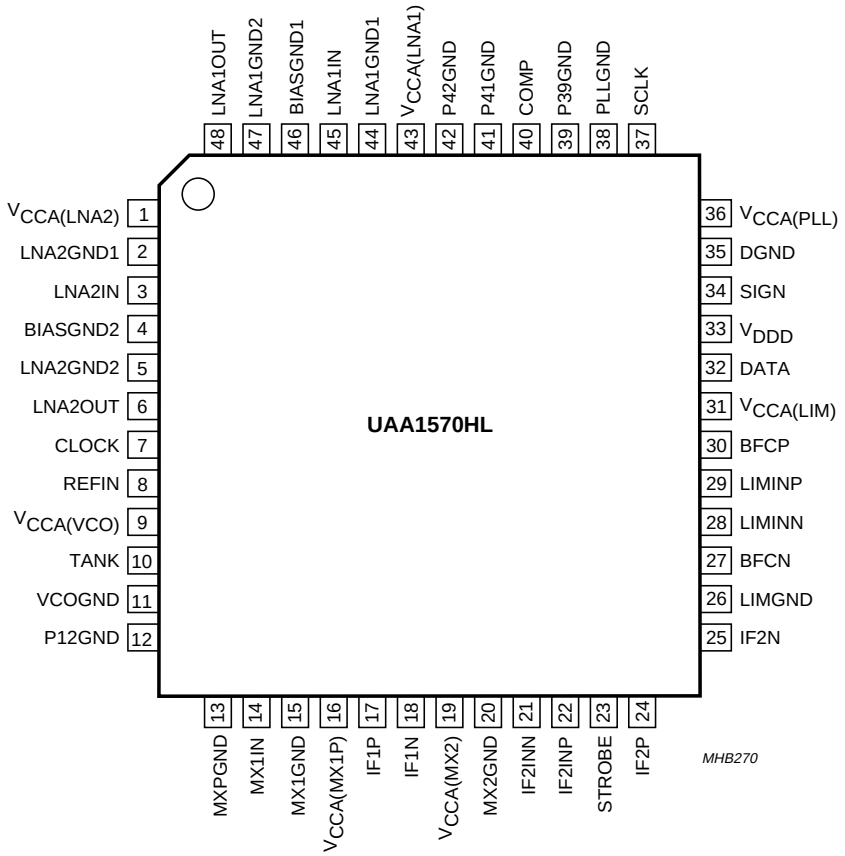


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The programmability of the UAA1570HL and flexible interface definitions allow the device to be configured for a wide range of applications. To restrict the content of this document the functional description of the device will generally concentrate on the C/A-code application circuit based on the default frequency plan.

The application circuit does not allow easy measurement, calibration and documentation of the many sub-block characteristics which ensure good system performance. Therefore, test boards have been developed which allow direct measurement of the sub-block characteristics.

The tables and graphs reflect the UAA1570HL specification as derived from simulation and measured results in these characterization board environments. The tables and graphs do not directly specify application board expectations. The functional description however, focuses on the default application.

The RF system diagram (see Fig.3) illustrates the default application of the UAA1570HL in the Philips GPS demonstration board. In this application the UAA1570HL is intended to be operated directly from a passive GPS antenna through a very short antenna cable. Any cable loss in this demonstrator adds directly to the system noise figure and should therefore be minimized.

LNA1 can be powered down in the UAA1570HL to accommodate applications built around external LNAs, typically where long antenna cable runs are required.

The first LNA is assumed to be matched with a 2nd-order band-pass structure to provide some input selectivity, since no dielectric or SAW filter has been used in the demonstration board. It should be noted that low loss RF SAW filters now make it possible to significantly improve the jam immunity of this amplifier, by placing a SAW filter at the output of the antenna.

On the demonstration board the first LNA is followed by a low loss RF SAW filter (<2.4 dB).

On the demonstration board the second LNA has been matched to 50 Ω using a simple transmission line structure.

Finally, another identical RF SAW filter follows the second LNA into the first mixer.

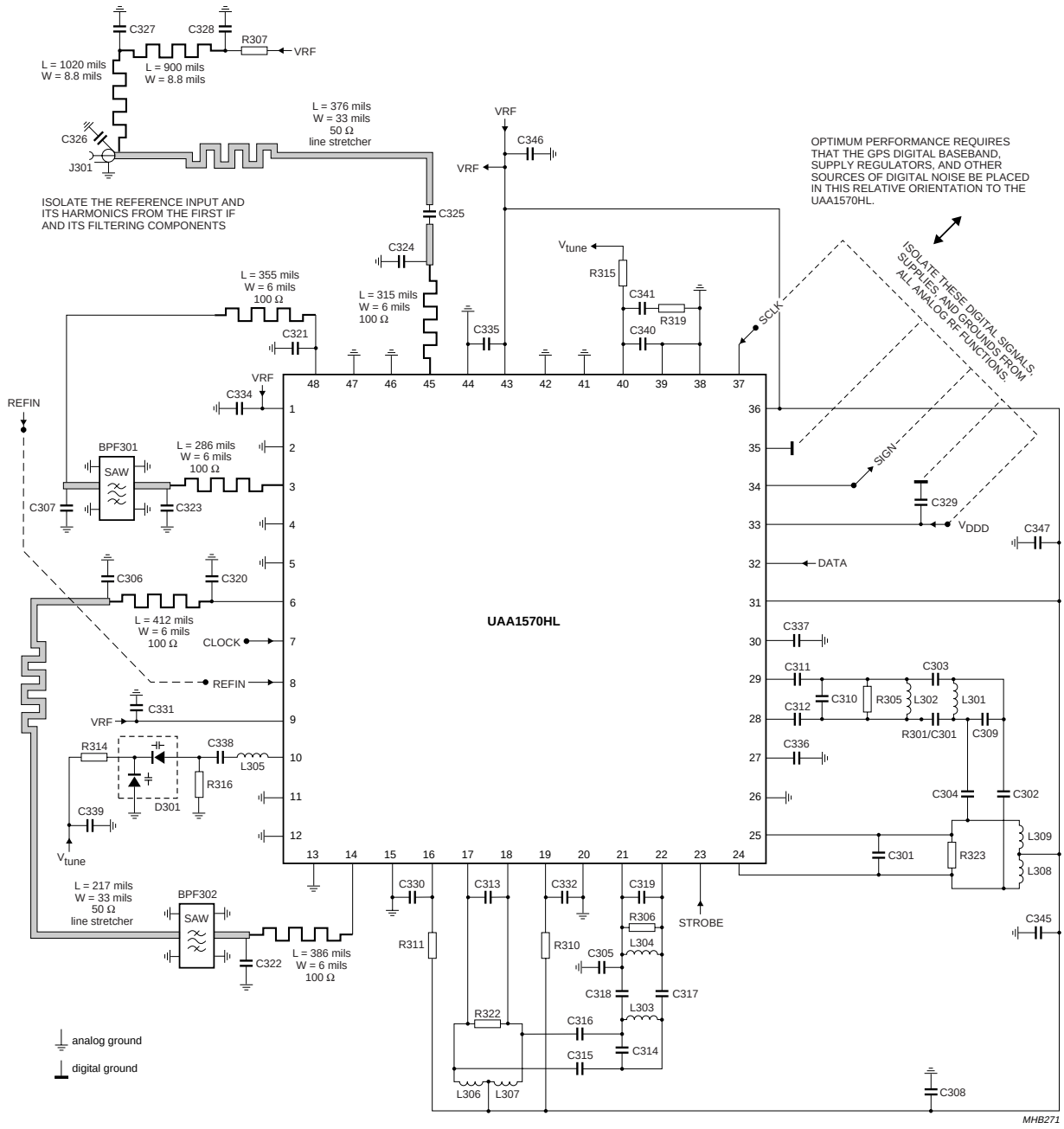


Fig.3 UAA1570HL RF system diagram (default application).

7.1 Low noise amplifiers LNA1 and LNA2

Two identical LNAs are provided on the IC although LNA1 need not be biased, if sufficient external gain is provided by an external LNA. The input stage of each amplifier consists of an unbalanced common emitter and a cascode stage. The AC-coupled output stage is a compound feedback bootstrap amplifier. Each stage is independently biased and regulated. LNA1 can be disabled by connecting the respective supply (pin 43) to ground. LNA2 has to be powered-up even if not used.

Each LNA can supply a power matched gain of approximately 15.5 dB with an associated noise figure of 3.7 dB.

Both LNAs have −1 dB input compression points of approximately −22 dBm from a 3 V supply. The 2nd and 3rd-order input intercepts are approximately −7.9 and −13 dBm, respectively, in a power matched environment.

The RF match impedances at L1 (1.57542 GHz) are provided in Table 1 for all RF inputs and outputs.

Table 1 RF matching impedances

PIN	REAL PART (Ω)	IMAGINARY PART (Ω)	FUNCTION
45	31	−j32	LNA1 input
48	77.5	+j6	LNA1 output
3	24	−j25	LNA2 input
6	74.5	−j0.5	LNA2 output
14	33.5	−j25.5	1st mixer input

These RF port impedances are marked on the following Smith charts (see Figs 4 to 8; normalized to 50 Ω) and suggested matching structure netlists are provided. They contain transmission lines defined by their characteristic impedance Z (in ohms), their electrical length E (in degrees) and the operating frequency f (in GHz). Capacitors C are given in pF. TLIN is a series transmission line and TLOC is an open-circuit stub transmission line. Node 1 is the UAA1570HL RF port being matched and Node 0 is ground. These matching networks are structurally identical to those illustrated on the GPS application block diagram, however, the component values in the application diagram are somewhat different to account for stray capacitances and other real world influences. The netlists are derived from EEZMATCH software (Besser Associates, Los Altos, CA, USA).

Generally, we assume a minimum shunt capacitance, due to the IC pin pad and adjacent pin strays, of approximately 0.25 pF as an initial stray element in the netlist below, that will always be present in the matching structure design. This value should be re-estimated and matched if the layout introduces significant additional strays at the pin pads.

7.1.1 LNA1IN

CAP 1 0 C = 0.25 ! C1 C = PF

TLIN 1 2 Z = 97.0 E = 34.5 F = 1.57542 ! TL1 Z = OH, E = DEG, F = GHZ

CAP 2 0 C = 2.0 ! C3 C = PF

Alternatively the 2 pF shunt capacitance at the input of the 97 Ω matching line above might be replaced with a 25 Ω microstrip open stub if space permits.

TLOC 2 0 Z = 25.0 E = 26.1 F = 1.57542

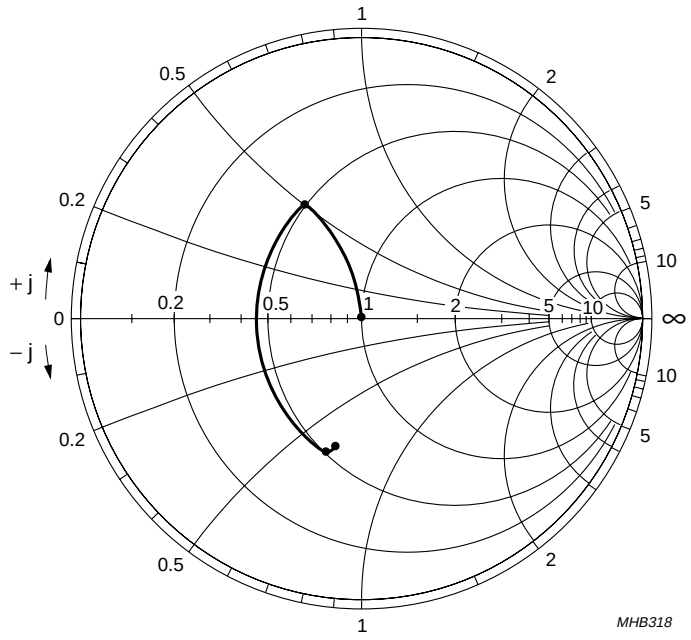


Fig.4 LNA1 input impedance and matching network.

7.1.2 LNA1OUT

To facilitate matching of both LNA outputs, a small shunt capacitance should be placed as close as possible to the output pin pad increasing the assumed 0.25 pF lumped pin capacitance by approximately 0.5 pF to 0.75 pF. This ensures that a simple, short, high impedance transmission line will provide a good 50 Ω match at high gain. A via to the opposite side of the board right at this output pin allows a stub or chip capacitance to be added without comprising the characteristics of the 97 Ω matching line.

CAP 1 0 C = 0.25 ! C22 C = PF

IND 1 28 L = 0.7 ! L7 = NH

CAP 28 0 C = 7.1658792e–1 ! C23 C = PF

TLIN 28 29 Z = 97.0 E = 26.239010 F = 1.57542 ! TL15

If an open line stub is used, the latter components have to be replaced by:

TLOC 28 0 Z = 20.0 E = 8.0 F = 1.57542 ! OTL7 Z = OH, E = DEG, F = GHZ

TLIN 28 30 Z = 97.0 E = 26.2 F = 1.57542 ! TL16 Z = OH, E = DEG, F = GHZ

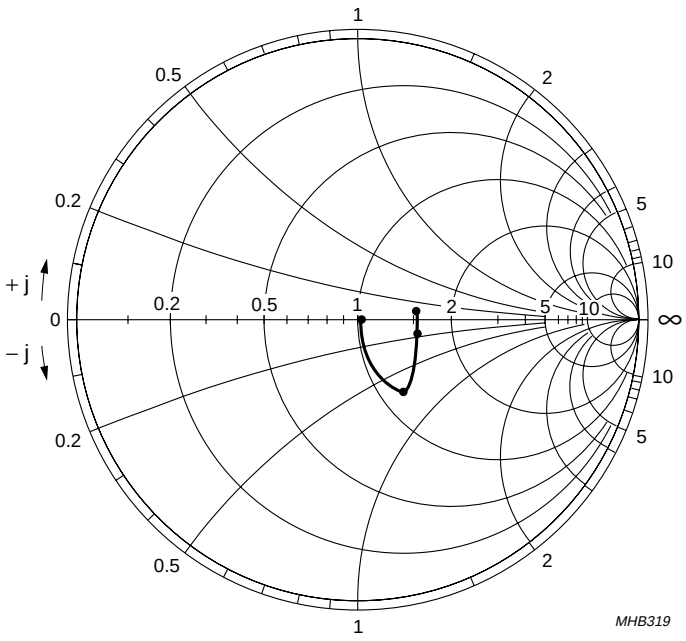


Fig.5 LNA1 output impedance and matching network.

7.1.3 LNA2IN

CAP 1 0 C = 0.25 ! C13 C = PF

TLIN 1 14 Z = 97.0 E = 30.0 F = 1.57542 ! TL9 Z = OH, E = DEG, F = GHZ

CAP 14 0 C = 2.3309277 ! C14 C = PF

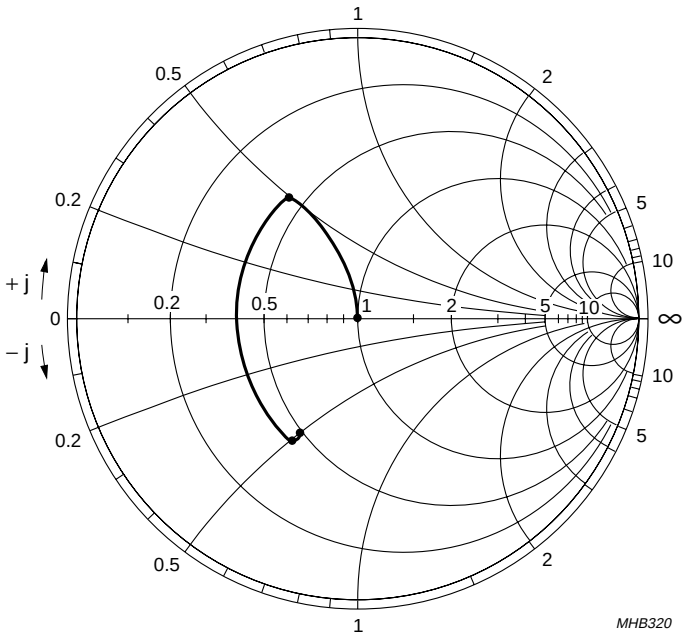


Fig.6 LNA2 input impedance and matching network.

7.1.4 LNA2OUT

CAP 1 0 C = 0.25 ! C22 C = PF

IND 1 31 L = 0.1 ! L8 L = NH

CAP 31 0 C = 0.5 ! C24 C = PF

TLIN 31 32 Z = 97.0 E = 25.077020 F = 1.57542 ! TL17 Z = OH, E = DEG, F = GHZ

In the event that the second capacitor is replaced by an open line stub, the last two components have to be changed:

TLOC 31 0 Z = 20.0 E = 5.5 F = 1.57542 ! OTL8 Z = OH, E = DEG, F = GHZ

TLIN 31 33 Z = 97.0 E = 24.460094 F = 1.57542 ! TL = 18 Z = OH, E = DEG, F = GHZ

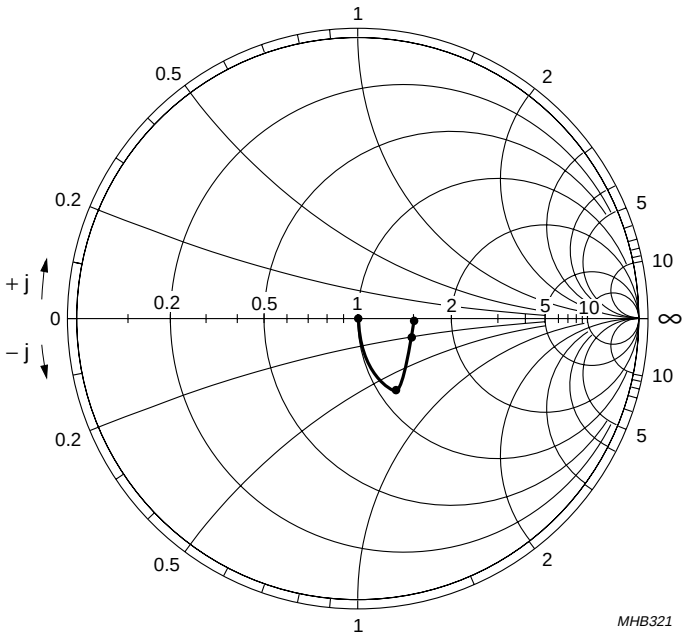


Fig.7 LNA2 output impedance and matching network.

7.1.5 MX1IN

CAP 1 0 C = 0.25 ! C5 C = PF

TLIN 1 13 Z = 100.0 E = 31.083933 F = 1.57542 ! TL9 Z = OH, E = DEG, F = GHZ

CAP 13 0 C = 1.673902 ! C6 C = PF

Again an alternative open stub line is suggested which could be used to replace the 1.67 pF capacitance at this end of the previous netlist.

TLOC 13 0 Z = 25.0 E = 23.0 F = 1.57542 ! OTL5 Z = OH, E = DEG, F = GHZ

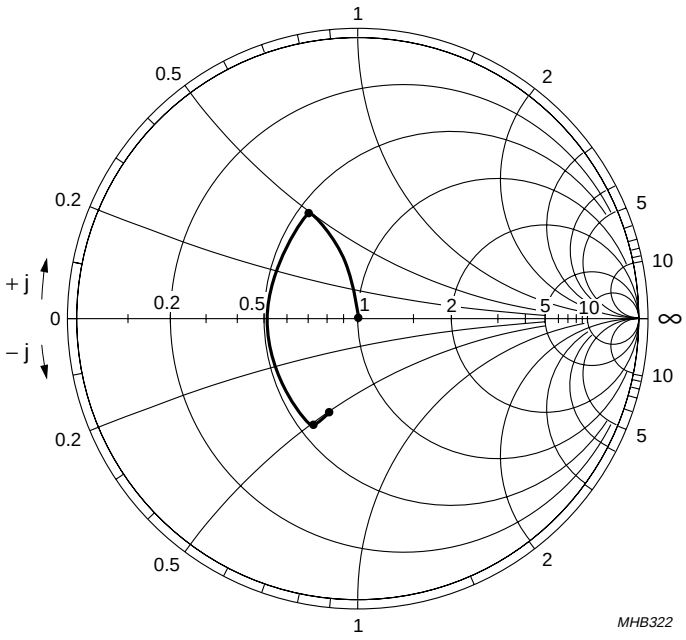
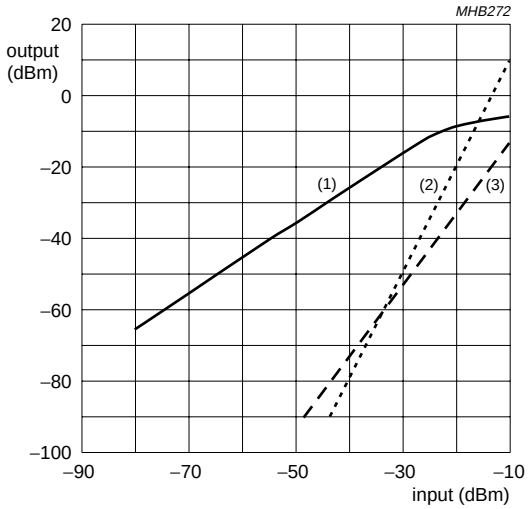


Fig.8 MX1 input impedance and matching network.

7.1.6 General remarks and results

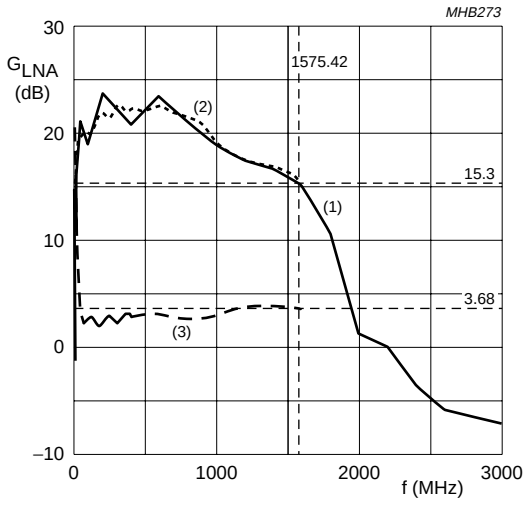
The RF match has an important effect on the gains, noise figure, and dynamic characteristics of the RF system blocks. Reflection coefficients better than −15 dB are easily attainable and can be improved to better than −25 dB with attention to details.



(1) Fundamental output.
(2) 3rd-order product output.
(3) 2nd-order product output.

Fig.9 Typical LNA fundamental, 2nd and 3rd-order product output levels as a function of input level.

In the following graph (see Fig.10) the solid trace G_{LNA} (dB) represents the measured frequency response of the UAA1570HL LNAs as measured on a spectrum analyzer, while the dotted and dashed results were obtained using a noise figure meter over a more restricted frequency range.



(1) LNA gain (dB).
(2) Power gain.
(3) Noise figure.

Fig.10 Typical LNA gain and noise figure as a function of frequency (50 Ω power matched on the input and output).

7.2 Correlation of the UAA1570HL data sheet, application and test boards

The application circuit does not allow easy measurement, calibration and documentation of the many sub-block characteristics which ensure good system performance. Therefore, test boards have been developed which allow direct measurement of the sub-block characteristics.

These boards use a 1 : 16 Ω ratio RF transformer to transform 50 Ω to the more appropriate value of 800 Ω at IF frequencies. The high-impedance side of these transformers is terminated with a physical resistor to adjust the UAA1570HL impedance at the port being measured, to approximately 800 Ω. This ensures that a calibrated signal is applied or received in the 50 Ω test environment. The transformer provides marginal performance at 41.8 MHz, so calibration results for this transformer are also included in this document.

The 800 Ω impedance environment is somewhat less than that used in the application board. The UAA1570HL Characteristic tables provided in this document are calibrated to this 800 Ω environment as quantified in the notes at the end of the table. The effects of the transformer and associated termination losses have also been removed to some extent, so that specifications reflect the performance of the IC. The measured graph results were all derived from the test boards and corrected to again reflect part performance as much as possible.

However, this was not always possible, so some discussion concerning the measurement limitations is provided where appropriate. Where possible, fundamental design relationships and limitations are indicated.

The following two graphs (Figs 11 and 12) reflect the measured performance of the 1 : 16 Ω ratio RF transformer used to test the IF functions. Two transformers were placed back-to-back to make these measurements. Figure 11 represents the transmission function of just one of these transformers over frequency. Figure 12 represents the associated return loss at one input with the second transformer terminated into 50 Ω. In the actual UAA1570HL test board a single transformer is terminated in 800 Ω.

In addition to the direct effects of power losses introduced by the transformer (approximately –1.3 dB at 41.82 MHz), which are reflected in the measured S21 results, the test board results may also be impacted by deficiencies in the transformer 1 : 4 voltage step-up ratio at 41.8 MHz; however, this has not been quantified.

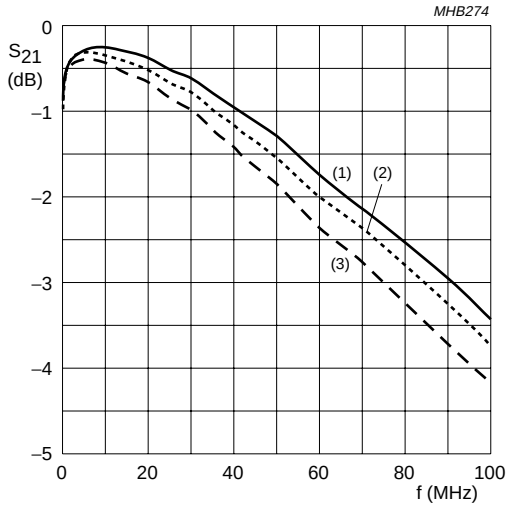
An additional correction must be made to the current test results to compensate for internal 4 pF shunt capacitors on each collector output of the first mixer, which have not been resonated out in the testing.

The first mixer measurements also include a 3 dB loss due to the 800 Ω transformer termination. This loss is also removed from the specification result. The second mixer has similar 2.1 dB input and 3 dB output transformer termination losses removed from the specification.

For measurements made at 3.48 MHz in the second IF, 0.4 dB must be added to the measured results to reflect transformer losses at IF2, also.

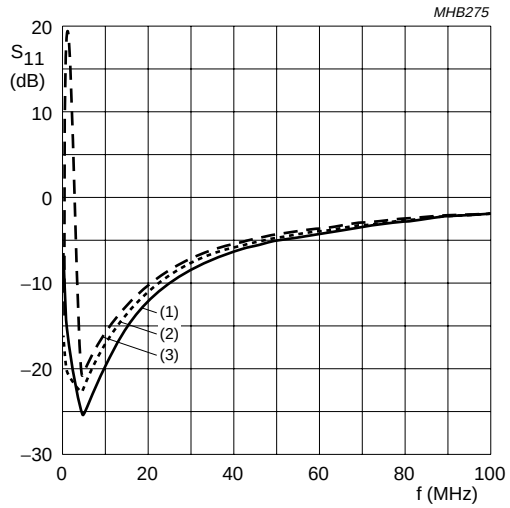
In summary the measured gain of the first mixer has been increased by 1.3 dB (transformer IL) + 1.4 dB (capacitive roll-off effects) + 0.2 dB (gain match) + 3 dB (output transformer termination loss) or 5.9 dB to calibrate out these losses in the specification.

The measured gain of the second mixer has been increased by 1.3 dB (input transformer IL) + 1.7 dB (input term loss) + 0.4 dB (output transformer IL) and + 3 dB (output term loss) or 6.4 dB to calibrate out these losses in the specification.



(1) S_{21}; T_{amb} = −40 °C.
(2) S_{21}; T_{amb} = +25 °C.
(3) S_{21}; T_{amb} = +85 °C.

Fig.11 S_{21} for the test measurement transformer.



(1) S_{11}; T_{amb} = −40 °C.
(2) S_{11}; T_{amb} = +25 °C.
(3) S_{11}; T_{amb} = +85 °C.

Fig.12 S_{11} for the test measurement transformer.

7.3 RF mixer with preamplifier

The 1st mixer (the RF mixer) consists of an RF preamplifier followed by a Gilbert cell mixer. The RF preamplifier consists of the same unbalanced common emitter and cascode stage as used in the LNAs, but without the compound feedback bootstrap output stage.

The cascode output is AC-coupled into one side of the lower tree of the Gilbert cell mixer. The other side is internally AC-coupled to mixer ground via a 20 pF decoupling capacitor. The Gilbert mixer RF input is degenerated with low loss inductive emitter feedback to increase the effective −1 dB compression point and intercept points. Referenced to the preamplifier input, the −1 dB compression point and 3rd-order intercept point are −25.4 dBm and −16.3 dBm, respectively. Another important first mixer parameter is its 2nd-order input intercept point, which will extrapolate to approximately 1.38 V (peak value) differential or +12.8 dBm in the 50 Ω mixer input environment.

The differential output of the Gilbert cell mixer is open-collector to allow optimization of conversion gain and matching to the first IF filter over a wide range of frequencies and filter options. The total conversion gain is therefore determined by the real part of the effective output load, which is given by the IF filter input impedance and loss and/or fixed filter input matching networks, if present.

The voltage conversion gain can be estimated by multiplying the effective single-ended to differential transconductance value for the first mixer (0.0531 A/V) by the total effective differential output resistance. The total power conversion gain to a differential load can be estimated from the voltage conversion gain by subtracting $10 \log \frac{\text{diff\_load}}{50\ \Omega}$. The total power delivered by the mixer to the output resistance is distributed between the fixed output termination, the IF filter input impedance, as well as equivalent loss impedances associated with the finite Q of filter components. The assumption has also been made that the output impedance which the mixer sees is real, at least in the IF band.

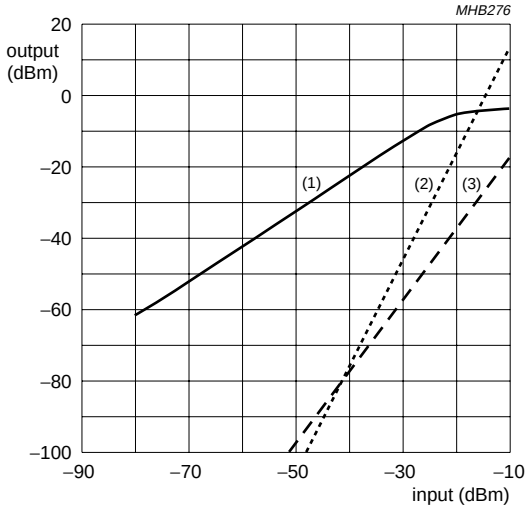
Note: The open-collector outputs of the first mixer each include internal 4 pF capacitors to ground. These capacitors should be included in the design of the first IF filter by removing 2 pF from the differential input capacitance for balanced filters and 4 pF from single-ended designs.

Therefore, the test circuit voltage conversion gain is estimated at 0.0531 A/V times the effective differential loading of approximately 440 Ω. This results in a voltage conversion gain of approximately 27.4 dBV. Subtracting 9.4 dB to convert from power in a 50 Ω environment to power into 440 Ω, we see that the first mixer delivers a total power conversion gain of approximately 18.0 dB in the test circuit. It is important to note that approximately 3 dB of this available power gain is lost in the test circuit output transformer termination and that much of this power can be recovered in application circuits.

The peak differential output voltage swing of the mixer should be limited to less than approximately 1 V (peak value) or 2 V (p-p) differential or 0.5 V (peak value) single-ended to prevent clipping by the internal output ESD protection diodes and to prevent mixer output saturation. This implies that effective differential output loads of approximately 2.5 kΩ could result in clipping at the output of the mixer.

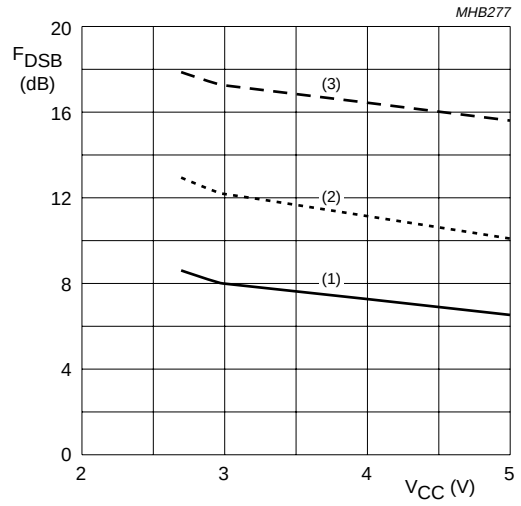
The first mixer output structure also supports single-ended first IF filter applications. By taking one of the mixer outputs to the supply rail, the other can drive a single-ended first IF filter, thereby reducing external component cost in some applications. Maintaining the same single-ended loading impedance, as in the differential case (i.e. double the effective single-ended load) results in the same peak voltage across the same load, even with only half the transconductance ½(0.0531 A/V) available. Therefore the same power is delivered to the same filter load and the conversion gain remains the same. However, an effective load of 1.25 kΩ would also bring this single-ended mixer output to the same clipping point as the full differential equivalent load of 2.5 kΩ. The maximum recommended first mixer single-sided voltage conversion gain (input to one output) is therefore approximately 32 for both single-ended and differential output applications.

The power matched Double-Side Band (DSB) noise figure of the RF mixer with preamplifier is approximately 12 dB at 1.57542 GHz from a 3 V supply.



(1) Fundamental output.
(2) 3rd-order product output.
(3) 2nd-order product output.

Fig.13 Typical first mixer fundamental, 2nd and 3rd-order product output levels as a function of input level.



(1) F_{DSB}; T_{amb} = −40 °C.
(2) F_{DSB}; T_{amb} = +25 °C.
(3) F_{DSB}; T_{amb} = +85 °C.

Fig.14 Typical RF mixer noise figure as a function of temperature and supply voltage (test board).

7.4 VCO

The VCO consists of a single transistor in common collector configuration with internal positive feedback realized by capacitors connected from emitter to ground and emitter to base. Together with the external resonator/inductor, this is a typical Colpitts circuit. With the transistor's base connected to pin 10 (TANK), the internal circuit arrangement produces a large negative input impedance at this pin.

At V_{CCA} = 3 V and T_{amb} = 27 °C the oscillator transistor is initially biased with approximately 1.5 mA of start-up current. This value is relatively constant varying from approximately 1.56 mA at T_{amb} = +120 °C to 1.4 mA at T_{amb} = –55 °C. During operation, the average currents are higher due to the large amplitudes involved leading to rectification and bias point shifting.

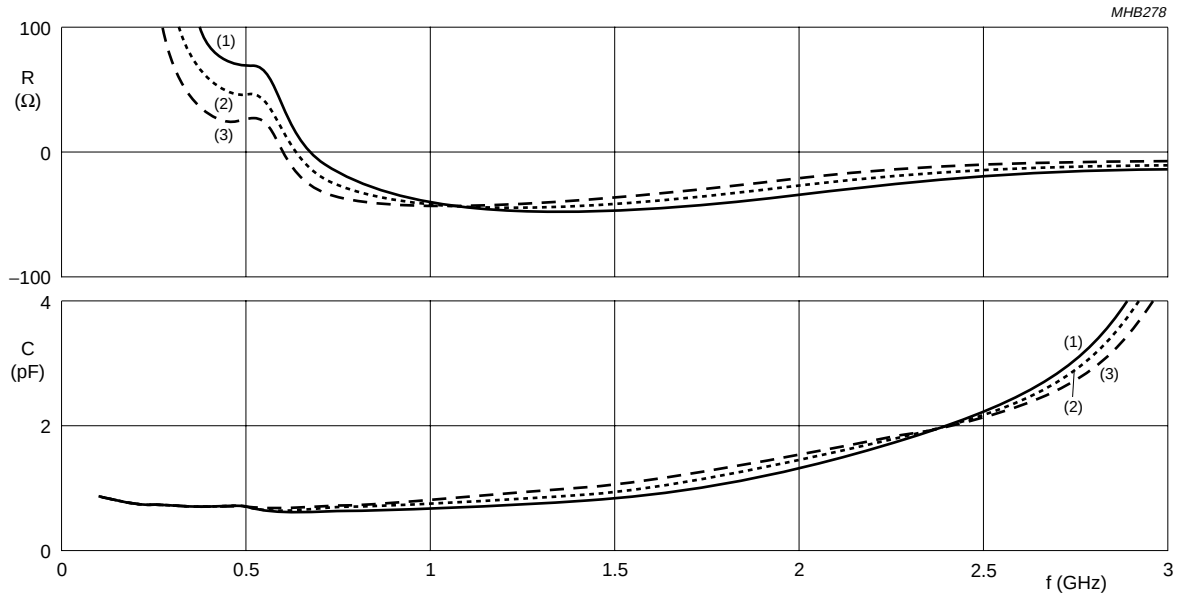
The VCO operates as a negative impedance oscillator with a suitable external inductive resonator.

Series or parallel resonators can be used, while tuning is achieved by an external varactor diode.

VCO gain as well as the out-of-loop bandwidth phase noise are dependent on the choice of external elements used here. Consequently, they should be selected with great care; their quality factor is especially important and should be as high as possible.

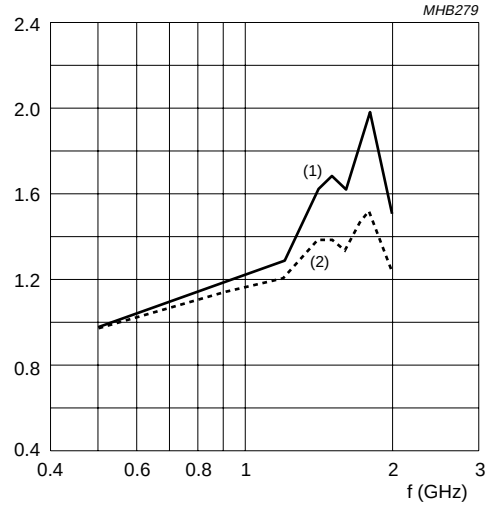
Finally, the VCO is followed by a differential buffer stage with emitter follower inputs splitting the signal to the divider and LO driver stage path to increase isolation between mixer and synthesizer and their wanted or unwanted signals.

This first buffer stage is followed by two other specialized buffer amplifier stages in the individual signal paths bringing the signal to the required levels for driving a mixer or a divider.



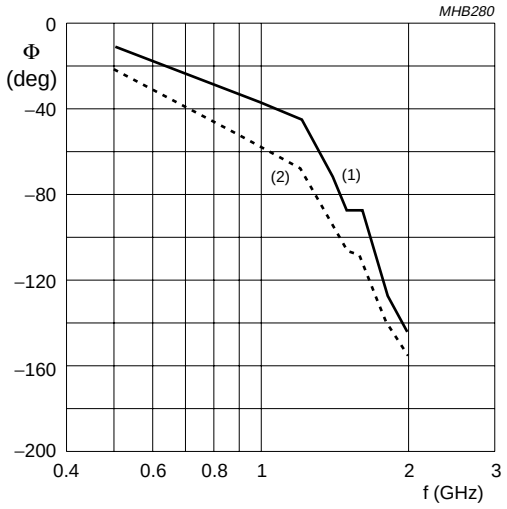
(1) T_{amb} = –55 °C.
(2) T_{amb} = +27 °C.
(3) T_{amb} = +120 °C.

Fig.15 Simulated VCO small signal negative resistance (top diagram) and capacitance (below), without strays.



(1) Corrected for strays.
(2) Raw data 3 V supply voltage.

Fig.16 Magnitude of the reflection coefficient of VCO negative resistance tank pin (measured).



(1) Corrected for strays.
(2) Raw data 3 V supply voltage.

Fig.17 Phase of the reflection coefficient of VCO negative resistance tank pin (measured).

7.5 First IF filter

The first IF filter provides four functions:

1. It provides selectivity to protect the 2nd mixer (the IF mixer) from high level spurious RF signals which pass through the wide band-pass envelope of the RF filters, typically 40 to 60 MHz.
2. The filter attenuates thermal noise and spurious signals in the 2nd mixer image band.
3. It can provide impedance matching/transformation from the RF mixer output to the IF mixer input.
4. It can reject spurious common mode and/or differential signals generated by high level local sources such as harmonics of the reference clock or sample clock.

The first IF can be structured to support a wide range of single-ended or balanced filters including LC or SAW realizations. High RF gain provides first IF signal levels high enough to accommodate first IF filter losses of 15 dB with optimum RF matching and conversion gain in the first mixer.

The Philips application board uses a 6th-order coupled resonator filter based on the butterworth response. The design method is described in the *"Handbook of FILTER SYNTHESIS"* by Anatol Zverev. The handbook tables formulate single-ended filter designs which we later convert to a balanced form.

The initial centre frequency and bandwidth were 41.82 and 4.5 MHz, respectively. The following list illustrates the tabular design 3 dB down k and q parameters from Zverev that were developed for the initial single-ended structure.

R_S = 331.4 Ω

R_L = 689.6 Ω

q_0 = 5.0; insertion loss = 4.742; q_1 = 0.8226;
q_n = 1.7115; k_{12} = 0.6567; k_{23} = 0.7060.

This tabular listing was chosen based on the desired selectivity and minimal insertion loss, which could be realized with available surface mount inductors operating with quality factors (Q) in the range of 40 to 50. The impedance level is determined by the choice of design inductance (165 nH), with foresight given to eventual balancing of the design. Maximizing the load presented to the first mixer was also a consideration. With some frequency plans stability in both the first and second IF will also need to be considered when choosing the impedance level of the design.

The handbook calculations result in a preliminary single-ended three shunt tank structure with a coupling capacitor between each tank as follows:

R_S = 331 Ω

Tank 1 = 165 nH in parallel with 81.6 pF

Coupling capacitor 1 = 6.2 pF

Tank 2 = 165 nH in parallel with 74.9 pF

Coupling capacitor 2 = 6.7 pF

Tank 3 = 165 nH in parallel with 81.1 pF

R_L = 690 Ω.

To convert this filter to a balanced design it can be mirrored in the ground plane which would result in the following balanced structure. It should be noted that the tank design inductances have doubled while the tank capacitances have halved, which can be seen by removing the virtual ground plane. The series elements remain unchanged in the balanced design, while the differential source and load have of course doubled.

R_S = 663 Ω

Tank 1 = 330 nH in parallel with 40.8 pF

Coupling capacitor 1 = 6.2 pF

Tank 2 = 330 nH in parallel with 37.5 pF

Coupling capacitor 2 = 6.7 pF

Tank 3 = 330 nH in parallel with 40.6 pF

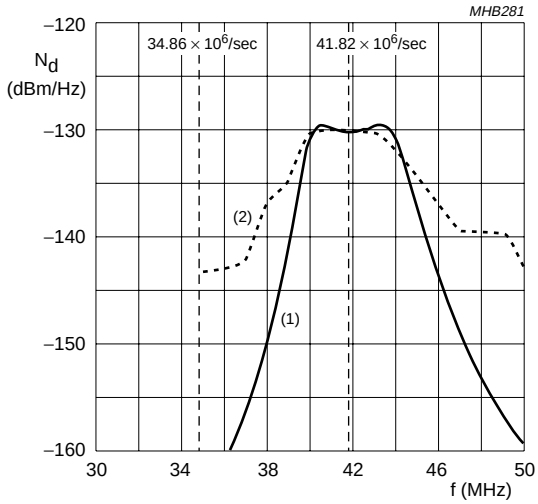
R_L = 1380 Ω.

To optimize the power developed by the first mixer its load was maximized by driving the 1380 Ω side of this filter. It was also decided to bias the output of the first mixer through Tank 3 components by breaking the former differential 330 nH inductor back into two 165 nH inductors connected to the supply which also acts as a virtual ground.

The filter was then resimulated in 'SPICE' to optimize against available discrete surface mount component values with finite quality factors. All filters must be driven by their design impedances to produce their prescribed response. Since the finite quality factors of the filter inductors emulate an equivalent shunting load of approximately $2 \times \pi \times f \times L \times Q$, the source and load terminating impedances can be increased to compensate for this parasitic element while maintaining ideal filter response and minimizing losses. In the default application, R322/306 in conjunction with the equivalent parallel resistance at the respective filter input and output give the desired terminating impedance.

The limitation imposed by image noise is illustrated in Fig.18 where the ideal calculated filter response is compared against the measured noise density at the output of the first IF filter. The single sided FET probe measured result was corrected by +6 dB to account for balanced processing and $10 \log \frac{50\ \Omega}{663\ \Omega}$ or −11.2 dB to accommodate power conversion losses. The IF noise density selectivity is seen to be limited by the available RF gain and noise figure of the first mixer. At the image frequency, 34.86 MHz, the measured noise floor is approximately 13 dB below the desired IF level at 41.82 MHz. This will result in an image contribution to the noise figure of the system of approximately 0.2 dB.

The in-band noise density can be estimated based on the single-ended voltage gain to the output of the IF filter. With the antenna thermal input level at approximately −174 dBm/Hz, noise figure of approximately 4 dB and voltage gain from the antenna to the IF filter output of approximately 47 dBV (at 5 V supply voltage), we can expect the differential noise power density to be approximately −174 dBm + 4 dB + 47 dBV + 6 dB (conversion to balanced) $- 10 \log \frac{663\ \Omega}{50\ \Omega}$ or −129 dBm/Hz. The final term converts the measured power using a high impedance FET probe, calibrated to a 50 Ω environment, to the actual 663 Ω differential filter output environment.



(1) Ideal calculated filter response.
(2) Measured filter noise density.

Fig.18 First IF filter output noise power density (application board).

7.6 Second IF mixer

The second mixer is a standard Gilbert cell mixer operating with a total tail current of 4.3 mA, which is Proportional To Absolute Temperature (PTAT). The RF input, or lower tree of the mixer, is not internally terminated other than by 5 kΩ biasing resistors to each input. With no significant emitter degeneration, the real part of the RF port input impedance is dominated by the two differential junction Rπs in parallel with the bias elements. The differential output of the Gilbert cell mixer is open-collector to allow the conversion gain and matching to the second IF filter to be optimized over a wide range of frequencies and to many types of IF filters.

The conversion voltage gain is determined by the tuned real part of the effective output load. This load may consist of the IF filter input impedance as well as fixed filter input matching compensation terminations and losses.

The voltage conversion gain can be estimated by multiplying the effective differential conversion transconductance value (0.0294 A/V) by the **total** effective differential load at the output of the mixer.

The conversion power gain is best described relative to specified mixer input and output impedance environments.

The power conversion gain is calculated by subtracting $10 \log \frac{\text{output resistance environment}}{\text{input resistance environment}}$ from the dBV value of the voltage conversion gain of the mixer. It should be noted that differential second mixer input terminations may be DC-coupled.

We can simplify and estimate the second mixer conversion gain in the default application by noting that the input impedance environment is approximately 663 Ω, while the output environment is approximately 1394 Ω. With effective output loading of 854 Ω (2.2 kΩ in parallel with $0.7 \times 2 \times 996$ Ω) the voltage conversion gain can therefore be expected to be approximately 25.1 V/V or 28 dBV. The power correction from 663 Ω at the input to 1394 Ω ($0.7 \times 2 \times 996$ Ω) at the output is −3.2 dB, so the resulting power conversion gain is approximately 24.8 dB. The factor of 0.7 in the calculation of the impedance level is explained in Section 7.7.

It should be noted that a balanced coupled k filter can be converted to a single-ended equivalent with a single-ended input impedance exactly equal to that of the full differential filter by keeping the same tank resonator components, but placing the series coupling capacitors in single-ended series (i.e. halving the differential value) and AC grounding one side of the tanks.

The demonstration board was converted from a balanced second IF filter in this manner.

To optimize the noise figure of the second mixer the input termination admittance should be reduced. However, this will be at the expense of the mixers input compression and 3rd-order intercept characteristics. Since the RF input of the IF mixer is a simple differential stage, the input −1 dB compression point and 3rd-order intercept points are relatively fixed at approximately 67 and 215 mV (peak value), respectively, in the second mixer. This results from noting that an undegenerated differential input can be expected to have an input −1 dB compression point of approximately 36.6 mV (peak value) differential. With a small additional extrinsic emitter degeneration the −1 dB compression point is raised to approximately 67 mV (peak value) differential. This is approximately −24.7 dBm in the 663 Ω second mixer GPS application input environment with the 3rd-order intercept point being approximately 10 dB higher at −14.6 dBm. Another important second mixer parameter is its 2nd-order input intercept point, which will extrapolate to approximately 79.8 V (peak value) differential or 36.8 dBm in the 663 Ω mixer input environment.

The peak output voltage swing of the IF mixer should be limited to a peak differential swing of less than approximately 1 V (peak value) or 2 V (p-p) differential to prevent clipping by the internal output ESD protection diodes and to prevent mixer output saturation. This implies that an effective differential output load of approximately 3.2 kΩ could result in clipping at the output of the mixer.

The IF mixer supports single-ended first and second IF filter applications. A single-ended input is implemented by AC bypassing one side of the IF mixer input to ground and accepting an associated drop in mixer conversion voltage gain. It should be noted that single-ended input terminations can still be DC-coupled to the mixer input pins by using the above mentioned bypass capacitor. The IF mixer output can be made single-ended by connecting the unused mixer output to the supply rail.

Extra care should be taken to characterize single-ended first IF applications. Using a single-ended second IF filter in combination with a balanced first IF filter may help reject common mode signals not rejected by the first IF filter. However, it should be noted that the differential tank capacitors of the fully differential IF filters can be replaced by common mode capacitors by doubling the differential value and connecting two of these capacitors to ground. Any distribution between these two extremes is also acceptable.

As with the RF mixer maintaining the same single-ended load as an effective differential load would result in the same voltage applied to the equivalent resistance. However, a single-ended effective load of 1.6 kΩ could also bring this mixer output to its clipping point. The maximum recommended second mixer single-sided voltage conversion gain (one input to one output) is therefore approximately 16 for both single-ended and differential output applications.

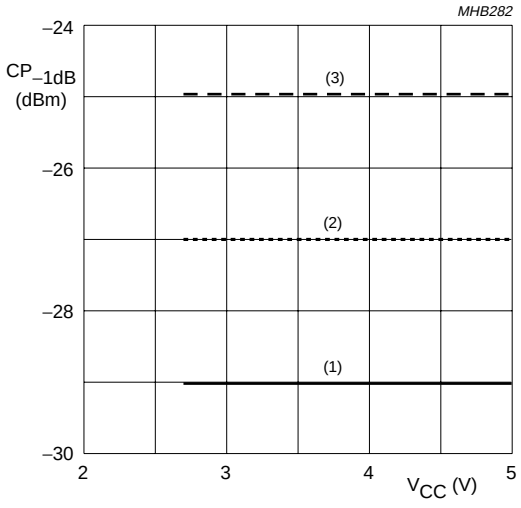
The estimated Single-Side Band (SSB) noise figure of the IF mixer is approximately 7.5 dB at T_{amb} = 27 °C from a 3 V supply with an input termination matching resistor of 2 kΩ. Removing the termination results in an expected noise figure of 4.9 dB from a 1 kΩ source. This degradation is distributed between the input termination input loss and approximately a 1.6 dB increase in the actual mixer noise figure.

The conversion gain is expected to be relatively supply independent, increasing by only approximately 0.5 dB from a supply value of 2.7 to 5.5 V. The IF mixer RF bandwidth is also expected to only increase by approximately 4%, while the mixer noise figure is expected to decrease by less than 0.1 dB as the supply is increased over the same supply range.

The IF mixer RF bandwidth, if not resonated, is dominated by the mixer differential input capacitance of approximately 1 pF.

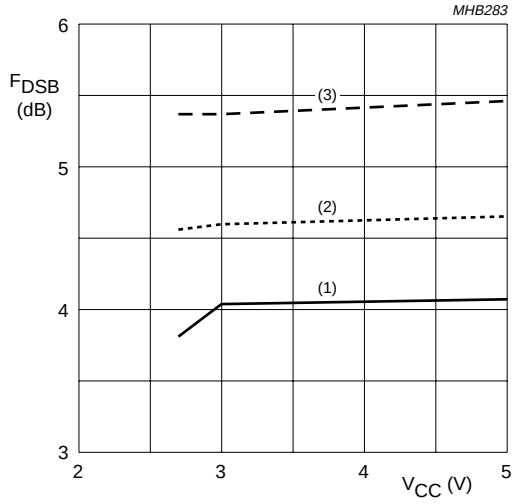
With tuned inputs, the IF mixer RF input bandwidth can be extended quite high, but practical consideration warrant that the RF filter terminating the input should provide band limiting, thereby restricting the RF high frequency roll-off to less than 200 MHz without special characterization efforts. This is also, generally, the upper limit that the programmable synthesizer supports. The noise figure of the IF mixer as well as the limiter can be expected to degrade as the operating frequencies are increased. For example, at 200 MHz in a terminated 100 Ω system the DSB noise figure of the IF mixer will increase by at least 10 dB to approximately 18 dB. If stability permits low impedance first IF filters can be matched into the IF mixer using step-up matching circuits such as baluns or transformer like tuned networks, to minimize the degradations.

The input compression point and noise figure of the IF mixer, as measured in the characterization test board, are plotted against temperature and supply voltage in Figs 19 and 20. The characterization test board employs the 1 : 16 Ω ratio transformers to provide a 50 Ω match to the 800 Ω test environment. The losses of the input and output transformers, as well as transformer insertion losses at 41.82 and 3.48 MHz, have been removed before plotting. Therefore, this graph correlates to specification and expected performance of the second mixer in the referenced 800 Ω environment.



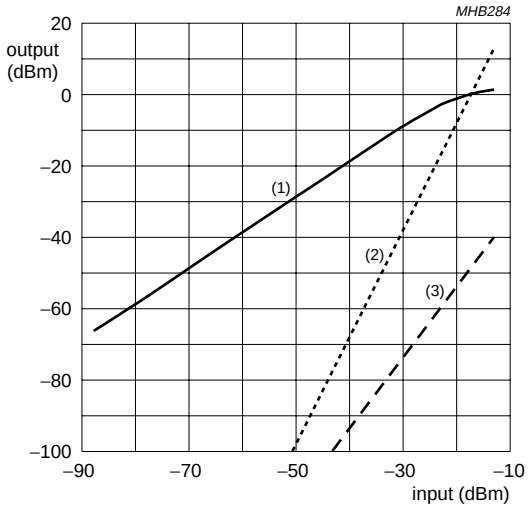
(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.19 IF mixer −1 dB input compression point (800 Ω test circuit).



(1) T_{amb} = –40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.20 IF mixer DSB noise figure (800 Ω test circuit).



(1) Fundamental output.
(2) 3rd-order product output.
(3) 2nd-order product output.

Fig.21 Typical second mixer fundamental, 2nd and 3rd-order product output levels as a function of input level (800 Ω environment).

7.7 Second IF filter

The second IF filter provides five functions:

1. It provides selectivity to protect the limiter input from spurious signals which pass through the first IF band-pass filter envelope, typically 5 MHz wide.
2. The filter attenuates undesired second mixer output products, such as the LO leak, to levels which will not block/capture the following limiter stage.
3. The filter defines and shapes the noise bandwidth to be amplitude quantized.
4. It can provide impedance matching/transformation from the IF mixer output to the limiter input while maintaining stability.
5. It can reject spurious common mode and/or differential signals generated by high level local sources such as harmonics of the reference clock or sample clock and digital processing noise from associated devices such as the SAA1575HL.

The second IF can be structured to support a wide range of single-ended or balanced filters including LC or ceramic realizations. The available system gain can provide second IF signal levels sufficient to accommodate high second IF filter losses.

The Philips application board again uses a 6th-order coupled resonator filter based on the butterworth response. The design method is described in the *"Handbook of FILTER SYNTHESIS"* by Anatol Zverev. Initially a skewed centre frequency and bandwidth were input at 3.1 and 1.75 MHz, respectively, to help overcome the asymmetry which is intrinsic in geometric low frequency band-pass filter designs as they approach DC. The following table design 3 dB down k and q parameters were used:

R_S = 548 Ω

R_L = 996 Ω

q_0 = 20.0; insertion loss = 0.958; q_1 = 0.8041; q_n = 1.4156; k_{12} = 0.7687; k_{23} = 0.6582.

This filter was originally mirrored by a virtual ground to convert it to a balanced form, but later the balanced components were converted back to a single-ended form (to reduce component count) simply by placing the balanced series capacitors in series on one side of the filter (effectively halving the capacitance value) and grounding the opposite side of the tanks where these series capacitors were removed. This effectively maintains the differential power gain while only using a single-sided output.

The filter was then resimulated in 'PSPICE' to optimize against available discrete surface mount component values. Finally the filters input and output direction were reversed to ensure that the highest impedance side was placed at the mixer output to maximize the available power developed. A 909 Ω termination was used at the output of the filter to terminate the 4.87 kΩ limiter input. This effective 766 Ω termination is somewhat lower than the initial design value of 2 × 548 Ω or 1096 Ω and therefore develops approximately −1.56 dB less power with respect to second mixer loading. The reduction of the impedance level by 30% (or a factor of 0.7) was done in order to have a large safety margin against instability of the limiter/quantizer path. Instability can be caused here by the large small-signal gain associated with this signal path in conjunction with the high signal levels present at the SIGN output. Furthermore, due to the strong non-linearities present in this signal path, LO2 leakage in conjunction with the IF2 itself can produce signals at the IF1 frequency and thus enter the IF1 filter together with the wanted signal. This impedance level reduction is passed through the second IF filter and consequently lowers the mixer 2 conversion gain by approximately 30%, too. The filter design was determined to be sufficiently tolerant to this adjustment by observing the effect on the filter's output noise response with respect to unstable peaking and maintaining the desired selectivity response. Care must be taken not to induce instability while observing the IF2 filter noise response by using a 10 : 1 divider in conjunction with a very low capacitance RF FET probe (<0.5 pF).

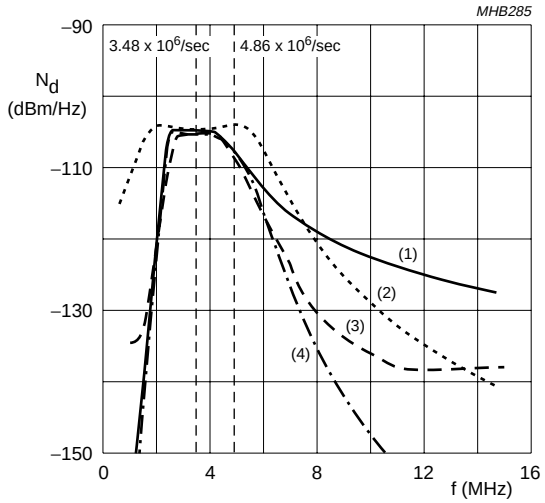
In the default application, R323/305 in conjunction with the equivalent parallel resistance at the respective filter input and output give the desired terminating impedance.

The frequency of the mixed down third harmonic of the reference oscillator is usually the most significant spurious product which is generated in the default frequency plan and must be kept at least 13 dB below the integrated noise response of the filter. For example, typical true power noise densities (Dn) for a nominal GPS demonstration board operating at 3 V are expected to be approximately −100 dBm/Hz differential at the input of the limiter and reflect the importance of designing a well matched RF system. Assuming that a somewhat lower gain variation has been realized with a noise density of approximately −105 dBm/Hz over an estimated 2 MHz noise equivalent bandwidth, it is possible to evaluate and measure the associated spurious product level that would result in a −13 dB jammer-to-noise (J/N) and 0.2 dB system noise figure degradations as follows:

The true power of a product at the output of the second IF filter in a 1 kΩ environment should be no more than −105 dBm/Hz + 63 dB − 13 dB or approximately −55 dBm. The equivalent single-sided measurement with a 50 Ω calibrated probe would be $-55\ \text{dBm} + 10\log\frac{548}{50}$ or −44.6 dBm. Figure 22 illustrates the true noise power density as measured points for this lower gain case. The filter response of the first IF filter is translated to the second IF and superimposed at the second IF to show that the 3rd harmonic reference spur at 43.2 MHz, is not filtered by this response.

Also shown is the second IF filter response and the combined first and second IF filter selectivities, which account for total observed selectivity noise response.

For difficult applications which require higher losses in the IF filters, self jamming can be minimized by choosing a reference and frequency plan which places the harmonics of the reference exactly at the second LO frequency, where they are benign.



(1) IF1 filter response superimposed on IF2 filter response.
(2) IF2 filter response (calculated).
(3) IF2 filter noise density (measured).
(4) IF1 filter response translated to IF2 frequency.

Fig.22 Second IF filter output noise density frequency response on the application board.

7.8 Time and amplitude quantization

After frequency conversion in the double-superheterodyne portion of the UAA1570HL and filtering to approximately a 2 MHz bandwidth in the second and final IF filter, the frequency translated thermal noise from the GPS pass-band around the L1 carrier is ready to be converted to a digital signal for processing by the companion GPS chip-set part (SAA1575HL). First the thermal noise's sign is determined by amplitude quantization in a 1-bit hard limiter. This asynchronous information is then time quantized by latching in a master/slave D-flip-flop to complete the analog-to-digital conversion process. Finally, this ECL digital SIGN bit data is translated to TTL levels and sent to the SAA1575HL.

Four differential stages are used to hard limit the thermal noise in the final IF. The total gain is approximately 63.9 dBV with a bandwidth of roughly 66 MHz and a noise figure of approximately 11.3 dB in a 1 kΩ environment. The parallel equivalent differential input impedance of the limiter is 4.87 kΩ in parallel with 0.3 pF. Offset control is provided through 42.5 kΩ feedback resistors from each balanced output back to the inputs. External decoupling capacitors cut the feedback loop for AC signals.

Limiter inputs as low as 25 μV (peak value differential) are resolved at the output master flip-flop DFF1 in its transparent mode. As the master flip-flop is latched positive feedback resolves metastable states. While the master flip-flop is in its transparent state the positive feedback in the slave flip-flop will resolve the remaining metastable states as it is latched.

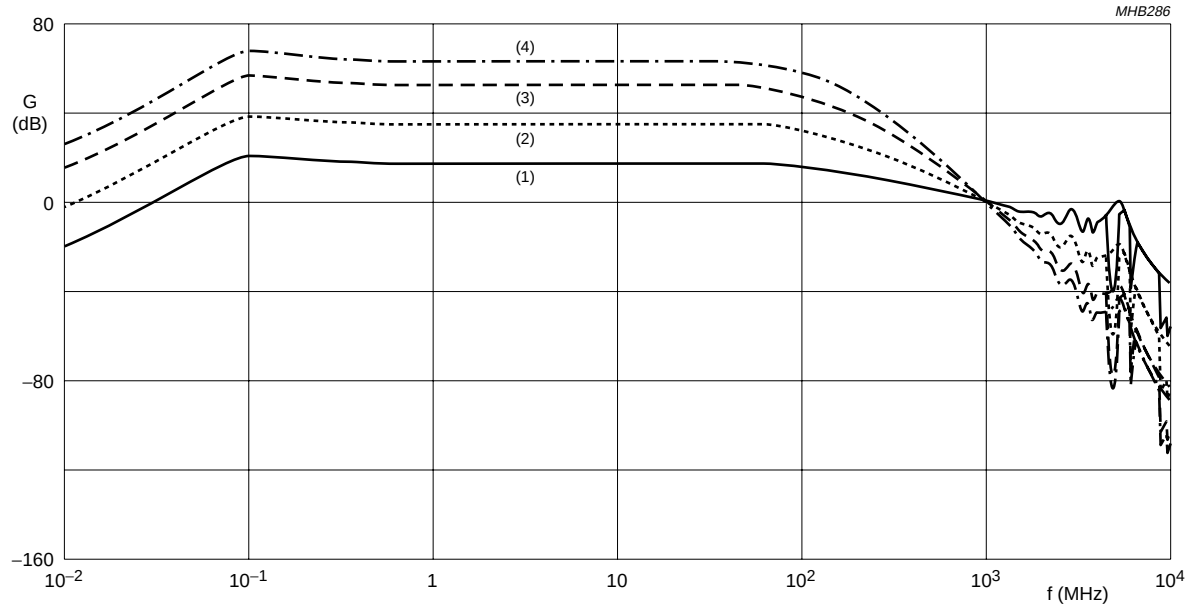
Three forms of LO leakage can block the limiter if they capture the device.

The first is LO leakage from the first mixer output which will couple into the package die pad through internal 4 pF common mode capacitors at the output of the 1st mixer. This leakage signal is effectively filtered at the 2nd IF filter output, but reappears internally on all down-bonded grounds. It appears at a level of approximately 0.5 mV (peak value differential) across the limiter input transistor bases with an assumed 1st mixer input RF offset of approximately 1 mV.

The second is LO leakage from the second mixer. Assuming 1.5 mV RF input offset, the leakage at the output of the second IF filter is expected to be approximately 500 μV (peak value differential) (−69 dBm into 1 kΩ) and sets the worst case nominal process blocking level. With a nominal −50 dBm IF thermal level at this point there is a 19 dB margin to blocking. To prevent blocking, IF filter losses should be minimized and the selectivity of the single-ended or differential second IF filter has to be designed and characterized to maintain this leakage product at least 11 dB below the integrated second IF filter thermal noise signal.

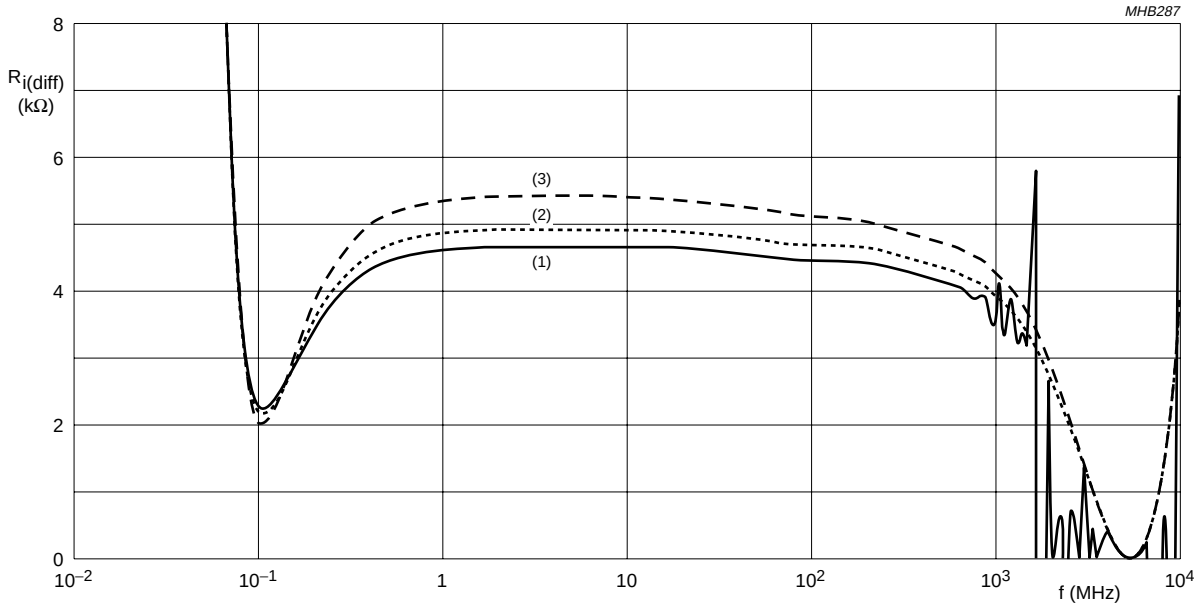
The third form of blocking can occur if LO1 leakage is sufficiently high (greater than 15 mV (peak value) on the die pad) to be injected into the 2nd mixer regulators and all down-bonded IF grounds. This results in burst of LO1 leakage at the 2nd mixer LO2 zero transition points which increase LO2 leakage peaks by factors of 10.

The gain response of the limiter from a low impedance source with no input strays is illustrated from the input to the output of each stage in Fig.23.



(1) Limiter input.
(2) 1st stage gain response.
(3) 2nd stage gain response.
(4) 3rd stage gain response.

Fig.23 Limiter input, 1st, 2nd and 3rd stage gain response as a function of frequency (simulated).



(1) T_{amb} = −55 °C.
(2) T_{amb} = +27 °C.
(3) T_{amb} = +120 °C.

Fig.24 Limiter differential input resistance as a function of frequency (simulated).

7.8.1 Clock inputs

Both the reference and the sample clock input can be driven by a Temperature Compensated Crystal Oscillator (TCXO). Typical TCXOs produce 0.5 to 1.0 V (p-p) clipped sine wave outputs. The drive capability is typically 20 kΩ in parallel with 5 pF or 10 kΩ in parallel with 10 pF. Some TCXOs are even capable of driving loads as low as 1 kΩ without buffering.

Alternatively, cost can be reduced by designing a simple discrete crystal oscillator reference, paying careful attention to temperature tolerance (±6 ppm) as well as shock and vibration characteristics.

Both UAA1570HL clock inputs, the synthesizer reference input REFIN (pin 8), and the sample clock input SCLK (pin 37), accept low level inputs and provide internal gain/squaring circuits.

The reference clock input has a high impedance with 20 kΩ in parallel with 0.07 pF. A high stability, low phase noise crystal reference source should be AC-coupled to this port. Reference inputs up to 35 MHz and levels between 50 to 500 mV (peak value) are acceptable. This source can be externally squared and attenuated before being applied. Direct sinusoidal inputs should be as large as possible within the prescribed range to optimize phase noise performance.

The sample clock input also features a high impedance of 23.3 kΩ. The sample clock input can be AC-coupled directly to the reference if the system sampling objectives are met. Alternatively, the TCXO/XO reference can be externally squared to CMOS input levels and applied to the SAA1575HL RCLK input (pin 98) and divided under firmware control to produce a signal commensurate with the sampling objective.

Due to the wide range of programmable frequency plans and sampling rates supported by the UAA1570HL, it is not possible to predict the frequencies and levels of the associated spurious products that will be generated. One significant source of potential spurs are the harmonics of the reference and sampling signals. The availability of on-chip squaring circuits provide some freedom to minimize large digital signal effects in sensitive RF circuit areas. In most cases digital sampling signal levels are acceptable as long as careful attention is paid to avoid injecting these signals or their harmonics into the pass bands of the IF filters.

The SCLK input of the UAA1570HL is self-biased at 50% of the analog supply voltage (V_{CCA}) near the internal threshold level. It is therefore possible to operate this input with levels as low as 10 mV (peak value) in order to avoid large digital signal flow on the Printed-Circuit Board (PCB) runners. This is done in the default application with a 6.8 and 3.9 kΩ resistive divider followed by a 10 pF AC coupling series capacitor in between the SAA1575HL and the UAA1570HL.

However, when it is nevertheless intended to use full CMOS or TTL levels, some attenuation is required so that the peak sample clock input does not exceed 75% of the UAA1570HL analog supply voltage. This is especially important while the UAA1570HL is operating from a lower supply (3 V) than the SAA1575HL (5 V). A resistive divider can help in these cases, but the AC coupling method described above should be preferred.

7.8.2 CMOS TO ECL SAMPLE CLOCK SQUARING CIRCUIT

The UAA1570HL internal sample clock squaring circuit allows single-ended sinusoidal clock inputs as low as 10 mV (peak value) over a frequency range from 5 to 35 MHz. The rise time of the clock output should be in the order of 25% of the maximum sampling frequency to ensure that aperture losses are less than approximately 1 dB (0.91 dB). The period of a 35 MHz clock is 28.57 ns. To keep the sampling aperture on the order of one fourth this period implies a rise time of 5.7 ns $\left(\frac{28.57\ \text{ns}}{4 \times 1.25}\right)$ is required and should also be kept with lower sampling clock rates.

Using a 14.4 MHz sampling rate test signal into the SCLK input results in good TTL eye pattern characteristics over a measured input range down to at least –25 dBm. At –35 dBm the effects of slew rate limiting begin to appear with the eye pattern closing beyond –40 dBm.

7.8.3 TIME QUANTIZATION (SAMPLER)

Two clocked D flip-flops are connected in a master/slave configuration to implement the sampling function of the 1-bit sampler. With the internal DFF clock (CLK) LOW the master flip-flop DFF1 is in its transparent mode and continuously follows the amplitude quantized limiter output. As the clock (CLK) goes HIGH the data is latched in the master flip-flop and the slave DFF2 becomes transparent to the latched output from the master flip-flop. The falling edge of the CLK signal latches the slave and again loads the limiter output into the master flip-flop. These stages also **provide additional limiting gain** for marginal input signals from the limiter.

Since the TTL/CMOS output stage is transparent the SIGN bit output is updated on the rising edge of the CLK with the master latched and the slave transparent. This implies the DSP can expect SIGN bit data to be latched on the LOW CLK state.

7.8.4 TTL OUTPUT STAGE

The TTL output stage is a variation of a totem pole modified to operate from an independent isolated supply voltage from 2.7 to 5.5 V. This supply voltage is also independent of other supply voltages used in the UAA1570HL. Circuits to minimize cross-conductance and short-circuit currents are provided.

Operating from a 2.7 V supply, V_{OL} and V_{OH} are nominally 132 mV and 1.95 V, respectively. Operating from a 5.5 V supply, V_{OL} and V_{OH} are nominally 195 mV and 4.6 V, respectively.

Typical rise times of 8 ns and fall times of 10 ns can be expected from this output driving CMOS loads.

7.8.5 1-BIT DELAYS

The rise and fall times of the TTL output with a 15 pF load are approximately 8 ns and are relatively independent of supply and temperature. A small decrease (1 to 2 ns) in rise and fall times is seen at T_{amb} = –55 °C and a small increase at T_{amb} = 120 °C (2 to 4 ns).

Typical propagation delay times through the time quantization circuitry while switching amplitude quantization states from a 5.5 V supply are:

SCLK input to TTL SIGN output 16 ns (rising edge)

SCLK input to TTL SIGN output 17.6 ns (falling edge).

7.9 Programmable synthesizer

The UAA1570HL includes a programmable synthesizer allowing the main, second LO and reference dividers to be programmed under external control via a three-wire serial control bus. Alternatively, a LOW on the STROBE input on power-up will load a 20-bit default frequency plan word and power-on options into the synthesizer registers. Frequency plans with a 2nd IF of $4 \times f_0$(1.023 MHz) = 4.092 MHz can be implemented.

7.9.1 VCO PRESCALER

After the VCO signal leaves its single-ended-to-balanced cascode buffer it is again amplified on its way to a high speed fixed divide-by-2 prescaler using a super buffer such as that described for the first mixer (see Section 7.3).

7.9.2 Main synthesizer dividers (N-path)

The main synthesizer divider path includes an additional fixed divide-by-3 prescaler preceding a programmable variable N-divider which can be programmed over a range from 64 to 127. The output of the programmable divider passes through a fixed divide-by-2 and finally an optional divide-by-1 or divide-by-2 before being applied to the phase frequency detector.

7.9.3 Second local oscillator dividers (L-path)

The second LO signal is divided down from the VCO prescaler output, first by a programmable L-divider and then by a fixed divide-by-2 before being buffered and applied to the second mixer.

7.9.4 Reference dividers (R-path)

After squaring (limiting), the reference signal is divided down first by a variable R-divider. The divide ratio ranges from 4 to 31. The variable divider is followed by an optional divide-by-1 or divide-by-2 before being applied to the phase/frequency detector.

7.10 Serial interface

The three-wire serial bus consists of DC-coupled DATA, CLOCK and STROBE CMOS level inputs. The DATA input loads serial 20-bit programming words into the synthesizer data input register on each rising edge of the CLOCK input, while the strobe line is held LOW.

The CLOCK signal should be set-up HIGH for at least 30 ns before the STROBE state is changed.

Each DATA bit should be set-up for at least 30 ns before being clocked into the register and then held for at least 30 ns. The CLOCK rate should not exceed 10 MHz and the CLOCK pulse width should be at least 30 ns.

The 20-bit DATA word definition follows in the order in which they are to be read (clocked) into the DATA register.

7.10.1 p0 and p1

The first bit read into the synthesizer should be the power-down bit, p1, which enables one of two power-down states if set HIGH. The second bit read into the register, p0, defines the type of power-down. A complete power-down of the UAA1570HL is performed if this bit is set HIGH and a partial power-down with the synthesizer remaining on if this bit is set LOW. For normal operation of the UAA1570HL both of these bits are set LOW, which are also the default values for p0,p1 = 0,0. The final p0,p1 = 1,0 state is undefined.

7.10.2 r5

Next a post reference scaler bit, r5, is set to program a divide-by-1 or divide-by-2 following the variable reference divider. With this bit set LOW the divide-by-2 post scaler is enabled and the phase frequency detector receives equal mark/space ratio reference port signals. This is the default state for this bit (r5 = 0). In the HIGH state the mark/space ratio is a function of the variable reference divider value, and the range of the reference divider is extended to lower division ratios.

7.10.3 r0, r1, r2, r3 and r4

The next five bits clocked into the DATA register are the binary equivalent value of the variable reference divider ratio. The programmable range of this divider is **4 to 31**, **continuous**. The default value is set to 4 (r0, r1, r2, r3, r4 = 0, 0, 1, 0, 0) with the Most Significant Bit (MSB) clocked into the DATA register first. The total reference division ratio is set by these five bits if r5 is set to the HIGH state. The range can be optionally doubled to **even values from 8 to 62** if r5 is set LOW. This option is set in the default case, resulting in equal mark/space ratios as described above. The total default reference division ratio is therefore 8 with (r0, r1, r2, r3, r4, r5 = 0, 0, 1, 0, 0, 0).

7.10.4 n7

As in the reference divider case the main synthesizer divider includes an optional post scaler divider following the main programmable divider. This divide-by-1 or divide-by-2 is controlled by program word bit n7. With this bit set LOW the divide-by-2 post scaler is enabled and the phase frequency detector receives equal mark/space ratio signals at its main synthesizer port. The default state for this bit is (n7 = 1) which does NOT double the total main synthesizer divide ratio as described below.

7.10.5 n0, n1, n2, n3, n4, n5 and n6

The next seven bits clocked into the DATA register are the binary equivalent value of the variable main synthesizer divider ratio. The programmable range of this divider is **64 to 127**, **continuous**. The default value is set to 71 (n0, n1, n2, n3, n4, n5, n6 = 1, 1, 1, 0, 0, 0, 1) with the MSB clocked into the DATA register first. The output of the main programmable divider includes a fixed divide-by-2 which modifies the previous range to all **even** values from **128 to 254**, inclusive. The programmable portion of the main synthesizer division ratio is set by these seven bits if n7 is set to the HIGH state as described above for the default case.

This ratio can again be **optionally doubled by setting n7 LOW**. The range is then extended to values from **256 to 508**, inclusive, in increments of **4**. Equal mark/space-ratio signals are always fed to the main synthesizer port of the phase frequency detector since the fixed divide-by-2 post scaler is always present. The main synthesizer path divisions ratio range, including the fixed divide-by-2 and divide-by-3 prescalers, is increased by a factor of 6 from **768 to 1524 in increments of 12 when n7 is set HIGH** or from **1536 to 3048 in increments of 24 if n7 is set LOW**. The total default main synthesizer path division ratio from the VCO is 12×71 or 852 with (n0, n1, n2, n3, n4, n5, n6, n7 = 1, 1, 1, 0, 0, 0, 1, 1).

7.10.6 I0, I1, I2 AND I3

The last four bits clocked into the DATA register set the programmable division ratio for the 2nd local oscillator. Again the MSB is read in first with the binary word set to a number between 4 and 15.

The default values are set to 10 (I0, I1, I2, I3 = 0, 1, 0, 1). Again a post scaler is provided with a fixed divide-by-2 value to ensure that the LO signal exhibits equal mark/space ratios driving the second mixer.
The programmable divider and fixed post scaler provide division between 8 and 30 in even increments. Since the 2nd local oscillator path from the VCO includes the divide-by-2 prescaler common to both the L-divider and N-divider paths, the total programmable 2nd local oscillator division range, relative to the VCO, is 16 to 60 in increments of 4.

With the 20-bit programming word completely clocked into the DATA register the STROBE signal is returned to a HIGH state after a minimum delay of 30 ns to latch and effect the parallel loading of the programmed word states.

7.11 The serial interface word

The complete default program word once serially loaded or loaded by default on power-up with the STROBE held LOW realizes the following frequency plan in the UAA1570HL. It should be noted that the MSB for the complete 20-bit program word is I0 and the Least Significant Bit (LSB) is p1 with the latter the first loaded into the DATA register. This is in contrast to the sequence in which the different bits determining the individual divider ratios are structured. The resulting default 20-bit word is:
I0, I1, I2, I3, n0, n1, n2, n3, n4, n5, n6, n7, r0, r1, r2, r3, r4, r5, p0, p1 =
0, 1, 0, 1, 1, 1, 1, 0, 0, 0, 1, 1, 0, 0, 1, 0, 0, 0, 0, 0.

7.12 The default frequency plan

The default synthesizer programming produces the following frequency plan:

Table 2 Frequency plan

PARAMETER	VALUE
RF input frequency	1.57542 GHz
VCO frequency	1.5336 GHz
RF image frequency	1.49178 GHz
First IF frequency	41.82 MHz
Second LO division ratio	$2 \times 10 \times 2 = 40$
Second LO frequency	38.34 MHz
Second image frequency	34.86 Hz
Second IF frequency	3.48 MHz
Reference frequency	14.4 MHz
Total main synthesizer division ratio	$2 \times 3 \times 71 \times 2 = 852$
Total reference division ratio	$2 \times 4 = 8$
Phase comparison frequency	1.8 MHz

7.13 Phase detector, charge pump and loop filter

The phase detector is of a phase and frequency sensitive digital type. In conjunction with the charge pump, it operates without a ‘dead zone’.

The charge pump itself has a single-ended output delivering or sinking current pulses with a maximum amplitude of 240 μA into the external loop filter.

The layout for the connection between the loop filter and the VCO input should be made with utmost care in order to avoid other signals entering this path.

The loop filter as chosen on the demonstration board yields a loop bandwidth of approximately 100 kHz, with a damping constant of 1. It consists of a 3.9 nF capacitor and a series resistor of 20 kΩ, both in parallel with a 150 pF capacitor.

8 OPERATING MODE SELECTION TABLES

Table 3 Programmable operating modes

MODE	p0	p1	LNA1	LNA2	VCO	MX1, MX2, 1-BIT	2nd LO	DPLL
Normal	0	0	yes	yes	yes	yes	yes	yes
Partial power-down	0	1	no	no	yes	no	no	yes
Undefined	1	0	–	–	–	–	–	–
Complete power-down	1	1	no	no	no	no	no	no

8.1 Manual selection operating modes

Some applications of the UAA1570HL may require the use of an external LNA. Since LNA1 is self contained and includes independent bias circuitry, it can be powered down simply by not connecting the respective supply pin or tying it to ground. Some considerations apply to optimize performance when using an external LNA. Generally the UAA1570HL has been optimized with approximately 15 dB of gain in the first LNA. To prevent degradation of the system noise figure or dynamic range in subsequent system functions, such as the first mixer or synthesizer, some limitations on the nominal effective gain and noise figure of external devices should be taken into account. The following values are not specified, since exceeding the recommended ranges may still result in adequate dynamic performance in some 1-bit GPS system applications.

Note: LNA2 has to be powered-up under all circumstances, i.e. its supply pin has to be connected to V_{CC} under all circumstances due to biasing constraints.

Table 4 Operation with external LNAs

MODE	$V_{CC(LNA1)}$	$V_{CC(LNA2)}$	MAXIMUM RECOMMENDED EXTERNAL GAIN INCLUDING CABLE AND FILTER LOSSES	MINIMUM RECOMMENDED EXTERNAL GAIN INCLUDING CABLE AND FILTER LOSSES	MAXIMUM RECOMMENDED EXTERNAL NOISE FIGURE INCLUDING CABLE AND FILTER LOSSES	INTERNAL CURRENT REDUCTION
Normal	yes	yes	10 dB	–3.5 dB	3.5 dB	–
LNA1 replacement; note 1	no	yes	25 dB	8 dB	4 dB	6.5 mA
LNA1/LNA2 replacement; notes 1 and 2	no	yes	41 dB	21 dB	4 dB	6.5 mA

Notes

1. The maximum external noise figure listed is that which will produce approximately a 1 dB degradation in system noise figure using the minimum recommended external gain. The maximum recommended external gain listed results in approximately 1 dB compression in the second mixer input with an in-band continuous wave jammer present (J/S = 35 dB) for nominal processed parts.
2. If a high gain external LNA is used, both LNA1 and LNA2 should be removed from the signal path. However, the LNA2 supply pin has to be connected to V_{CC} to retain power to the first mixer.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All ground pins are tied together.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{max}	maximum voltage at any pin with respect to ground		–0.5	V_{CC} + 0.5	V
V_{CCA}	analog supply voltage		–0.5	+5.5	V
V_{DDD}	digital supply voltage		–0.5	+5.5	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature	$V_{CCA} = V_{DDD} = 5$ V	–40	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V

Note

1. Human body model: Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	74	K/W

11 DC CHARACTERISTICS

T_{amb} = 25 ±2 °C; test circuit see Fig.25; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$I_{CCA(LNA1)}$	LNA1 analog supply current	V_{CCA} = 2.7 V	4.27	6.4	8.23	mA
		V_{CCA} = 3 V	4.79	6.54	8.04	mA
		V_{CCA} = 5 V	5.3	7.15	8.73	mA
$I_{CCA(LNA2)}$	LNA2 analog supply current	V_{CCA} = 2.7 V	5	7.1	8.9	mA
		V_{CCA} = 3 V	5.22	7.26	9.01	mA
		V_{CCA} = 5 V	5.68	7.92	9.83	mA
$I_{CCA(VCO)}$	VCO analog supply current	V_{CCA} = 2.7 V	2.85	3.74	4.64	mA
		V_{CCA} = 3 V	2.86	3.77	4.69	mA
		V_{CCA} = 5 V	2.89	3.82	4.76	mA
$I_{bias(MX1)}$	MX1 bias current	V_{CCA} = 2.7 V	5.18	7.49	9.03	mA
		V_{CCA} = 3 V	5.36	7.63	9.13	mA
		V_{CCA} = 5 V	5.61	8.02	9.63	mA
$I_{O(MX1)}$	MX1 output current (pins 17 and 18)	V_{CCA} = 2.7 V	3.84	4.97	5.77	mA
		V_{CCA} = 3 V	3.89	5.06	5.9	mA
		V_{CCA} = 5 V	4.06	5.39	6.33	mA
$I_{bias(MX2)}$	MX2 bias current	V_{CCA} = 2.7 V	1.67	2.36	2.88	mA
		V_{CCA} = 3 V	1.69	2.39	2.92	mA
		V_{CCA} = 5 V	1.71	2.44	2.98	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{O(MX2)}$	MX2 output current (pins 24 and 25)	V_{CCA} = 2.7 V	2.41	3.73	4.56	mA
		V_{CCA} = 3 V	2.46	3.79	4.62	mA
		V_{CCA} = 5 V	2.53	3.93	4.81	mA
$I_{CCA(LIM)}$	LIM analog supply current	V_{CCA} = 2.7 V	0.9	1.31	1.53	mA
		V_{CCA} = 3 V	0.97	1.41	1.65	mA
		V_{CCA} = 5 V	1.39	2	2.34	mA
$I_{CCA(PLL)}$	PLL analog supply current	V_{CCA} = 2.7 V	11.45	14.3	16.07	mA
		V_{CCA} = 3 V	11.67	14.98	17.06	mA
		V_{CCA} = 5 V	12.2	15.85	18.13	mA
I_{DDDL}	LOW TTL digital current	5 kΩ DC load; V_{DDD} = 2.7 V	2.9	3.75	4.6	mA
		5 kΩ DC load; V_{DDD} = 3 V	3.02	3.9	4.77	mA
		5 kΩ DC load; V_{DDD} = 5 V	3.49	4.58	5.94	mA
I_{DDDH}	HIGH TTL digital current	5 kΩ DC load; V_{DDD} = 2.7 V	0.13	0.44	0.65	mA
		5 kΩ DC load; V_{DDD} = 3 V	0.2	0.5	0.7	mA
		5 kΩ DC load; V_{DDD} = 5 V	0.47	0.88	1.15	mA
$I_{tot(wake)}$	total current (wake state)	V_{CCA} = V_{DDD} = 2.7 V	46.36	55.1	62.3	mA
		V_{CCA} = V_{DDD} = 3 V	47.54	56.66	64.26	mA
		V_{CCA} = V_{DDD} = 5 V	51.04	61.02	69.33	mA
$I_{tot(sleep)}$	total current (sleep state)	V_{CCA} = V_{DDD} = 2.7 V	–	116.2	223.5	µA
		V_{CCA} = V_{DDD} = 3 V	–	182.7	323.2	µA
		V_{CCA} = V_{DDD} = 5 V	–	648.4	900.9	µA
$I_{tot(synth)}$	total current (synthesizer state)	V_{CCA} = V_{DDD} = 2.7 V	14.36	18.08	20.4	mA
		V_{CCA} = V_{DDD} = 3 V	14.98	19.02	21.54	mA
		V_{CCA} = V_{DDD} = 5 V	15.72	20.37	23.27	mA
LNA1 and LNA2						
V_{LNAIN}	DC operating point LNA1IN and LNA2IN (pins 45 and 3)	V_{CCA} = V_{DDD} = 2.7 V	781	815	856	mV
		V_{CCA} = V_{DDD} = 3 V	784	811	843	mV
		V_{CCA} = V_{DDD} = 5 V	780	807	839	mV
V_{LNAOUT}	DC operating point LNA1OUT and LNA2OUT (pins 48 and 6)	V_{CCA} = V_{DDD} = 2.7 V	1.02	1.48	1.71	V
		V_{CCA} = V_{DDD} = 3 V	1.284	1.75	1.983	V
		V_{CCA} = V_{DDD} = 5 V	3.115	3.629	3.886	V
Reference input; pin 8						
V_{REFIN}	DC operating point REFIN	V_{CCA} = 2.7 V	1.56	1.69	1.87	V
		V_{CCA} = 3 V	1.87	1.99	2.15	V
		V_{CCA} = 5 V	3.84	3.99	4.19	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VCO; pin 10						
V_{TANK}	DC operating point TANK	V_{CCA} = 2.7 V	1.825	1.918	2.01	V
		V_{CCA} = 3 V	1.822	1.916	2.011	V
		V_{CCA} = 5 V	1.818	1.918	2.018	V
Mixer 1; pin 14						
V_{MX1IN}	DC operating point MX1IN	V_{CCA} = 2.7 V	800	818	846	mV
		V_{CCA} = 3 V	797	814	839	mV
		V_{CCA} = 5 V	792	810	837	mV
Mixer 2; pins 21 and 22						
V_{IF2IN}	DC operating point IF2INN and IF2INP	V_{CCA} = 2.7 V	939	983	1011	mV
		V_{CCA} = 3 V	937	981	1009	mV
		V_{CCA} = 5 V	936	980	1008	mV
Limiter						
V_{BFC}	DC operating point BFCN and BFCP (pins 27 and 30)	V_{CCA} = 2.7 V	1.276	1.696	1.831	V
		V_{CCA} = 3 V	1.578	1.998	2.133	V
		V_{CCA} = 5 V	3.579	3.999	4.134	V
V_{LIMIN}	DC operating point LIMINN and LIMINP (pins 28 and 29)	V_{CCA} = 2.7 V	1.276	1.696	1.831	V
		V_{CCA} = 3 V	1.578	1.998	2.133	V
		V_{CCA} = 5 V	3.579	3.999	4.134	V
SIGN bit output (TTL); pin 34						
$V_{OL(SIGN)}$	LOW-level DC operating point output SIGN	5 kΩ DC load; V_{CCA} = 2.7 V	45	130.6	160.8	mV
		5 kΩ DC load; V_{CCA} = 3 V	42	127	157	mV
		5 kΩ DC load; V_{CCA} = 5 V	–	71.8	–	mV
$V_{OH(SIGN)}$	HIGH-level DC operating point output SIGN	5 kΩ DC load; V_{CCA} = 2.7 V	1.589	1.876	1.956	V
		5 kΩ DC load; V_{CCA} = 3 V	1.794	2.168	2.273	V
		5 kΩ DC load; V_{CCA} = 5 V	3.566	4.1	4.251	V
SCLK input (CMOS to ECL); pin 37						
$V_{th(SCLK)}$	DC operating point SCLK threshold [$0.5 \times V_{CCA(LIM)}$ (pin 31)]	$V_{CCA} = V_{DDD}$ = 2.7 V	1.329	1.341	1.353	V
		$V_{CCA} = V_{DDD}$ = 3 V	1.479	1.491	1.503	V
		$V_{CCA} = V_{DDD}$ = 5 V	2.478	2.499	2.519	V
COMP; pin 40						
$V_{O(COMP)}$	charge pump output voltage swing	V_{CCA} = 2.7 V	0.2	–	2.1	V
		V_{CCA} = 3 V	0.2	–	2.4	V
		V_{CCA} = 5 V	0.2	–	4.4	V
$I_{cp(max)}$	maximum current sinked or sourced by the charge pump	V_{CCA} = 2.7 V	–	240	–	µA
		V_{CCA} = 3 V	–	240	–	µA
		V_{CCA} = 5 V	–	240	–	µA

12 AC CHARACTERISTICS

T_{amb} = 25 ±2 °C; default frequency plan; test circuit see Fig.25; unless otherwise specified. S-parameters given below (S11, S22 and S12) are design goals which should be achieved in order to reach the other given values. They are depending on application.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System performance						
F_{RX}	receiver noise figure (LNA1 input to SIGN bit output)	f = 1.57542 GHz; V_{CCA} = 3 V; note 1	3.8	4.5	5.2	dB
S	sensitivity	–3 dB; note 2	–103	–106	–109	dBm
LNA 1; note 3						
$S21_{LNA1}$	power gain	50 Ω matched input and output				
		V_{CCA} = 2.7 V	12.3	15.4	18.1	dB
		V_{CCA} = 3 V	12.4	15.7	18.5	dB
		V_{CCA} = 5 V	12.9	16.6	19.7	dB
$S11_{LNA1}$	input reflection coefficient	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–	–18	–16.3	dB
		V_{CCA} = 3 V	–	–18	–16.2	dB
		V_{CCA} = 5 V	–	–18	–16.2	dB
$S12_{LNA1}$	reverse isolation	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–	–38.9	–29.9	dB
		V_{CCA} = 3 V	–	–38	–29	dB
		V_{CCA} = 5 V	–	–35.6	–26.6	dB
$S22_{LNA1}$	output reflection coefficient	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–	–21.2	–12.7	dB
		V_{CCA} = 3 V	–	–18	–13.4	dB
		V_{CCA} = 5 V	–	–10.8	–8.7	dB
$IP3_{LNA1}$	3rd-order input intercept point	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–17	–13.4	–	dBm
		V_{CCA} = 3 V	–16.8	–13.2	–	dBm
		V_{CCA} = 5 V	–16.6	–12.6	–	dBm
$IP2_{LNA1}$	2nd-order input intercept point	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–	7.7	–	dBm
		V_{CCA} = 3 V	–	7.9	–	dBm
		V_{CCA} = 5 V	–	8.6	–	dBm

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$CP_{-1dB(LNA1)}$	–1 dB input compression point	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–26.6	–22.2	–	dBm
		V_{CCA} = 3 V	–26.6	–22.2	–	dBm
		V_{CCA} = 5 V	–28.2	–22	–	dBm
F_{LNA1}	noise figure LNA1	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–	3.6	4.7	dB
		V_{CCA} = 3 V	–	3.6	4.3	dB
		V_{CCA} = 5 V	–	3.6	4.2	dB
LNA 2; note 3						
$S21_{LNA2}$	power gain	50 Ω matched input and output				
		V_{CCA} = 2.7 V	11.4	14.8	18.2	dB
		V_{CCA} = 3 V	12.1	15.3	18.5	dB
		V_{CCA} = 5 V	11.6	15.9	20.3	dB
$S11_{LNA2}$	input reflection coefficient	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–	–18.5	–14.2	dB
		V_{CCA} = 3 V	–	–18	–13.5	dB
		V_{CCA} = 5 V	–	–17.1	–12.6	dB
$S12_{LNA2}$	reverse isolation	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–	–35.8	–26.8	dB
		V_{CCA} = 3 V	–	–34.9	–25.9	dB
		V_{CCA} = 5 V	–	–32.5	–23.5	dB
$S22_{LNA2}$	output reflection coefficient	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–	–18.4	–14.9	dB
		V_{CCA} = 3 V	–	–18	–15	dB
		V_{CCA} = 5 V	–	–15.7	–14.1	dB
$IP3_{LNA2}$	3rd-order input intercept point	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–28.6	–13.5	–	dBm
		V_{CCA} = 3 V	–16.9	–12.8	–	dBm
		V_{CCA} = 5 V	–16.3	–12	–	dBm
$IP2_{LNA2}$	2nd-order input intercept point	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–	7.7	–	dBm
		V_{CCA} = 3 V	–	7.9	–	dBm
		V_{CCA} = 5 V	–	8.6	–	dBm

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$CP_{-1dB(LNA2)}$	–1 dB input compression point	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–28.1	–22.4	–	dBm
		V_{CCA} = 3 V	–27.1	–22.6	–	dBm
		V_{CCA} = 5 V	–26.6	–22.2	–	dBm
F_{LNA2}	noise figure LNA2	50 Ω matched input and output				
		V_{CCA} = 2.7 V	–	3.7	4.4	dB
		V_{CCA} = 3 V	–	3.7	4.3	dB
		V_{CCA} = 5 V	–	3.8	6.3	dB
Mixer 1						
$Y21_{MX1}$	conversion transconductance	50 Ω matched input and 800 Ω matched output; note 4				
		V_{CCA} = 2.7 V	0.032	0.0513	0.0813	A/V
		V_{CCA} = 3 V	0.0334	0.0531	0.0837	A/V
		V_{CCA} = 5 V	0.0403	0.0593	0.0889	A/V
$G_{conv(v)}$	voltage conversion gain	50 Ω matched input and output; note 5				
		V_{CCA} = 2.7 V	23.9	27.1	32.1	dBV
		V_{CCA} = 3 V	24.3	27.5	32.4	dBV
		V_{CCA} = 5 V	25.7	28.4	32.7	dBV
$G_{conv(p)}$	power conversion gain	50 Ω matched input and 800 Ω matched output; note 6				
		V_{CCA} = 2.7 V	14.5	17.7	22.6	dB
		V_{CCA} = 3 V	14.8	18	22.9	dB
		V_{CCA} = 5 V	16.2	18.9	23.2	dB
$S11_{MX1}$	input reflection coefficient	50 Ω matched input and 800 Ω matched output				
		V_{CCA} = 2.7 V	–	–17.8	–15.9	dB
		V_{CCA} = 3 V	–	–18	–16.2	dB
		V_{CCA} = 5 V	–	–18.9	–16.6	dB
$CP_{-1dB(MX1)}$	–1 dB input compression point	50 Ω matched input and 800 Ω matched output; note 6				
		V_{CCA} = 2.7 V	–29.7	–25.4	–	dBm
		V_{CCA} = 3 V	–31.2	–25.4	–	dBm
		V_{CCA} = 5 V	–31	–25.4	–	dBm

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$F_{DSB(MX1)}$	double-side band noise figure MX1	50 Ω matched input and 800 Ω matched output; note 6				
		V_{CCA} = 2.7 V	–	12.8	16.8	dB
		V_{CCA} = 3 V	–	12	15.8	dB
		V_{CCA} = 5 V	–	10	12.7	dB
Mixer 2						
$Y21_{MX2}$	conversion transconductance	800 Ω matched input and output; note 7				
		V_{CCA} = 2.7 V	0.0252	0.0293	0.0344	A/V
		V_{CCA} = 3 V	0.0171	0.0294	0.0438	A/V
		V_{CCA} = 5 V	0.0258	0.03	0.0352	A/V
$G_{conv(v)}$	voltage conversion gain	800 Ω matched input and output; note 8				
		V_{CCA} = 2.7 V	17.8	21.4	25.5	dBV
		V_{CCA} = 3 V	17.8	21.4	25.6	dBV
		V_{CCA} = 5 V	18	21.6	25.8	dBV
$G_{conv(p)}$	power conversion gain	800 Ω matched input and output; note 9				
		V_{CCA} = 2.7 V	17.8	21.4	25.6	dB
		V_{CCA} = 3 V	17.8	21.4	25.6	dB
		V_{CCA} = 5 V	18	21.6	25.8	dB
$R_{i(dif)}$	differential input resistance	note 10				
		V_{CCA} = 2.7 V	1.6	2.05	2.45	kΩ
		V_{CCA} = 3 V	1.6	2.05	2.45	kΩ
		V_{CCA} = 5 V	1.6	2.05	2.45	kΩ
$C_{i(dif)}$	differential input capacitance	note 10				
		V_{CCA} = 2.7 V	0.9	1	1.1	pF
		V_{CCA} = 3 V	0.9	1	1.1	pF
		V_{CCA} = 5 V	0.9	1	1.1	pF
$CP_{-1dB(MX2)(M)}$	−1 dB differential input compression point	800 Ω matched input and output (peak value); note 9				
		V_{CCA} = 2.7 V	50	67.2	84.3	mV
		V_{CCA} = 3 V	44	67.2	90.3	mV
		V_{CCA} = 5 V	44.6	67.2	89.8	mV
$F_{DSB(MX2)}$	double-side band noise figure MX2	800 Ω matched input and output; note 9				
		V_{CCA} = 2.7 V	–	4.8	6.1	dB
		V_{CCA} = 3 V	–	4.8	5.5	dB
		V_{CCA} = 5 V	–	4.8	7	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Limiter						
$G_{v(lim)}$	small signal limiting voltage gain	800 Ω matched limiter input to internal limiter output				
		V_{CCA} = 2.7 V	–	64.5	–	dB
		V_{CCA} = 3 V	61.8	65.7	69.5	dB
		V_{CCA} = 5 V	–	66.0	–	dB
$R_{i(dif)}$	differential input resistance	note 10				
		V_{CCA} = 2.7 V	4.10	4.85	6.67	kΩ
		V_{CCA} = 3 V	4.11	4.87	6.69	kΩ
		V_{CCA} = 5 V	4.15	4.92	6.76	kΩ
$C_{i(dif)}$	differential input capacitance	note 10	0.25	0.28	0.31	pF
F_{lim}	limiter noise figure referred to 800 Ω	800 Ω matched source; note 11				
		V_{CCA} = 2.7 V	–	16.5	–	dB
		V_{CCA} = 3 V	12.0	15.0	17.0	dB
		V_{CCA} = 5 V	–	11.0	–	dB
$S_{lim(M)}$	differential limiter sensitivity	800 Ω matched source (peak value); note 11				
		V_{CCA} = 2.7 V	46	100	154	μV
		V_{CCA} = 3 V	68.8	100	131.2	μV
		V_{CCA} = 5 V	46	100	154	μV
SCLK (sample clock conditioning)						
$G_{v(SCLK)}$	small signal voltage gain	50 Ω terminated SCLK input to internal DFF clock input				
		V_{CCA} = 2.7 V	–	38.9	–	dB
		V_{CCA} = 3 V	–	39.0	–	dB
		V_{CCA} = 5 V	–	39.6	–	dB
$R_{i(SCLK)}$	input resistance	note 10				
		V_{CCA} = 2.7 V	–	23.2	–	kΩ
		V_{CCA} = 3 V	–	23.4	–	kΩ
		V_{CCA} = 5 V	–	23.7	–	kΩ
$C_{i(SCLK)}$	input capacitance	note 10				
		V_{CCA} = 2.7 V	–	0.86	–	pF
		V_{CCA} = 3 V	–	0.84	–	pF
		V_{CCA} = 5 V	–	0.74	–	pF
B_{SCLK}	small signal bandwidth	50 Ω terminated source	–	42.5	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$S_{SCLK(M)}$	SCLK sensitivity	50 Ω terminated source (peak value)				
		V_{CCA} = 2.7 V	10	–	–	mV
		V_{CCA} = 3 V	10	–	–	mV
		V_{CCA} = 5 V	10	–	–	mV
VCO						
$R_{i(1.4GHz)(seqn)}$	series equivalent negative resistance at 1.4 GHz (only for reference)	V_{CCA} = 2.7 V	–	–14.5	–	Ω
		V_{CCA} = 3 V	–	–14.7	–	Ω
		V_{CCA} = 5 V	–	–15.0	–	Ω
$C_{i(1.4GHz)(seq)}$	series equivalent capacitance at 1.4 GHz (only for reference)	V_{CCA} = 2.7 V	–	2.61	–	pF
		V_{CCA} = 3 V	–	2.56	–	pF
		V_{CCA} = 5 V	–	2.47	–	pF
$R_{i(1.5GHz)(seqn)}$	series equivalent negative resistance at 1.5 GHz (only for reference)	V_{CCA} = 2.7 V	–	–12.1	–	Ω
		V_{CCA} = 3 V	–	–12.3	–	Ω
		V_{CCA} = 5 V	–	–12.6	–	Ω
$C_{i(1.5GHz)(seq)}$	series equivalent capacitance at 1.5 GHz (only for reference)	V_{CCA} = 2.7 V	–	3.06	–	pF
		V_{CCA} = 3 V	–	3.00	–	pF
		V_{CCA} = 5 V	–	2.90	–	pF
$R_{i(1.6GHz)(seqn)}$	series equivalent negative resistance at 1.6 GHz (only for reference)	V_{CCA} = 2.7 V	–	–10.4	–	Ω
		V_{CCA} = 3 V	–	–10.7	–	Ω
		V_{CCA} = 5 V	–	–11.0	–	Ω
$C_{i(1.6GHz)(seq)}$	series equivalent capacitance at 1.6 GHz (only for reference)	V_{CCA} = 2.7 V	–	2.94	–	pF
		V_{CCA} = 3 V	–	2.89	–	pF
		V_{CCA} = 5 V	–	2.78	–	pF
$V_{VCO(M)}$	first LO signal level (peak value)	note 12				
		V_{CCA} = 2.7 V	–	–	0.9	V
		V_{CCA} = 3 V	–	–	0.9	V
		V_{CCA} = 5 V	–	–	0.9	V
$K_{VCO(av)}$	average VCO gain in typical application	V_{CCA} = 2.7 V	–	84.84	–	MHz/V
		V_{CCA} = 3 V	61.7	96.62	101	MHz/V
		V_{CCA} = 5 V	–	67.15	–	MHz/V
Synthesizer						
$f_{i(ref)}$	reference input frequency		1	14.4	35	MHz
$P_{i(ref)}$	reference input level	relative to 50 Ω	–32.27	+5	+9.75	dBm
$Z_{i(ref)}$	reference input impedance		–	20	–	kΩ
PN_{10kHz}	PLL phase noise 10 kHz offset	note 12				
		V_{CCA} = 2.7 V	–	72	–	dBc/Hz
		V_{CCA} = 3 V	–	72	–	dBc/Hz
		V_{CCA} = 5 V	–	72	–	dBc/Hz

Notes

1. The noise figure of the GPS application board is estimated from the −3 dB sensitivity testing by substitution using a 10 dB external LNA with a noise figure of less than 2 dB.
2. The sensitivity of the GPS application board is measured by recording the RF level required to observe a 3 dB drop in the sampled L1 signal, after sampling to 1.32 MHz product [3.48 MHz(IF2) − 4.8 MHz (f_{sample})] in the SIGN bit output.
3. At L1 (1.57542 GHz) with a −35 dBm input with matching components tuned at 3 V at T_{amb} = 25 °C.
4. From the matched single-ended RF mixer preamplifier input to the differential IF output of MX1.
5. From the matched single-ended RF mixer preamplifier input to the differential IF output of MX1 across an equivalent 400 Ω loading of an 800 Ω termination and transformer differential load (4 : 1 ratio to a 50 Ω measurement termination).
6. From the matched single-ended RF input to the differential IF output of MX1 into an equivalent 400 Ω differential load. Half of the delivered conversion gain power is delivered to an 800 Ω termination, with the remaining power transformed (z-ratio 16 : 1) down and delivered to a 50 Ω termination. The available tabulated power is 3 dB higher than the power delivered to the 50 Ω termination.
7. From the differential transformer matched RF input to the differential IF output of MX2.
8. From the differential transformer matched RF input to the differential IF output of MX2 across an equivalent 400 Ω loading of an 800 Ω termination and transformer differential load (4 : 1 ratio to a 50 Ω measurement termination).
9. From the differential transformer matched RF input to the differential IF output of MX2 into an equivalent 400 Ω differential load. Half of the delivered conversion gain power is delivered to an 800 Ω termination, with the remaining power transformed (z-ratio 16 : 1) down and delivered to a 50 Ω termination. The available tabulated power is 3 dB higher than the power delivered to the 50 Ω termination. The back-to-back 50 Ω : 800 Ω : 800 Ω : 50 Ω response characteristics of mini circuits RF transformer T16-6T are provided in Fig.11.
10. Simulated values without external pin strays.
11. Due to test time constraints the sensitivity of the limiter is measured indirectly in the current ATE test definition. Bench characterization using a 1 : 16 Ω ratio transformer established −3 dB limiting sensitivity at 100 μV (peak value) across the 800 Ω terminated transformer output at the limiter input. This sensitivity is not due to gain limitations, but rather intrinsic complex broadband noise characteristics over an estimated 800 MHz equivalent sampled spectral bandwidth. However, the measured −82 dBm sensitivity of the device in an 800 Ω operating environment defines the minimum level which can be detected in the sampling quantizer. The ATE test method results perform about 8.2 dBV better than bench characterization using conventional −3 dB limiting. The specification results represent the ATE results degraded by 8.2 dB. The limiter noise figure test is being degraded by 800 Ω transformer termination loss. Only a weak and remote correlation exist between highly non-linear noise figure measurements made on a time sampled quantizer output and linear simulation results.
12. The peak VCO tank swing and phase noise are measured in the default application board. With high Q resonators the peak voltage swing at the resonator pin should be limited to <0.8 V (peak value). A de-biasing resistor can be added from the TANK pin to ground.

13 CHARACTERIZATION TEST CIRCUIT

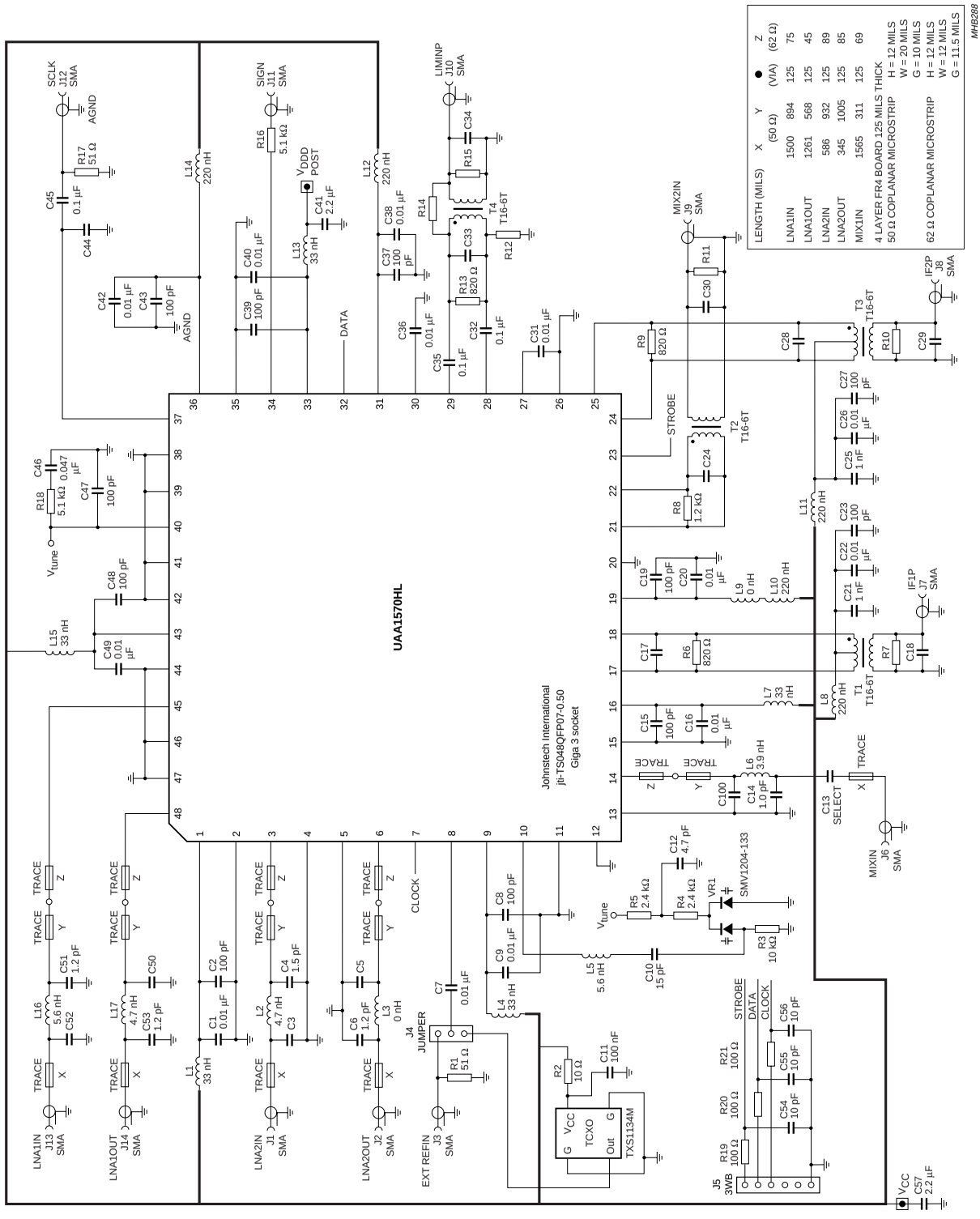


Fig.25 Characterization test circuit.

Table 5 Component list for Fig.25

COMPONENT	COMPONENT CHARACTERISTICS		
	VALUE	TOLERANCE	PACKAGE
C1, C7, C9, C16, C20, C22, C26, C31, C36, C38, C40, C42 and C49	0.01 μF	10%	603
C2, C8, C15, C19, C23, C27, C37, C39, C43, C47 and C48	100 pF	5%	603
C3, C5, C50 and C100	not loaded	–	–
C4	1.5 pF	±0.25 pF	805
C6, C51 and C53	1.2 pF	±0.25 pF	805
C10	15 pF	5%	603
C11[1]	not loaded	–	–
C12	4.7 pF	±0.25 pF	603
C13	short	–	–
C14	1.0 pF	±0.25 pF	805
C17, C18, C24, C28, C29 and C30	not loaded	–	–
C21 and C25	1000 pF	5%	603
C32, C35 and C45	0.1 μF	10%	603
C33, C34 and C44	not loaded	–	–
C41 and C57[2]	2.2 μF	10%	–
C46	0.047 μF	10%	603
C52	not loaded	–	–
C54 to C56[3]	10 pF	5%	603
R1 and R17	51 Ω	1%	603
R2[4]	not loaded	–	–
R3	10 kΩ	1%	603
R4 and R5	2.4 kΩ	1%	603
R6, R9 and R13	820 Ω	1%	603
R7, R10 and R11	not loaded	–	–
R8	1.2 kΩ	1%	603
R12	not loaded	–	–
R14	not loaded	–	–
R15	not loaded	–	–
R16[5]	5.1 kΩ	1%	603
R18	5.1 kΩ	1%	603
R19, R20 and R21	100 Ω	5%	603
L1, L4, L7, L13 and L15	33 nH	10%	805 (Coilcraft)
L2 and L17	4.7 nH	±0.3 nH	805 (Toko)
L3	short	–	–
L5	5.6 nH	±0.3 nH	603 (Toko)
L6	3.9 nH	±0.3 nH	805 (Toko)
L8, L10, L11, L12 and L14	220 nH	10%	805 (Coilcraft)
L9	short	–	–

COMPONENT	COMPONENT CHARACTERISTICS		
	VALUE	TOLERANCE	PACKAGE
L16	5.6 nH	±0.3 nH	805 (Toko)
VR1	SMV1204-133 low capacitance varactor (Alpha)		
T1 to T4	transformer Mini circuits T16-6T-KK81/W38, 16 : 1 impedance ratio		
TCXO(6)	not loaded	–	–

Notes

1. 0.1 μF, 10%, 603 if used.
2. 16 V voltage rating.
3. For default frequency plan: short.
4. 10 Ω, 5%, 603 if used.
5. For AC characterization, terminate with 50 Ω to ground and use a 50 Ω input test instrument.
6. TXS1134MTEW if used.

14 DEFAULT APPLICATION AND DEMONSTRATION BOARD

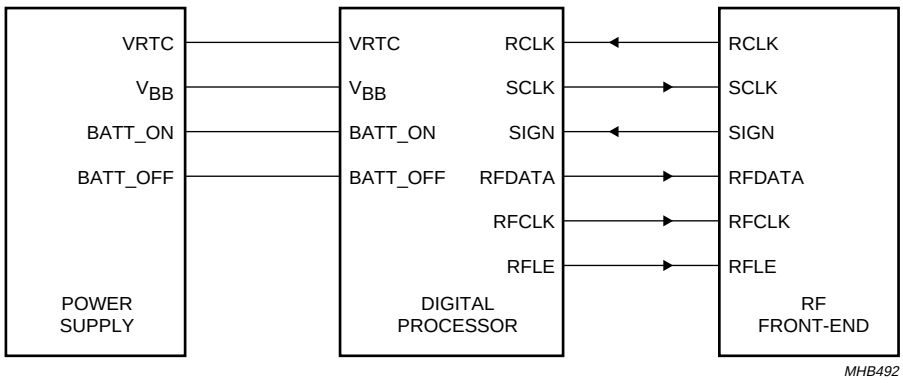


Fig.26 Overall schematic.

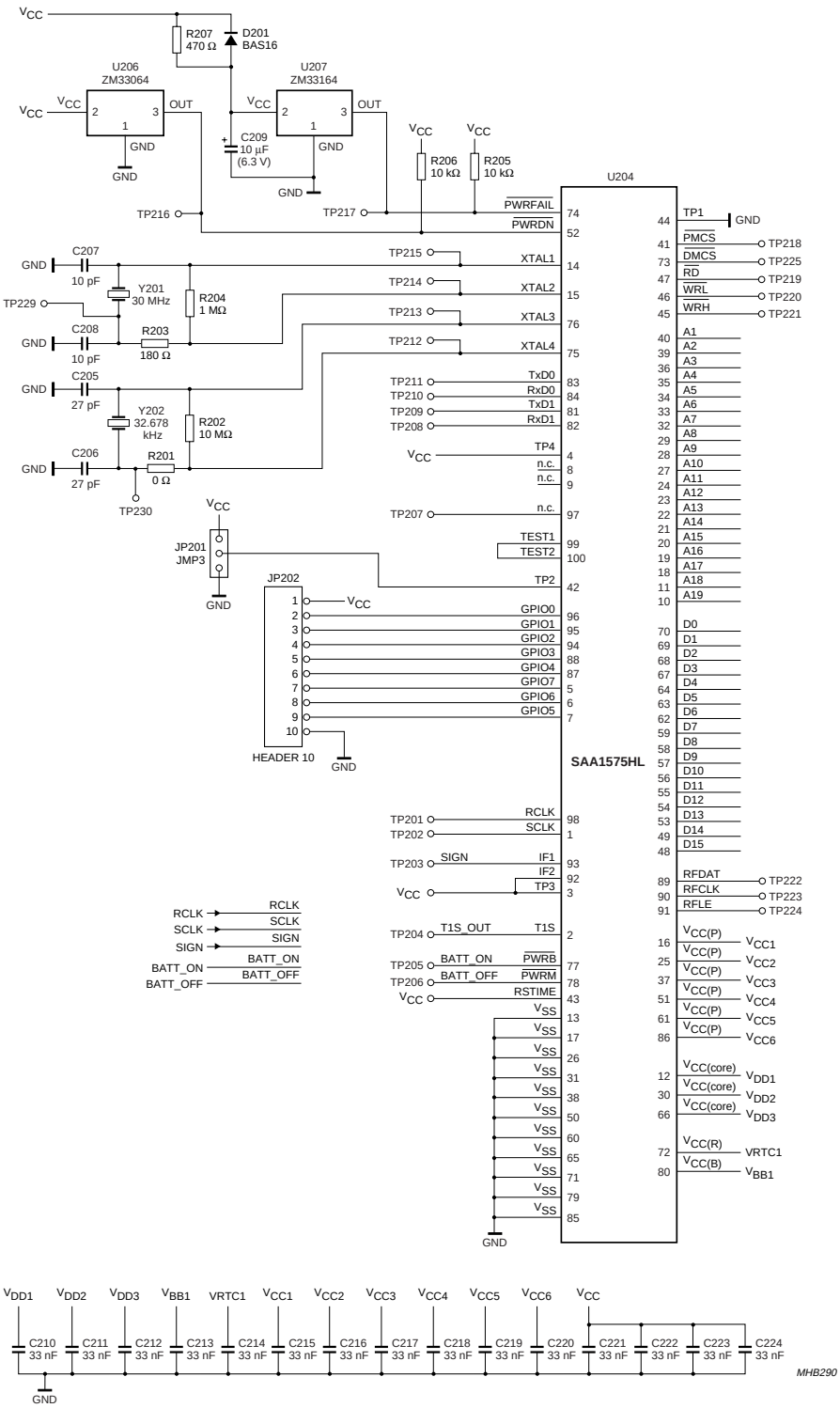


Fig.27 Baseband circuitry (continued in Fig.28).

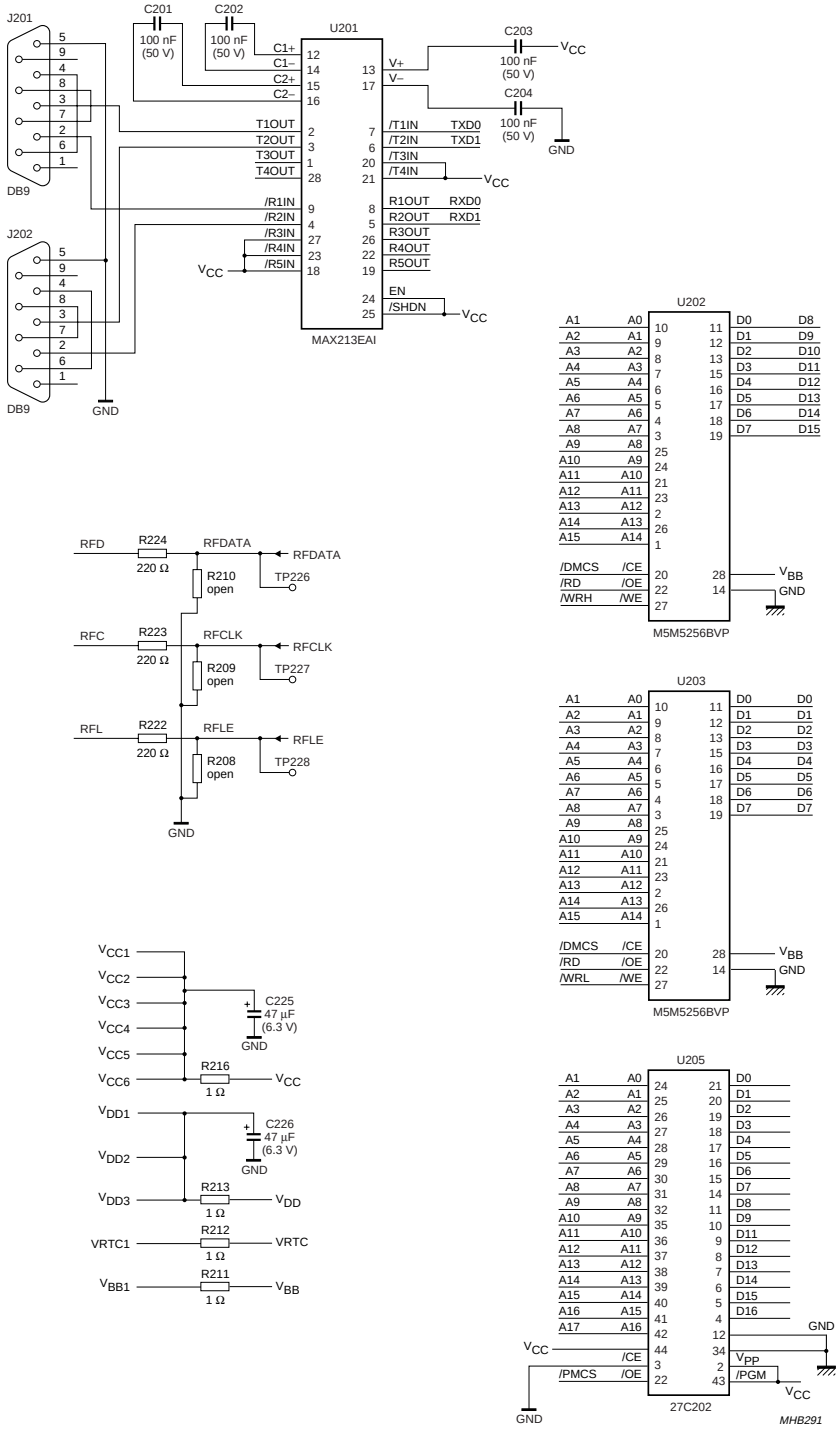


Fig.28 Baseband circuitry (continued from Fig.27).

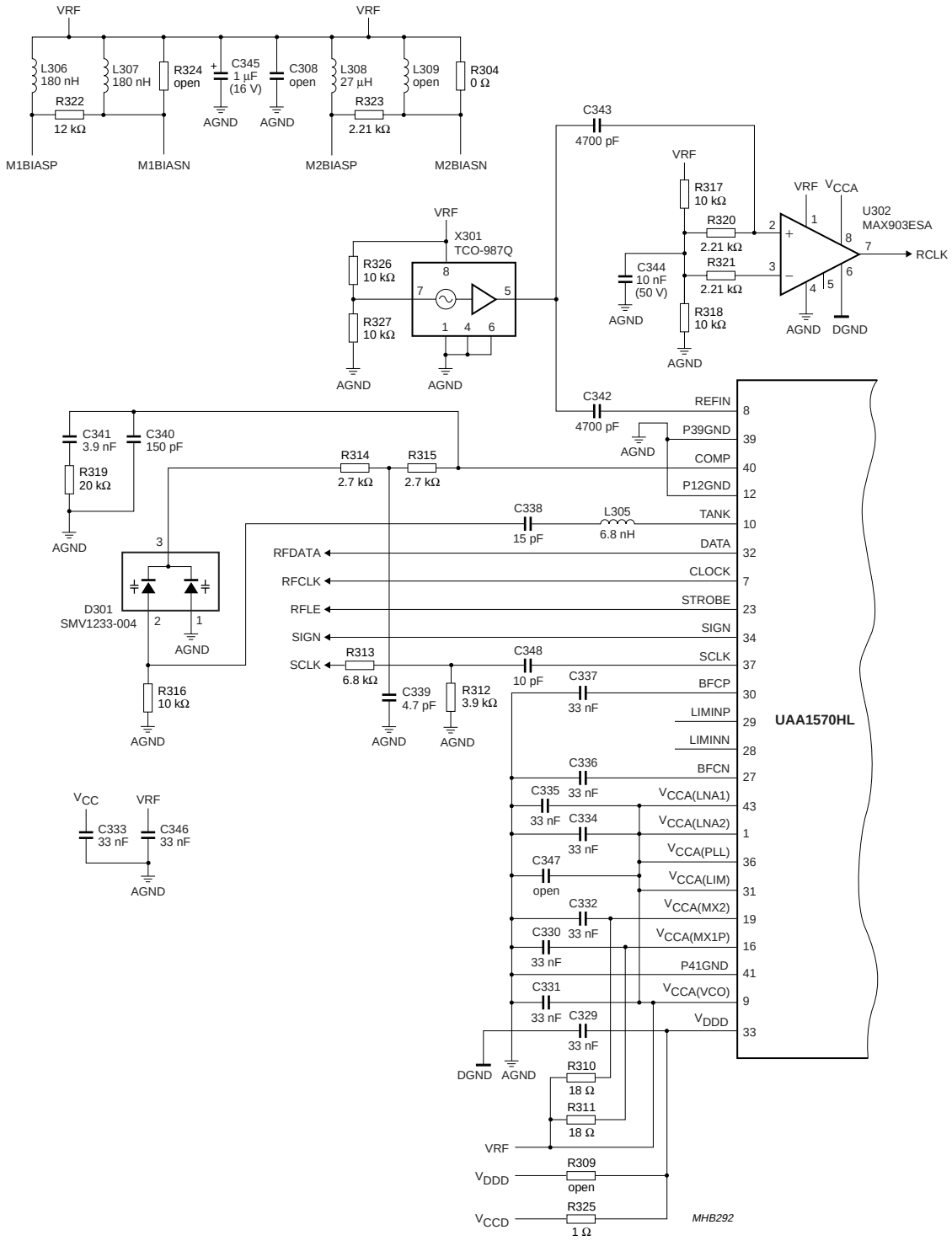


Fig.29 RF front-end circuit (continued in Fig.30).

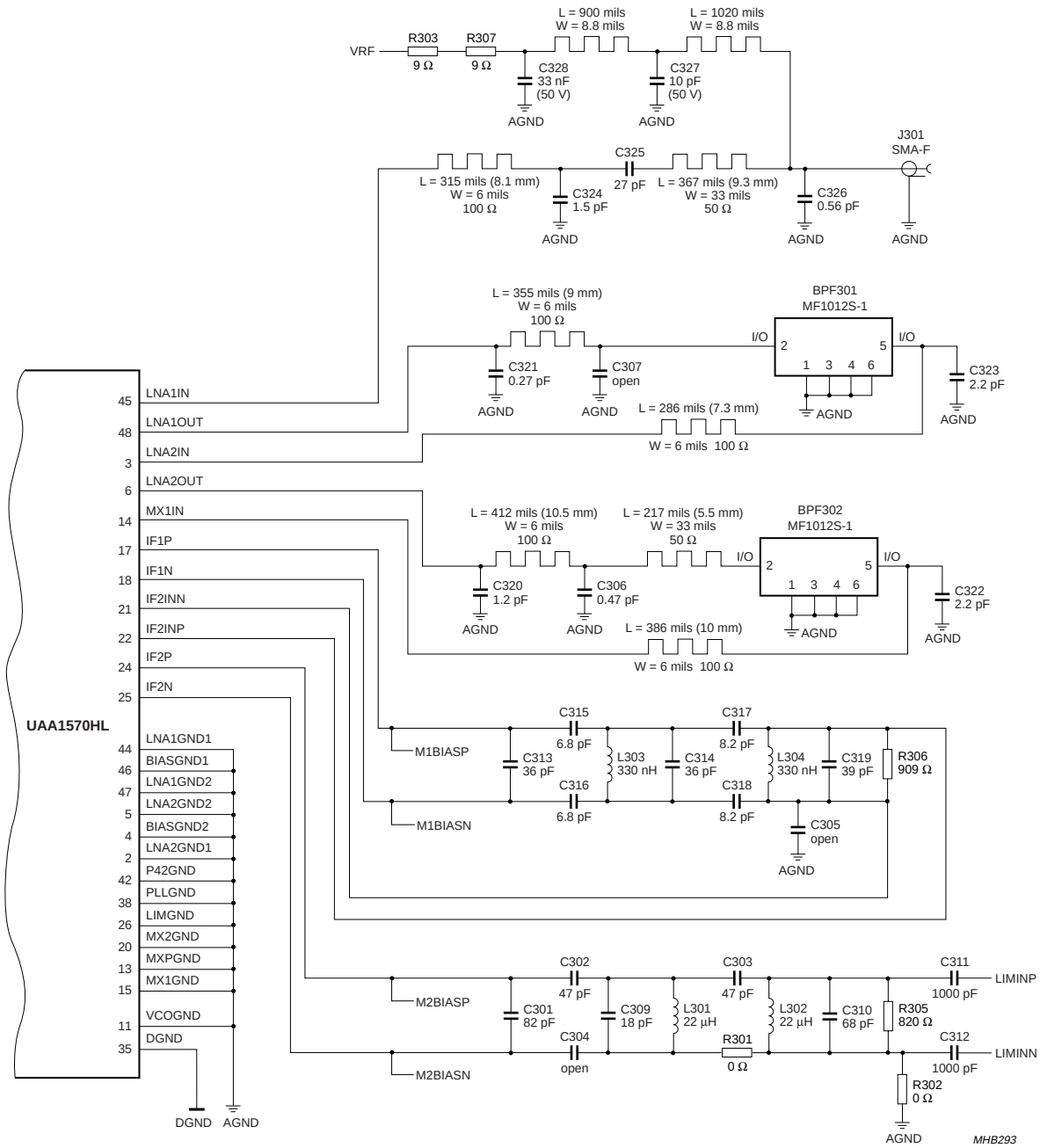


Fig.30 RF front-end circuit (continued from Fig.29).

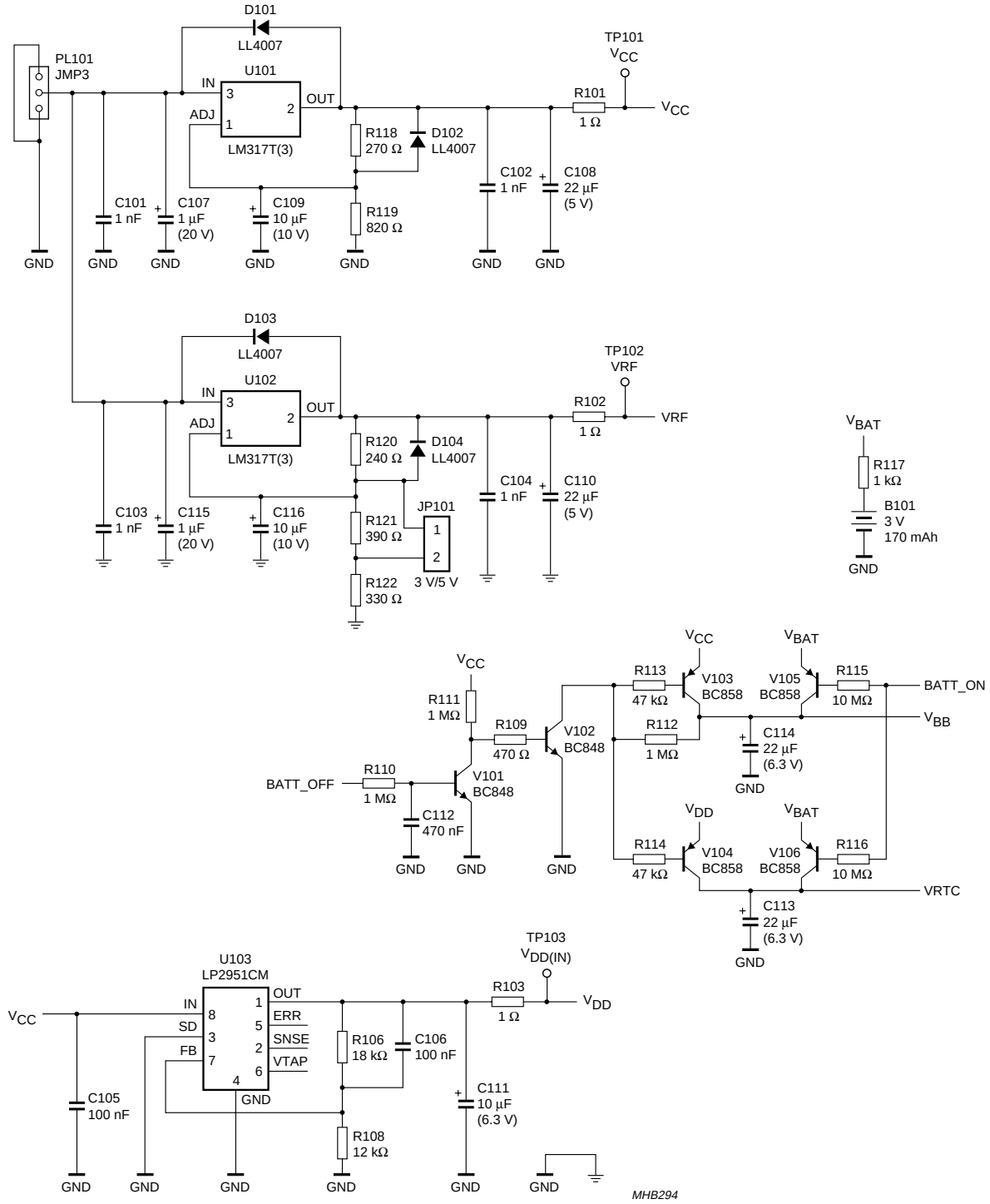


Fig.31 Power supply circuitry.

The GPS system application demonstration board consists of 6 layers with a total final thickness of 1.5 mm. The PCB material is FR4.

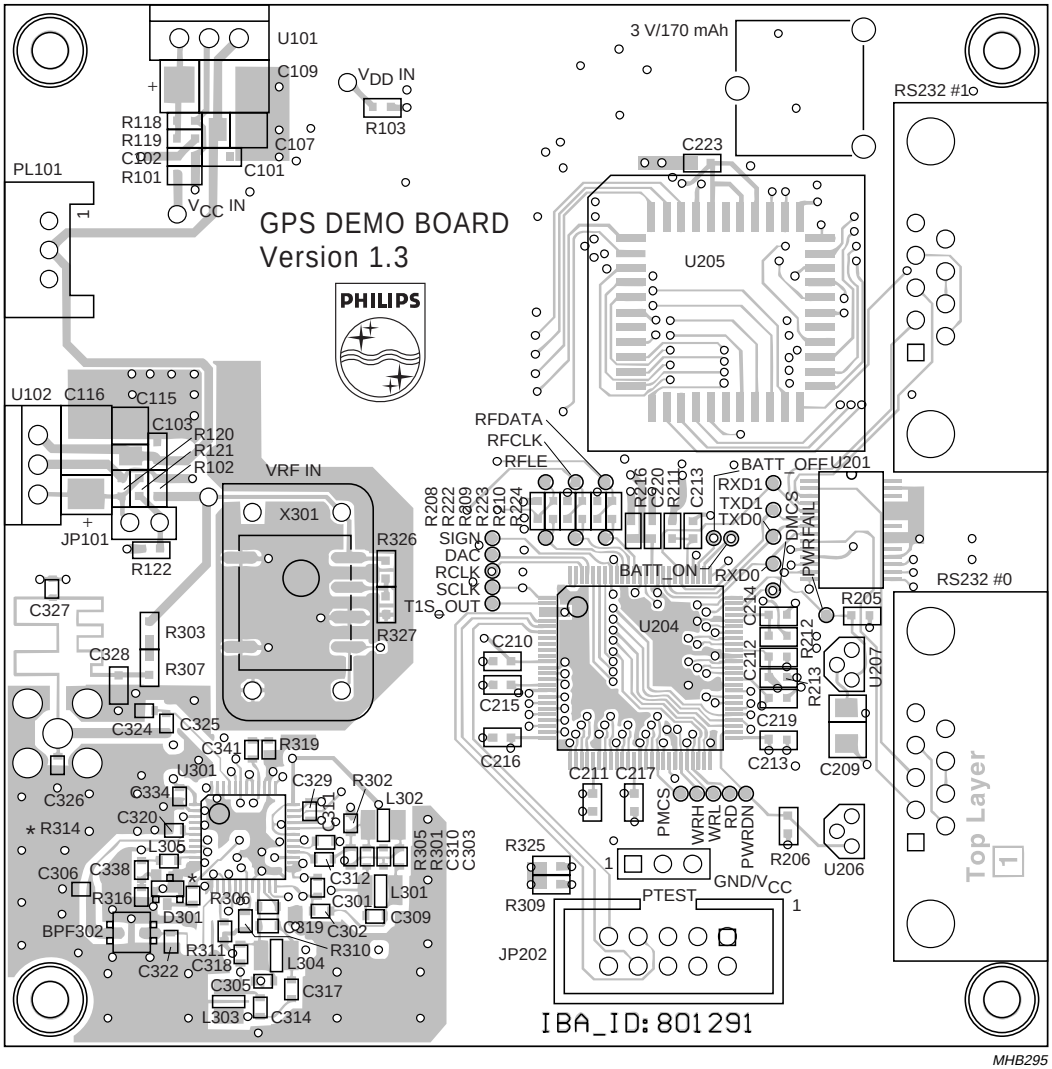


Fig.32 Demonstration board top layer plus components (real size 88.9 mm × 88.9 mm).

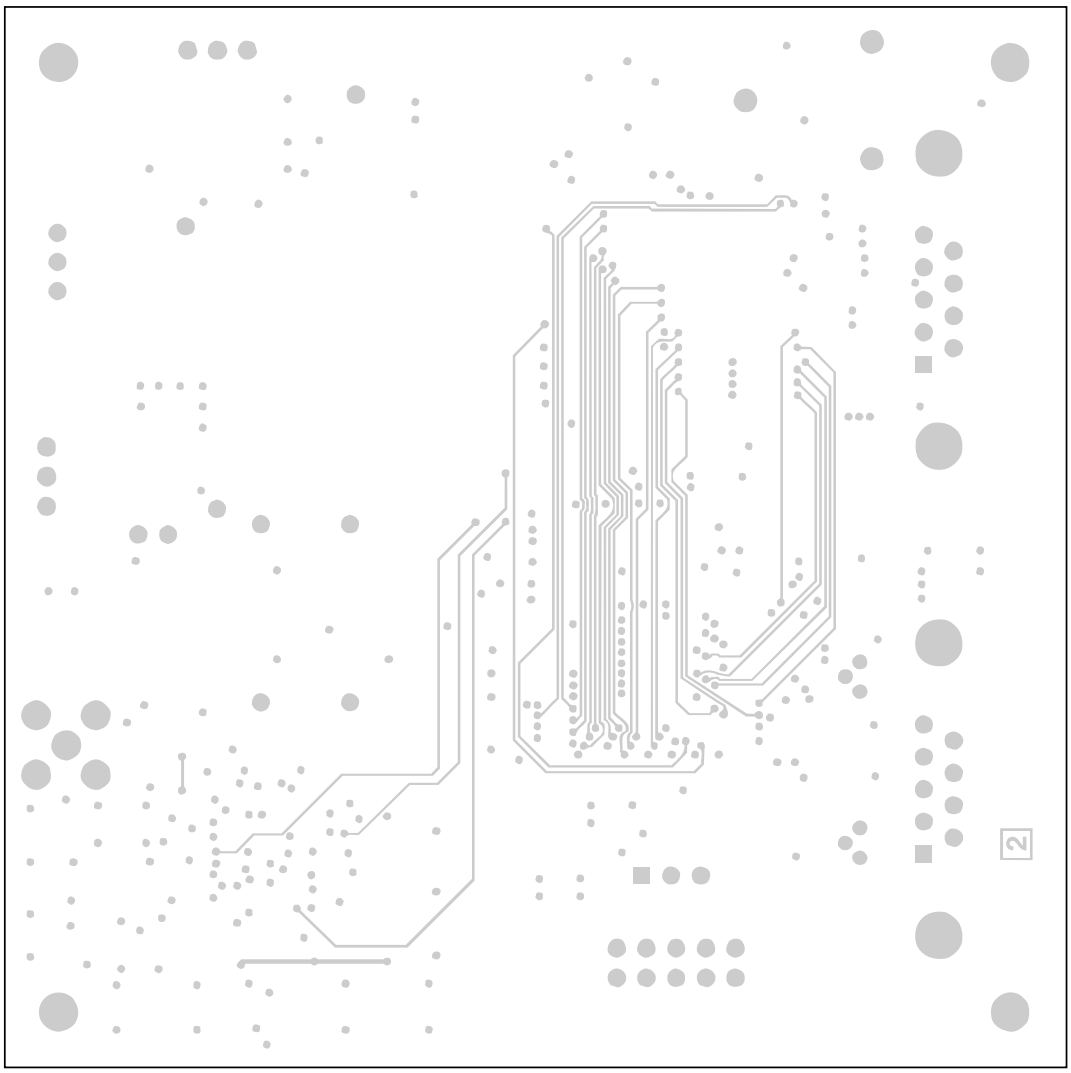


Fig.33 Demonstration board 2nd layer.

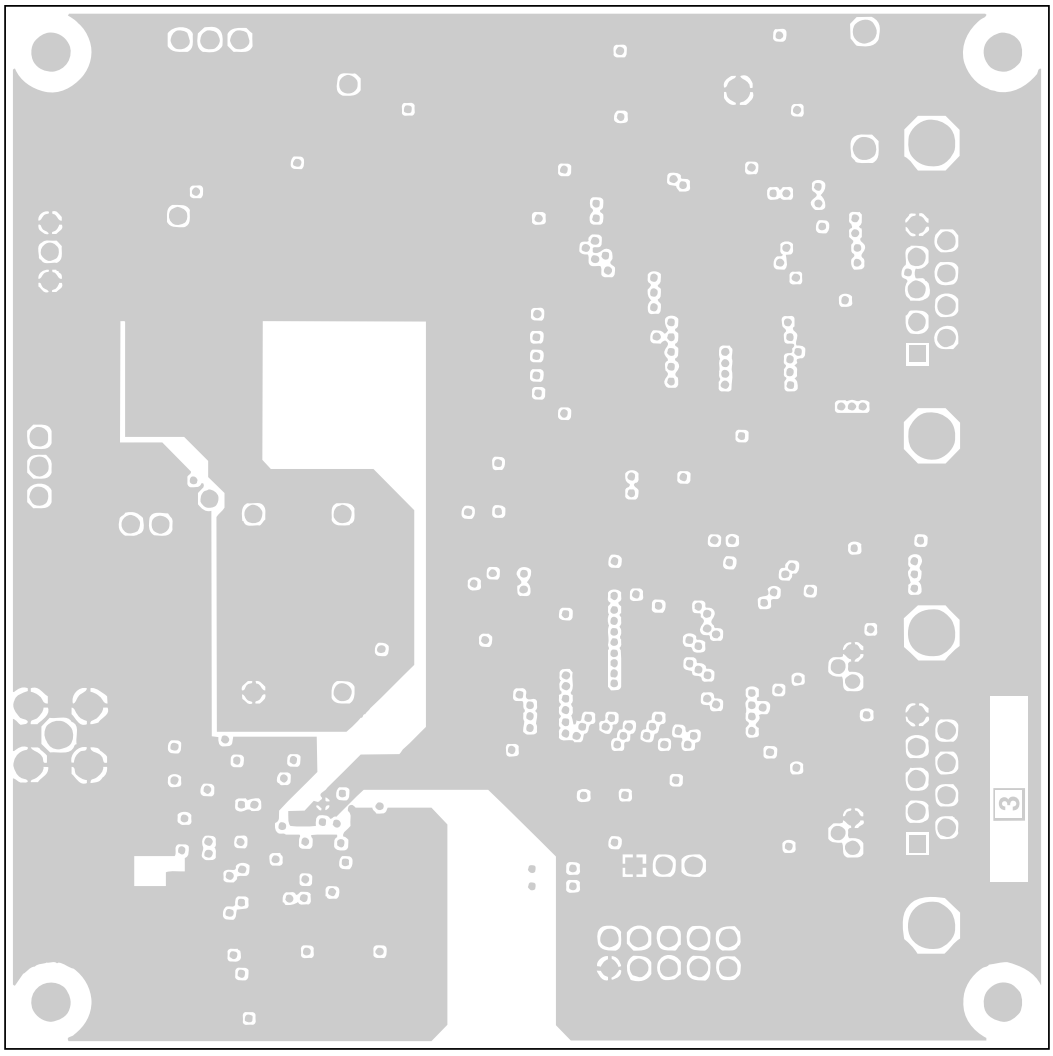


Fig.34 Demonstration board 3rd layer.

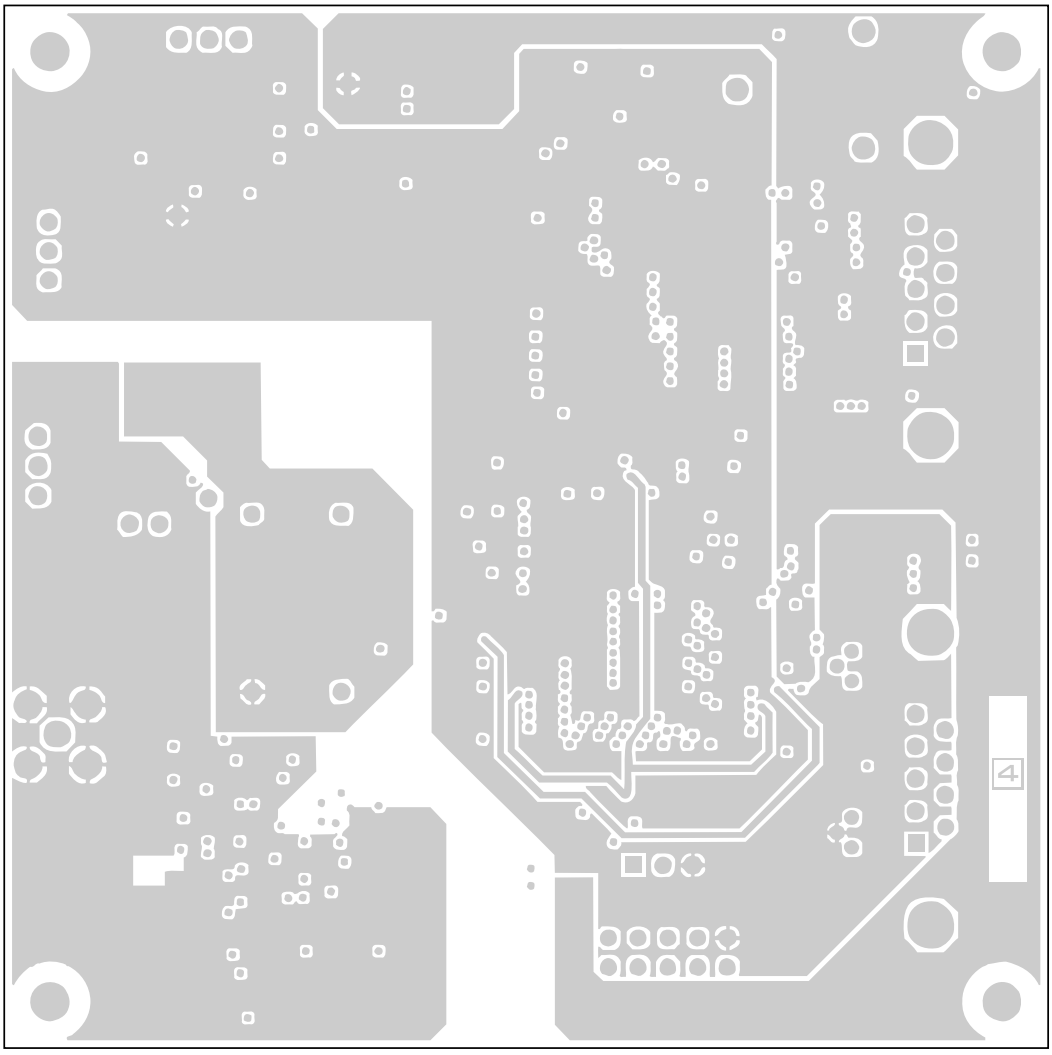
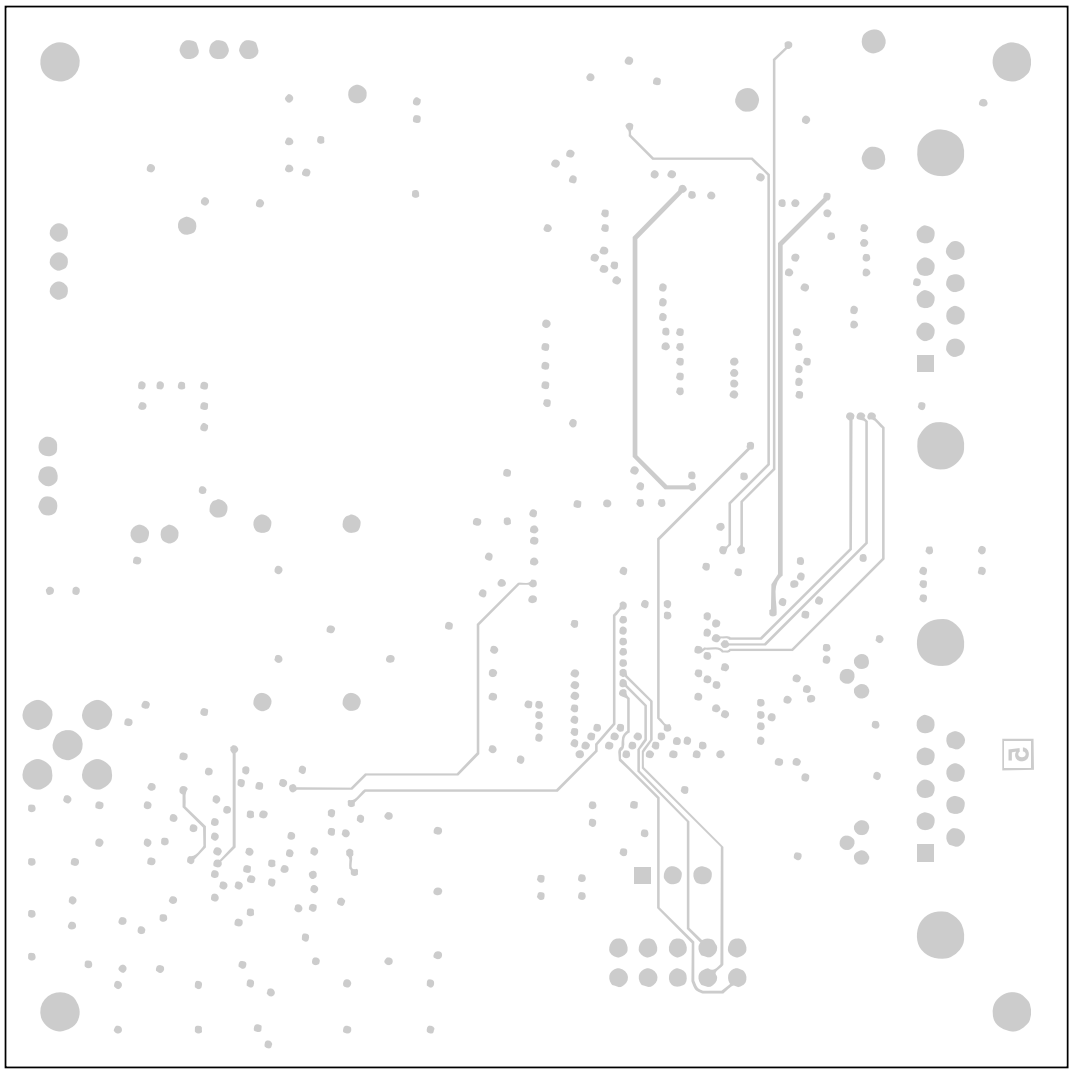


Fig.35 Demonstration board 4th layer.



MHB299

Fig.36 Demonstration board 5th layer.

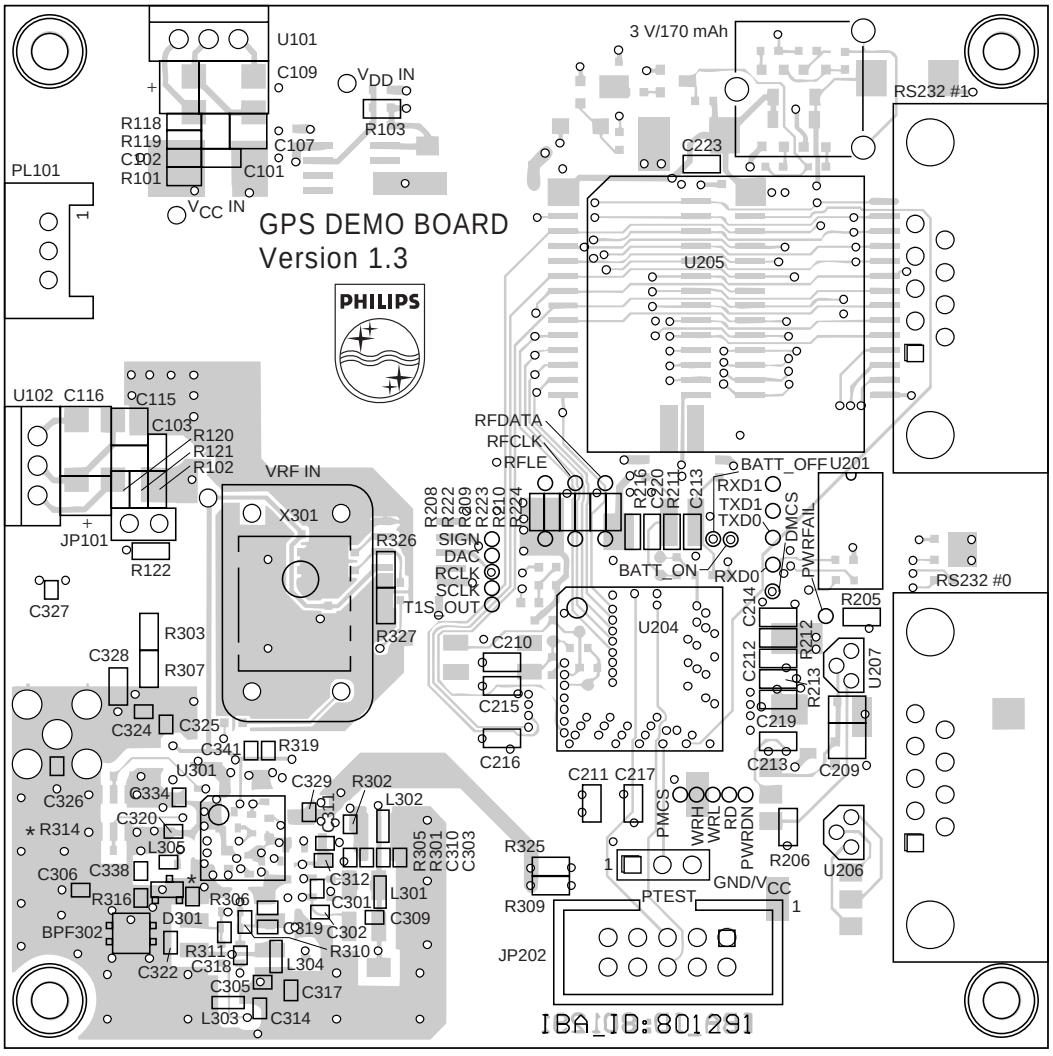


Fig.37 Demonstration board bottom layer plus components.

Table 6 Component list for GPS demonstration board

COMPONENT	TYPE	COMPONENT CHARACTERISTICS		
		VALUE	TOLERANCE	PACKAGE
B101	Lithium battery	3 V/170 mAh	–	CR1/3
C101 to C104, C311 and C312	ceramic capacitor	1 nF/50 V	10%	603
C105, C106, C201 to C204	ceramic capacitor	100 nF/50 V	20%	603
C107 and C115	ceramic capacitor	1 μF/63 V	20%	1210
C108 and C110	tantalum capacitor	22 μF/16 V	20%	–
C109 and C116	tantalum capacitor	10 μF/16 V	20%	–
C111 and C209	tantalum capacitor	10 μF/6.3 V	20%	–
C112	ceramic capacitor	470 nF/63 V	20%	1206
C113 and C114	tantalum capacitor	22 μF/6.3 V	20%	–
C205, C206 and C325	ceramic capacitor	27 pF/50 V	5%	603
C207, C208, C327 and C348	ceramic capacitor	10 pF/50 V	5%	603
C210 to C224, C328 to C337 and C346	ceramic capacitor	33 nF/63 V	10%	603
C225 and C226	tantalum capacitor	47 μF/6.3 V	20%	–
C301	ceramic capacitor	82 pF/50 V	5%	603
C302 and C303	ceramic capacitor	47 pF/50 V	5%	603
C304, C305, C307, C308 and C347	–	not loaded	–	–
C306	ceramic capacitor	0.47 pF/50 V	±0.1 pF	603
C309	ceramic capacitor	18 pF/50 V	5%	603
C310	ceramic capacitor	68 pF/50 V	5%	603
C313 and C314	ceramic capacitor	36 pF/50 V	5%	603
C315 and C316	ceramic capacitor	6.8 pF/50 V	±0.25 pF	603
C317 and C318	ceramic capacitor	8.2 pF/50 V	±0.25 pF	603
C319	ceramic capacitor	39 pF/50 V	5%	603
C320	ceramic capacitor	1.2 pF/50 V	±0.25 pF	603
C321	ceramic capacitor	0.27 pF/50 V	±0.1 pF	603
C322 and C323	ceramic capacitor	2.2 pF/50 V	±0.25 pF	603
C324	ceramic capacitor	1.5 pF/50 V	±0.25 pF	603
C326	ceramic capacitor	0.56 pF/50 V	±0.1 pF	603
C338	ceramic capacitor	15 pF/50 V	5%	603
C339	ceramic capacitor	4.7 pF/50 V	±0.25 pF	603
C340	ceramic capacitor	150 pF/50 V	5%	603
C341	ceramic capacitor	3.9 nF/50 V	10%	603
C342 and C343	ceramic capacitor	4.7 nF/50 V	5%	603
C344	ceramic capacitor	10 nF/50 V	10%	603
C345	tantalum capacitor	1 μF/16 V	20%	–
D101 to D104	LL4007 diode, equivalent to 1N4007	–	–	–
D201	SMD diode BAS 16	–	–	SOT23

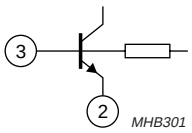
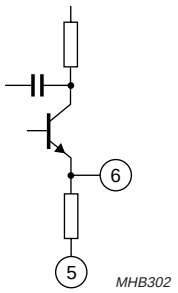
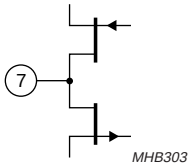
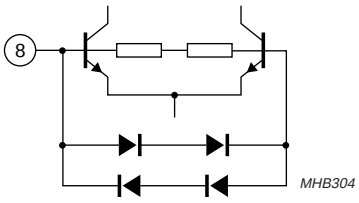
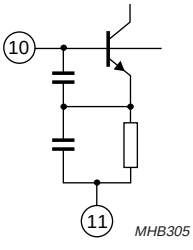
COMPONENT	TYPE	COMPONENT CHARACTERISTICS		
		VALUE	TOLERANCE	PACKAGE
D301	Alpha SMV1204-133 varactor	–	–	SOT23
L301 and L302	SMD inductor	22 μH	5%	1008
L303 and L304	SMD inductor	330 nH	5%	1008
L305	SMD inductor	6.8 nH	±5%	603
L306 and L307	SMD inductor	180 nH	±5%	1008
L308	SMD inductor	27 μH	5%	1008
L309	–	not loaded	–	–
R101, R102, R103, R211, R212, R213, R216 and R325	SMD resistor	1 Ω	5%	603
R106	SMD resistor	18 kΩ	5%	603
R108 and R322	SMD resistor	12 kΩ	1%	603
R109 and R207	SMD resistor	470 Ω	1%	603
R110, R111, R112 and R204	SMD resistor	1 MΩ	1%	603
R113 and R114	SMD resistor	47 kΩ	1%	603
R115, R116 and R202	SMD resistor	10 MΩ	1%	603
R117	SMD resistor	1 kΩ	1%	603
R118	SMD resistor	270 Ω	1%	603
R119 and R305	SMD resistor	820 Ω	1%	603
R120	SMD resistor	240 Ω	1%	603
R121	SMD resistor	390 Ω	1%	603
R122	SMD resistor	330 Ω	1%	603
R201, R301, R302 and R304	SMD resistor	0 Ω	–	603
R203	SMD resistor	180 Ω	5%	603
R205, R206, R316, R317, R318, R326 and R327	SMD resistor	10 kΩ	1%	603
R208, R209, R210, R309 and R324	–	not loaded	–	–
R222 to R224	SMD resistor	220 Ω	5%	603
R303 and R307	SMD resistor	9.1 Ω	5%	603
R306	SMD resistor	910 Ω	1%	603
R310 and R311	SMD resistor	18 Ω	1%	603
R312	SMD resistor	3.9 kΩ	1%	603
R313	SMD resistor	6.8 kΩ	1%	603
R314 and R315	SMD resistor	2.7 kΩ	1%	603
R319	SMD resistor	20 kΩ	5%	603
R320, R321 and R323	SMD resistor	2.2 kΩ	1%	603
U101 and U102[(1)]	LM317T voltage regulator	–	–	TO220
U103	LP2951CM voltage regulator (National)	–	–	SO8

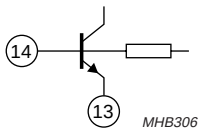
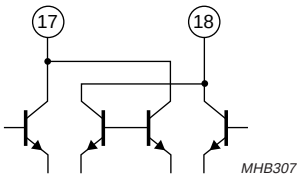
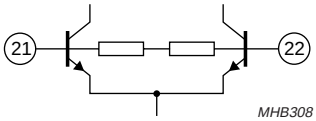
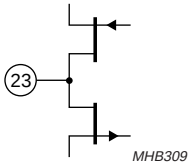
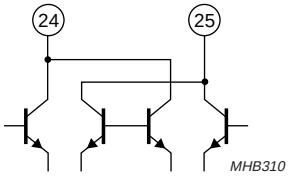
COMPONENT	TYPE	COMPONENT CHARACTERISTICS		
		VALUE	TOLERANCE	PACKAGE
U201	MAX213EAIRS2312 transceiver (Maxim)	–	–	SSOP28
U202 and U203	SRAM M5M5256BFP-70LL 32k × 8 (Mitsubishi)	–	–	SO28
U205	27C202 EPROM	–	–	PLCC44
U206	ZM33064 power monitor	–	–	–
U207	ZM33164 power monitor	–	–	–
U302	MAX903ESA comparator (Maxim)	–	–	SO8
V101 and V102	BC848 or BC847C NPN transistor	–	–	SOT23
V103 to V106	BC858 PNP transistor	–	–	SOT23
X301	TCXO TCO-987Q	–	–	–
Y201	30 MHz crystal, 16 pF load capacitance	–	–	–
Y202	SMD crystal	32.768 kHz	±30 ppm	–
BPF301 and BPF302	MF1012S-1 saw filter	–	–	–

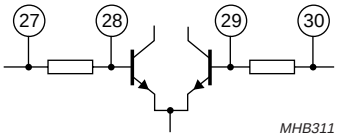
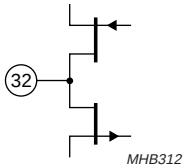
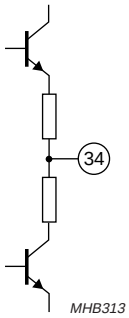
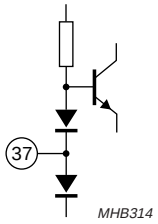
Note

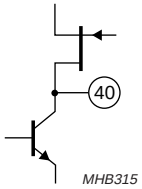
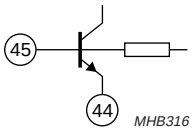
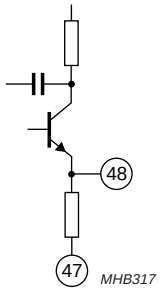
1. With heat sink depending on input voltage.

15 INTERNAL CIRCUITRY

PIN	SYMBOL	PIN VOLTAGE TYPICAL VALUES (V)		EQUIVALENT CIRCUIT WITHOUT ESD PROTECTION CIRCUITS
		V_{CC} = 2.7 V	V_{CC} = 5 V	
1	$V_{CCA(LNA2)}$	2.7	5	
2	LNA2GND1	0	0	
3	LNA2IN	0.815	0.807	
4	BIASGND2	0	0	
5	LNA2GND2	0	0	
6	LNA2OUT	1.48	3.629	
7	CLOCK	CMOS level	CMOS level	
8	REFIN	1.69	3.99	
9	$V_{CCA(VCO)}$	2.7	5	
10	TANK	1.92	1.92	

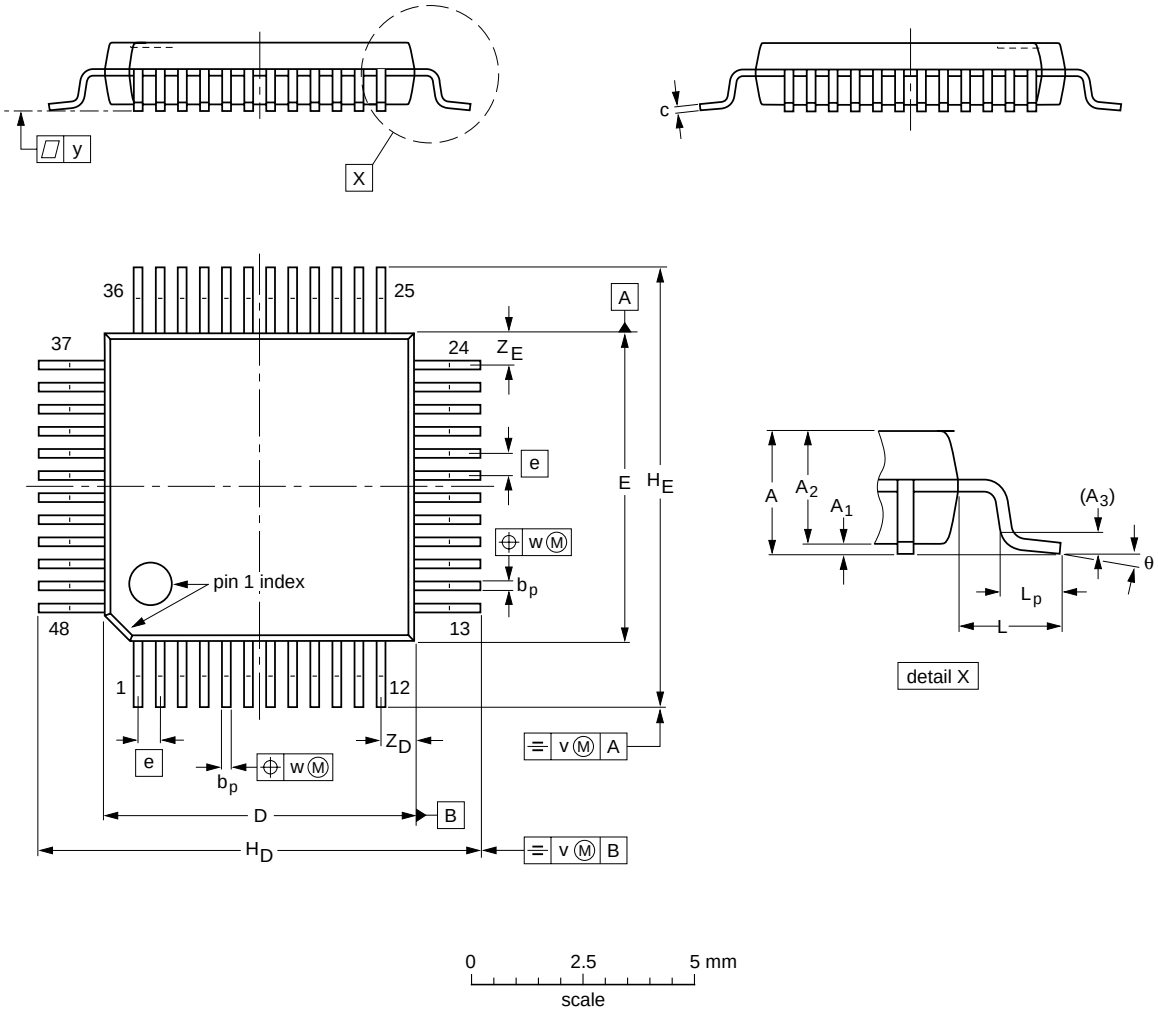
PIN	SYMBOL	PIN VOLTAGE TYPICAL VALUES (V)		EQUIVALENT CIRCUIT WITHOUT ESD PROTECTION CIRCUITS
		V_{CC} = 2.7 V	V_{CC} = 5 V	
11	VCOGND	0	0	
12	P12GND	0	0	
13	MXPGND	0	0	
14	MX1IN	0.82	0.81	
15	MX1GND	0	0	
16	$V_{CCA(MX1P)}$	2.7	5	
17	IF1P	2.7	5	
18	IF1N	2.7	5	
19	$V_{CCA(MX2)}$	2.7	5	
20	MX2GND	0	0	
21	IF2INN	0.983	0.98	
22	IF2INP	0.983	0.98	
23	STROBE	CMOS level	CMOS level	
24	IF2P	2.7	5	
25	IF2N	2.7	5	
26	LIMGND	0	0	

PIN	SYMBOL	PIN VOLTAGE TYPICAL VALUES (V)		EQUIVALENT CIRCUIT WITHOUT ESD PROTECTION CIRCUITS
		V_{CC} = 2.7 V	V_{CC} = 5 V	
27	BFCN	1.696	3.999	
28	LIMINN	1.696	3.999	
29	LIMINP	1.696	3.999	
30	BFCP	1.696	3.999	
31	$V_{CCA(LIM)}$	2.7	5	
32	DATA	CMOS level	CMOS level	
33	V_{DDD}	2.7 (independent of V_{CC} level)	5 (independent of V_{CC} level)	
34	SIGN	TTL output	TTL output	
35	DGND	0	0	
36	$V_{CCA(PLL)}$	2.7	5	
37	SCLK	1.34	2.5	
38	PLLGND	0	0	
39	P39GND	0	0	

PIN	SYMBOL	PIN VOLTAGE TYPICAL VALUES (V)		EQUIVALENT CIRCUIT WITHOUT ESD PROTECTION CIRCUITS
		V_{CC} = 2.7 V	V_{CC} = 5 V	
40	COMP	depends on VCO application	depends on VCO application	
41	P41GND	0	0	
42	P42GND	0	0	
43	$V_{CCA(LNA1)}$	2.7	5	
44	LNA1GND1	0	0	
45	LNA1IN	0.815	0.807	
46	BIASGND1	0	0	
47	LNA1GND2	0	0	
48	LNA1OUT	1.48	3.629	

16 PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

17 SOLDERING

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
HLQFP, HSQFP, HSOP, SMS	not suitable[2]	suitable
PLCC[3], SO	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SQFP	not suitable	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

18 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

19 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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