DATA SHEET

UAA3540TS
DECT receiver

Product specification
File under Integrated Circuits, IC17

2000 Feb 15

Philips
Semiconductors

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FEATURES

- Single-chip RF plus IF
- Integrated channel filter
- Low component count
- No production trimming
- High dynamic range
- Low power
- 3.2 V operation
- Built-in power-down mode.

GENERAL DESCRIPTION

The UAA3540TS is a low-power, highly integrated circuit, for Digital Enhanced Cordless Telecommunication (DECT) applications.

It features a fully integrated channel selection filter, an analog Received Signal Strength Indicator (RSSI) and a switched demodulator output to interface to Philips Semiconductors ABC baseband chip. The circuit can be fully powered down during the idle locked state.

QUICK REFERENCE DATA

V_{CC} = 3.2 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	over T_{amb}	3.0	3.2	3.6	V
I_{CC}	supply current		–	34	45	mA
$I_{CC(pd)}$	power-down mode supply current		–	10	50	µA
T_{amb}	ambient temperature		–10	–	+60	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3540TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

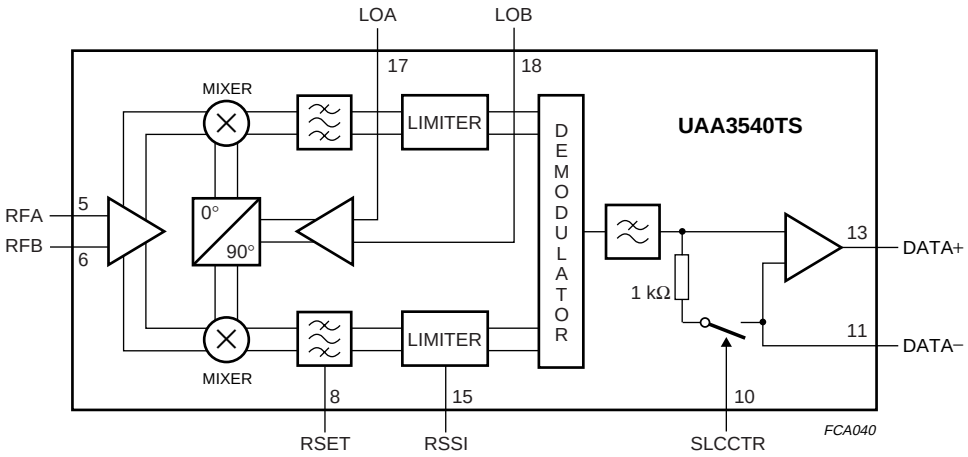


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$GND_{(LO)}$	1	local oscillator ground
PD	2	power-down control input (logic 1 disables the chip)
$V_{CC(RF)}$	3	RF positive supply voltage
$GND_{(RF)}$	4	RF ground
RFA	5	RF balanced input A
RFB	6	RF balanced input B
$GND_{(IF)}$	7	IF ground
RSET	8	set filter (connect to external resistor)
TEST1	9	test 1 (connect to GND)
SLCCTR	10	slicer threshold switch control input (logic 1 closes the switch)
DATA–	11	switched demodulator output
TEST2	12	test 2 (connect to GND)
DATA+	13	demodulator digital signal output
TEST3	14	test 3 (connect to V_{CC})
RSSI	15	received signal strength intensity voltage output
$V_{CC(IF)}$	16	IF positive supply
LOA	17	local oscillator balanced input A
LOB	18	local oscillator balanced input B
$V_{CC(LO)}$	19	local oscillator positive supply
TEST4	20	test 4 (connect to GND)

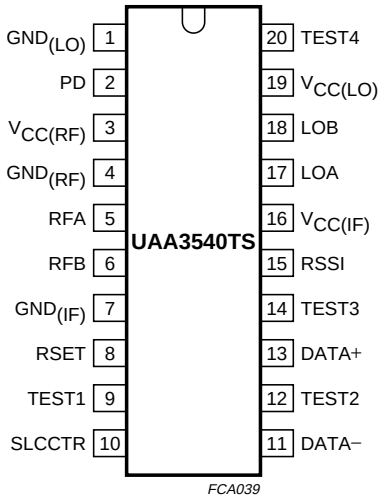


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The UAA3540TS is a fully integrated RF plus IF strip and demodulator for DECT applications. It provides all the required channel filtering over the DECT band and generates analog RSSI and a data output for the baseband chip. Very few off-chip components are required and should not require trimming in normal applications. The chip is designed to operate from a power supply voltage which can fall to 3.0 V, and features full power-down capabilities.

The inputs are an RF antenna signal and a Local Oscillator (LO) signal. The RF antenna signal is from a band filter or antenna switch. The higher frequency LO signal is from an external Voltage Controlled Oscillator (VCO).

The outputs are an RSSI voltage, representing the instantaneous signal strength, and DATA– and DATA+ which are two high-level demodulator output signals. DATA– is switched by SLCCTR to generate a threshold voltage for the internal slicer, and DATA+ is the comparator digital output.

Filter

The integrated filter provides all the channel selectivity required for the DECT receiver. An external resistor of 18 kΩ must be connected to RSET (pin 8).

Limiter and RSSI

The main purpose of the limiter circuit is to reduce the dynamic range of the signals presented to the demodulator; these have a dynamic range greater than 60 dB.

The limiter also provides the RSSI output voltage. The RSSI output has very little filtering applied, and it is assumed that external circuits will be used to provide the time constant and peak holding required by the DECT specification.

Demodulator

The demodulator produces an output voltage directly proportional to the instantaneous frequency of the received signal. The output stage of the demodulator contains a data filter to remove high frequencies from the signal, prior to data slicing.

The demodulator provides a continuous output timing signal that is applied to an internal data slicer. The same signal is also switched to generate the threshold voltage of the slicer during the initial DECT bit sequence.

Power-down

The power-down control input (pin 2) allows the current consumption of the chip to be reduced to a very low level when it is connected to V_{CC}. In this state, some voltages in the chip become indeterminate requiring time for the receiver to stabilize after power-up.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+3.6	V
$V_{i(PD)}$; $V_{i(SLCCTR)}$	input voltage on pins PD and SLCCTR	–0.3	+3.6	V
$P_{i(max)}$	maximum input power	–	15	dBm
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
$P_{(max)}$	maximum power dissipation in quiet air	–	180	mW
T_{stg}	storage temperature	–55	+125	°C

HANDLING

All pins withstand 1500 V ESD test in accordance with *"EIA/JESD22-A114 Class1 (Feb. 96)"*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	152	K/W

DC CHARACTERISTICS

V_{CC} = 3.2 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (Pins $V_{CC(LO)}$, $V_{CC(RF)}$ and $V_{CC(IF)}$)						
V_{CC}	supply voltage	$T_{amb} \geq 25$ °C	3.0	3.2	3.6	V
I_{CC}	supply current		–	34	45	mA
$I_{CC(pd)}$	power-down mode supply current		–	10	50	µA
Interface logic input signal levels (Pins PD and SLCCTR)						
V_{IH}	HIGH-level input voltage		1.4	–	V_{CC}	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.4	V
$I_{i(bias)}$	input bias current	logic 1 or 0	–5	–	+5	µA

AC CHARACTERISTICS

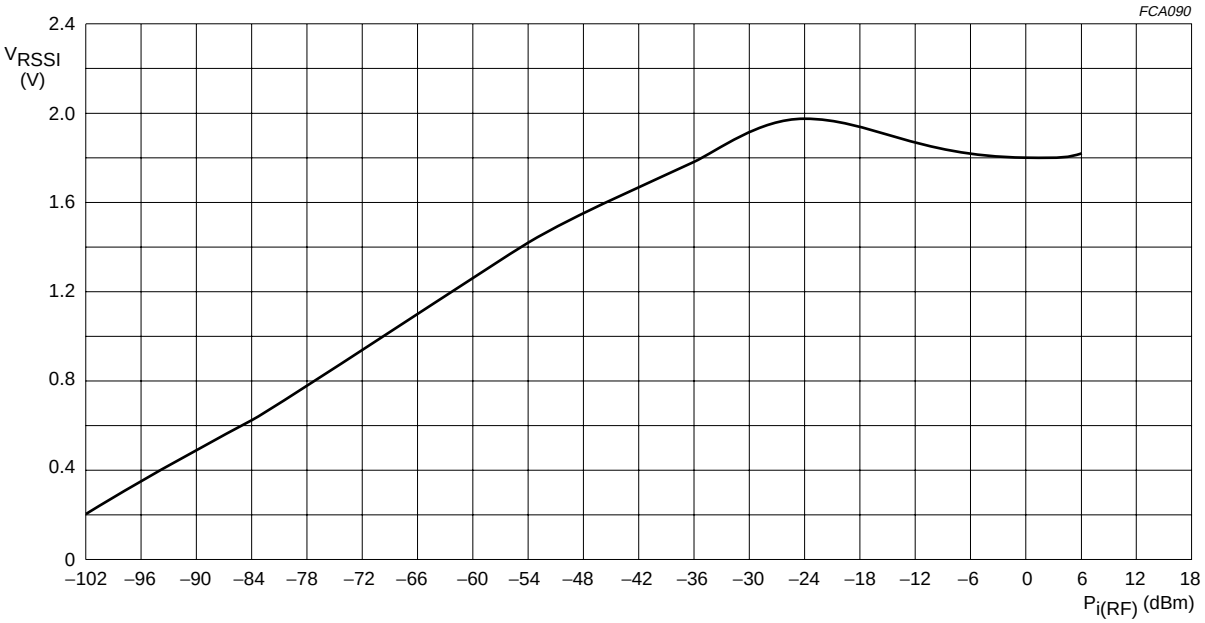
V_{CC} = 3.2 V; T_{amb} = 25 °C; modulation deviation Δf = 288 kHz; measured on Philips Semiconductors characterization board at the RF balun input; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin RSSI						
V_{RSSI}	RSSI output voltage monotonic over range –96 to –36 dBm	with –36 dBm at RF input	–	1.7	2	V
		with –96 dBm at RF input	–	0.3	–	V
t_{wake}	period between power-up signal and valid RSSI output (wake-up time)	no external capacitor on the RSSI output	–	25	40	µs
Systems						
$S_{B.3}$	sensitivity of RF input	BER ≤ 10^{-3}; note 1	–	–95	–93	dBm
$S_{B.5}$	sensitivity of RF input	BER ≤ 10^{-5}; note 1	–	–92	–76	dBm
IM_3	intermodulation rejection	unwanted interferers level in channels N + 2 and N + 4 referred to wanted at –83 dBm in channel 5 for BER < 10^{-3}; note 1	33	40	–	dBc
R_{co}	co-channel rejection	co-channel interferer level referred to wanted at –76 dBm both in channel 5 for BER < 10^{-3}; note 1	–10	–8	–	dBc
$R_{j(N+1)}$	adjacent channel rejection	adjacent channel interferer level referred to wanted at –76 dBm in channel 5 for BER < 10^{-3}; note 1	13	19	–	dBc
$R_{j(N+2)}$	bi-adjacent channel rejection	bi-adjacent channel interferer level referred to wanted at –76 dBm in channel 5 for BER < 10^{-3}; note 1	34	40	–	dBc
$R_{j(N+\geq 3)}$	≥3 channels rejection	N ≥ 3 adjacent channel interferer level referred to wanted at –76 dBm in channel 5 for BER < 10^{-3}; note 1	40	44	–	dBc
$BI_{\Delta f > 6\ MHz}$	rejection of a blocking signal in the range $\lvert f - f_{cl} \rvert$ > 6 MHz	unwanted CW level referred to wanted at –83 dBm in channel 5 for BER < 10^{-3}; note 1	37	55	–	dBc
$BI_{near}1$	rejection of a blocking signal in the ranges: $f_{(RF)(min)} - 100\ MHz < f < f_{(RF)(min)} - 5\ MHz$; $f_{(RF)(max)} + 5\ MHz < f < f_{(RF)(max)} + 100\ MHz$		52	58	–	dBc
$BI_{near}2$	rejection of a blocking signal in the ranges: $f_{(RF)(min)} - 300\ MHz < f < f_{(RF)(min)} - 100\ MHz$; $f_{(RF)(max)} + 100\ MHz < f < f_{(RF)(max)} + 300\ MHz$		52	58	–	dBc

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BI_{farlow}	rejection of a blocking signal in the range: 25 MHz < f < $f_{(RF)(min)}$ − 300 MHz	unwanted CW level referred to wanted at −83 dBm in channel 5 for BER < 10^{-3}; note 1	37	58	–	dBc
$BI_{farhigh}$	rejection of a blocking signal in the range: $f_{(RF)(max)}$ + 300 MHz < f < 4.32 GHz	unwanted CW level referred to wanted at −83 dBm in channel 5 for BER < 10^{-3}; note 1; except 3 occurrences at F_{G1}, F_{G2} and F_{G3} as defined in TBR6	47	58	–	dBc
BF_{G1}	rejection of a blocking signal in occurrence around: F_{G1} = 2835.648 MHz	unwanted CW level referred to wanted at −83 dBm in channel 5 for BER < 10^{-3}; note 1	37	45	–	dBc
BF_{G2}	rejection of a blocking signal in occurrence around: F_{G1} = 3150.144 MHz		37	49	–	dBc
BF_{G3}	rejection of a blocking signal in occurrence around: F_{G1} = 3779.136 MHz		20	30	–	dBc
Receive section						
$R_{i(RF)}$	RF input resistance (real part of the parallel input impedance)	balanced; at 1890 MHz	–	70	–	Ω
$C_{i(RF)}$	RF input capacitance (imaginary part of the parallel input impedance)		–	0.8	–	pF
$f_{(RF)(max)}$	maximum RF input frequency		–	–	1930	MHz
$f_{(RF)(min)}$	minimum RF input frequency		1880	–	–	MHz
$RL_{i(RF)(m)}$	return loss on matched RF input	balanced; note 1	11	15	–	dB
Local oscillator section						
$R_{i(lo)}$	LO input resistance (real part of the parallel input impedance)	balanced; at 1890 MHz	–	140	–	Ω
$C_{i(lo)}$	LO input capacitance (imaginary part of the parallel input impedance)		–	0.3	–	pF
$RL_{i(lo)}$	return loss on matched LO input	balanced; note 2	9	12	–	dB
$P_{i(lo)}$	LO input power level		–	−15	–	dBm
Demodulator section						
G_{dem}	demodulator gain		–	1.5	–	V/MHz

Notes

1. Measured on the Philips Semiconductors characterisation board at the RF balun input.
2. Measured on the Philips Semiconductors characterisation board at the LO balun input.



V_{CC} = 3.2 V; T_{amb} = 25°C.

Fig.3 RSSI output voltage as a function of RF input power.

APPLICATION INFORMATION

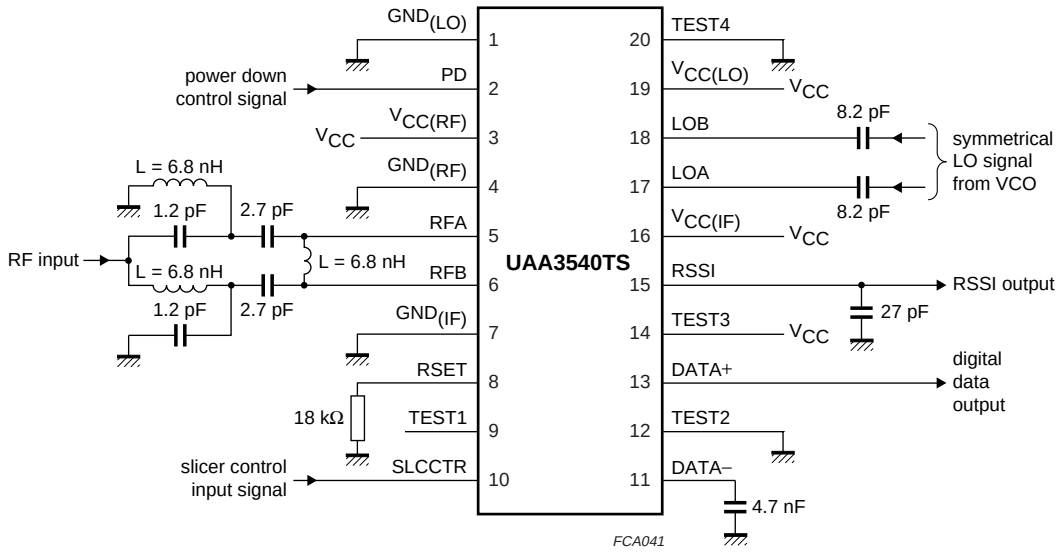
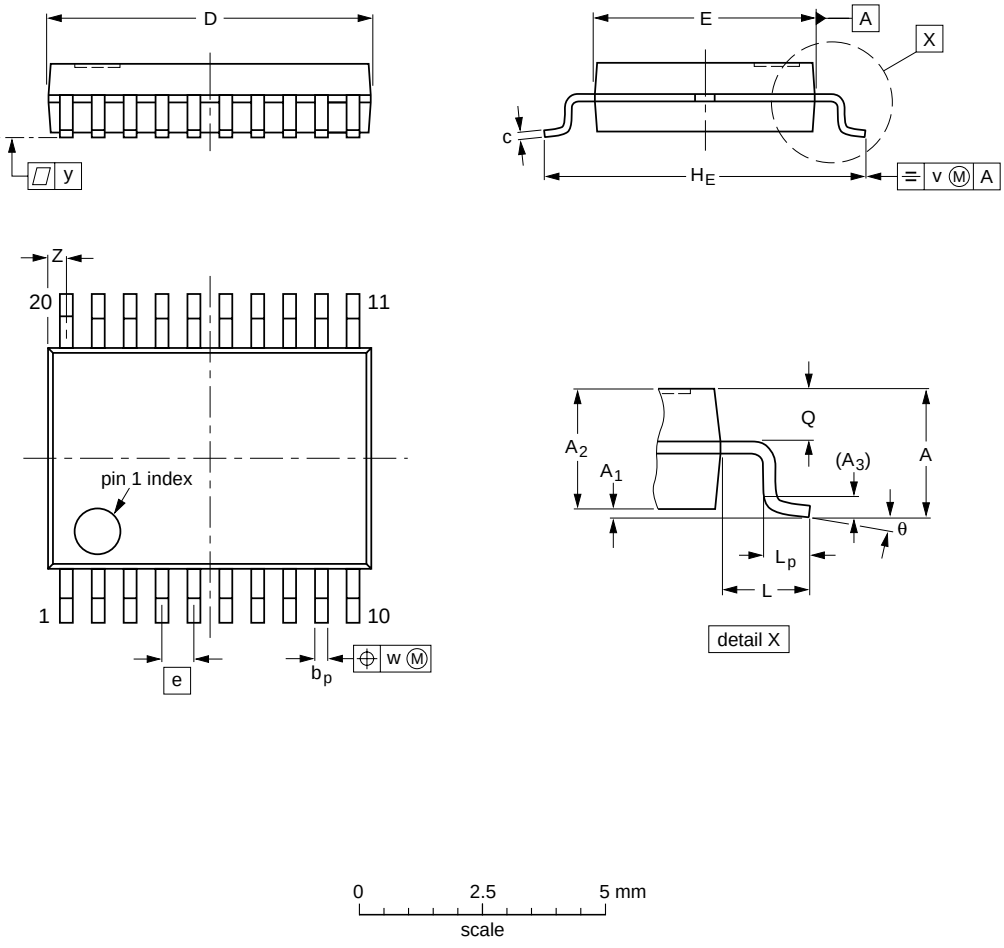


Fig.4 Application diagram.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1		MO-152					~~95-02-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands 403506/02/pp16 Date of release: 2000 Feb 15 Document order number: 9397 750 06422

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