DATA SHEET

UAA3592
Wideband code division multiple access frequency division duplex power amplifier

Objective specification

2002 Jul 02

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Wideband code division multiple access frequency division duplex power amplifier

UAA3592

FEATURES

- 3.6 V nominal supply voltage
- 24 dBm average output power
- 0 dBm input power
- Wide operating temperature range from −30 to +70 °C
- HVQFN16 package.

GENERAL DESCRIPTION

The UAA3592 is a Wideband Code Division Multiple Access (WCDMA) silicon bipolar transistor Monolithic Microwave Integrated Circuit (MMIC) Power Amplifier (PA). The circuit is specially designed to operate at a nominal 3.6 V battery supply voltage. It includes a current saving architecture at low output power levels.

APPLICATIONS

- WCDMA-FDD applications.

QUICK REFERENCE DATA

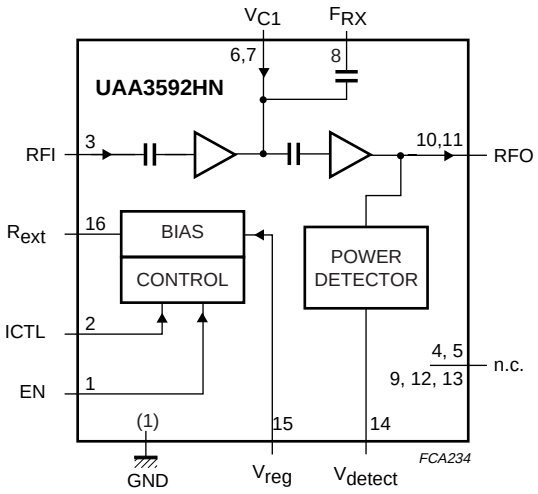
T_{amb} = 25 °C; V_{C1} = 3.6 V; V_{reg} = 2.7 V.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{C1}	positive supply voltage	–	3.6	–	V
$P_{o(max)}$	maximum output power	–	24.5	–	dBm
η	efficiency at maximum power	–	35	–	%
T_{amb}	ambient temperature	−30	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3592HN	HVQFN16	plastic, heatsink very thin quad flat package; no leads; 16 terminals; body $4 \times 4 \times 0.85$ mm	SOT629-1

BLOCK DIAGRAM



Die pad must be connected to ground.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
EN	1	enable input
ICTL	2	current control input
RFI	3	power amplifier input
n.c.	4	not connected
n.c.	5	not connected
V_{C1}	6	supply voltage for the first stage collector
V_{C1}	7	supply voltage for the first stage collector
F_{RX}	8	RX filter
n.c.	9	not connected
RFO	10	power amplifier output
RFO	11	power amplifier output
n.c.	12	not connected
n.c.	13	not connected
V_{detect}	14	power detection
V_{reg}	15	regulated supply voltage
R_{ext}	16	connection to external resistor
	die pad	ground

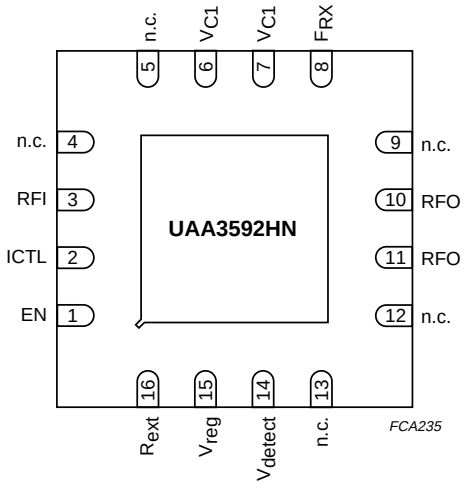


Fig.2 Pin configuration (bottom view).

FUNCTIONAL DESCRIPTION

Operating conditions

The UAA3592 is designed to meet the *"Third Generation Partnership Project (3GPP) specification"* for the Universal Mobile Telecommunication System (UMTS) standard.

Power amplifier

The device is intended for WCDMA power amplification. The control signals select the bias current as given in Table 1.

Table 1 Current control

EN	ICTL	DESCRIPTION
0	0	off
0	1	off
1	0	nominal bias current
1	1	bias current is reduced by 50% on the second stage

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{C1}	supply voltage for the first stage collector		–	5.5	V
V_{reg}	regulated voltage		–	3.3	V
$T_{j(max)}$	maximum operating junction temperature		–	150	°C
P_{tot}	total power dissipation	note 1	–	tbf	mW
P_i	input power		–	10	dBm
T_{stg}	storage temperature		–55	+150	°C

Note

1. On Philips evaluation board.

HANDLING

Do not operate or store near strong electrostatic fields.

Mets class 1 ESD test requirements (Human Body Model - HBM), in accordance with *"EIA/JESD22-A114-A (October 1997)"* and class A ESD test requirements (Machine Model - MM), in accordance with *"EIA/JESD22-A115.-A (October 1997)"*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	tbf	K/W

Note

1. On Philips evaluation board.

DC CHARACTERISTICS

V_{C1} = 3.6 V; V_{reg} = 2.7 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{C1}	supply voltage for the first stage collector		3.25	3.6	4.5	V
V_{reg}	regulated supply voltage		2.6	2.7	3	V
$I_{C1(q)}$	quiescent supply current	pin ICTL is LOW	–	–	50	mA
		pin ICTL is HIGH	–	–	25	mA
I_{leak}	leakage current	V_{C1} = 4.5 V; pin EN is LOW	–	–	5	μA
Inputs EN and ICTL						
V_{IL}	LOW-level input voltage		–	–	1.1	V
V_{IH}	HIGH-level input voltage		1.5	–	–	V

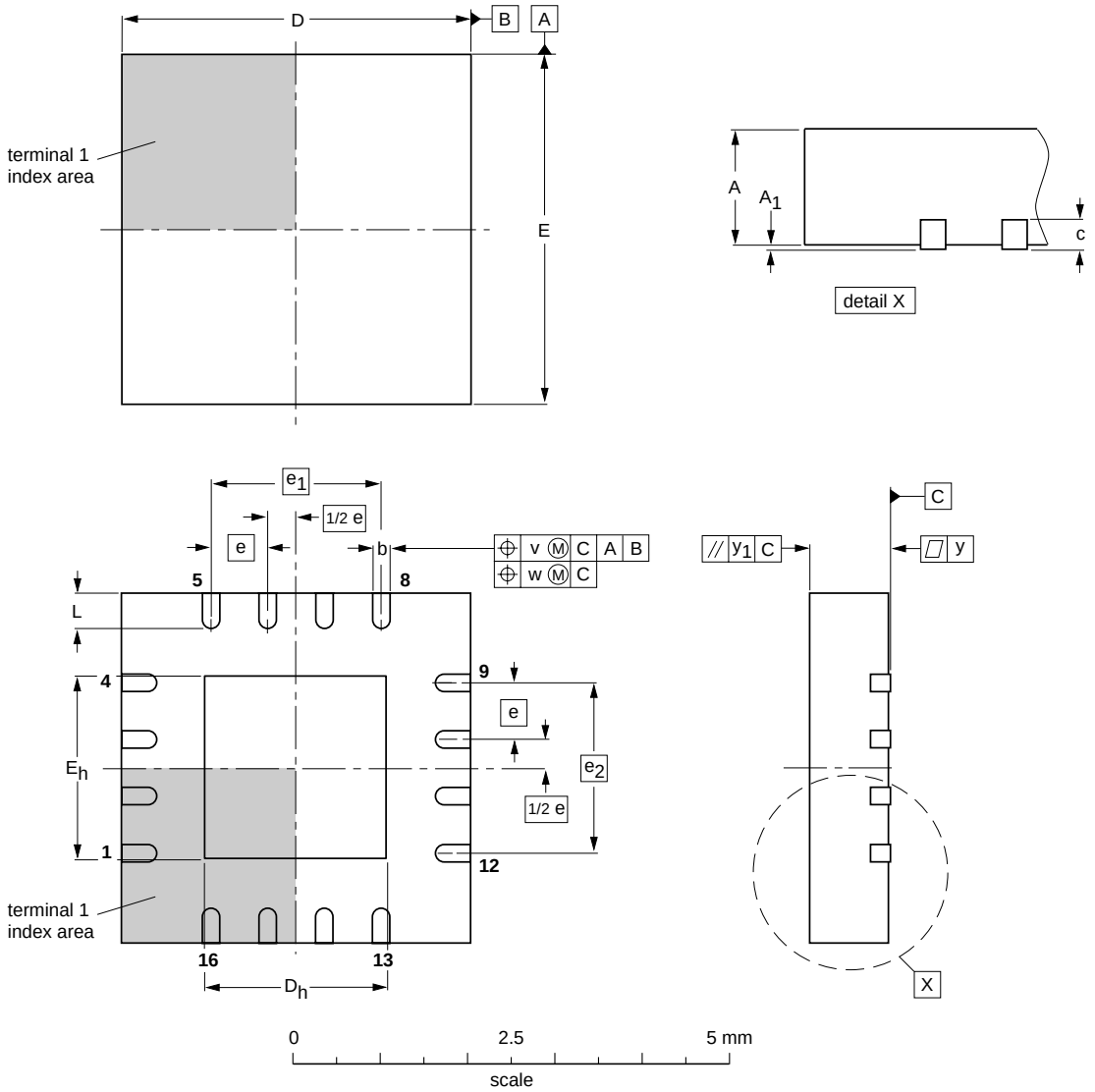
AC CHARACTERISTICS

V_{C1} = 3.6 V; V_{reg} = 2.7 V; T_{amb} = 25 °C; f_{RF} = 1920 to 1980 MHz; P_i adjusted for P_o = 24.5 dBm; R_{ext} = 2.2 kΩ; measured and guaranteed on Philips evaluation board; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_i	input power	T_{amb} = –30 to +70 °C	–6	–	0	dBm
$P_{o(max)}$	maximum output power	T_{amb} = –30 to +70 °C; V_{C1} = 3.25 V	22.5	–	–	dBm
η	efficiency		30	–	–	%
$N_{o(RX)}$	output noise in RX band	at 190 MHz offset; f_{RF} = 2110 to 2170 MHz	–	–	–135	dBm/Hz
H2	second-harmonic level		–	–	–40	dBc
H3	third-harmonic level		–	–	–45	dBc
$CPR_{(adj)}$	adjacent channel power ratio	B = 3.84 MHz; at 5 MHz from carrier frequency	–	–	–37	dBc
$CPR_{(alt)}$	first alternate channel power ratio	B = 3.84 MHz; at 10 MHz from carrier frequency	–	–	–47	dBc
RL_i	input return loss	T_{amb} = –30 to +70 °C; f_{RF} = 1.5 to 2.5 GHz	–	–	–6	dB
$G_{(ripple)}$	ripple gain	Δf_{RF} = 5 MHz; f_{RF} = 1920 to 1980 MHz	–	–	0.5	dB
ΔG	gain variation	P_o up to 24.5 dBm; pin ICTL is LOW	–	–	tbf	dB

PACKAGE OUTLINE

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm **SOT629-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.40 0.23	0.2	4.05 3.95	2.25 1.95	4.05 3.95	2.25 1.95	0.65	1.95	1.95	0.75 0.35	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT629-1	- - -	MO-220	- - -			~~01-06-28~~ 01-08-08

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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Printed in The Netherlands 403506/01/pp12 Date of release: 2002 Jul 02 Document order number: 9397 750 09326

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