256K x 1 DRAM

Features

- Dynamic random access memory 262144 x 1 bit manufactured using a CMOS technology
- $\overline{RAS}$ access times 70 ns, 80 ns
- TTL-compatible
- Three-state output
- 256 refresh cycles
  4 ms refresh cycle time
- FAST PAGE MODE
- Operating modes: Read, Write, Read - Write,
  $\overline{RAS}$ only Refresh,
  Hidden Refresh with address transfer
- Power Supply Voltage 5 V
- Packages PDIP16 (300 mil)
  SOJ20/26 (300 mil)
- Operating temperature range
  0 to 70 °C
- Quality assessment according to CECC 90000, CECC 90100 and CECC 90112

Description

Addressing

The UD61256 is a dynamic Write-Read-memory with random access. FPM facilitates faster data operation with predefined row address. Via 9 address inputs the 18 address bits are transmitted into the internal address memories in a time-multiplex operation. The falling $\overline{RAS}$-edge takes over the row address. During $\overline{RAS}$ Low, the column address together with the $\overline{CAS}$ signal are taken over. The selection of one or more memory circuits can be made by activation of the $\overline{RAS}$ input.

Read-Write-Control

The choice between Read or Write cycle is made at the $\overline{W}$ input. HIGH at the $\overline{W}$ input causes a Read cycle, meanwhile LOW leads to a Write cycle.

Both $\overline{CAS}$-controlled and $\overline{W}$-controlled Write cycles are possible with activated $\overline{RAS}$ signal.

Data Output Control

The usual state of the data output is the High-Z state. Whenever $\overline{CAS}$ is inactive (HIGH), Q will float (High-Z). Thus, $\overline{CAS}$ functions as data output control.

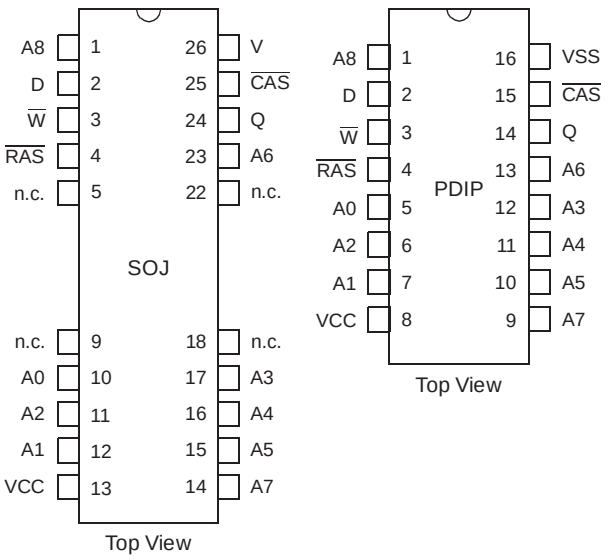
After access time, in case of a Read cycle, the output is activated, and it contains the logic „0“ or „1“.

Q is then valid until $\overline{CAS}$ returns into to inactive state (HIGH).

The memory cycle being a Read, Read-Write or a Write cycle ($\overline{W}$-controlled), Q changes from High-Z state to the active state („0“ or „1“). After the access time the contents of the selected cell is available, except for the Write cycle.

The output remains active until $\overline{CAS}$ becomes inactive, irrespective of $\overline{RAS}$ becoming inactive or not. The memory cycle being a Write cycle ($\overline{CAS}$-controlled), the data output keeps its High-Z state throughout the whole cycle. This configuration makes Q fully controllable by the user merely through the timing of $\overline{W}$. The output storaging the data, they remain valid from the end of access time until the start of another cycle.

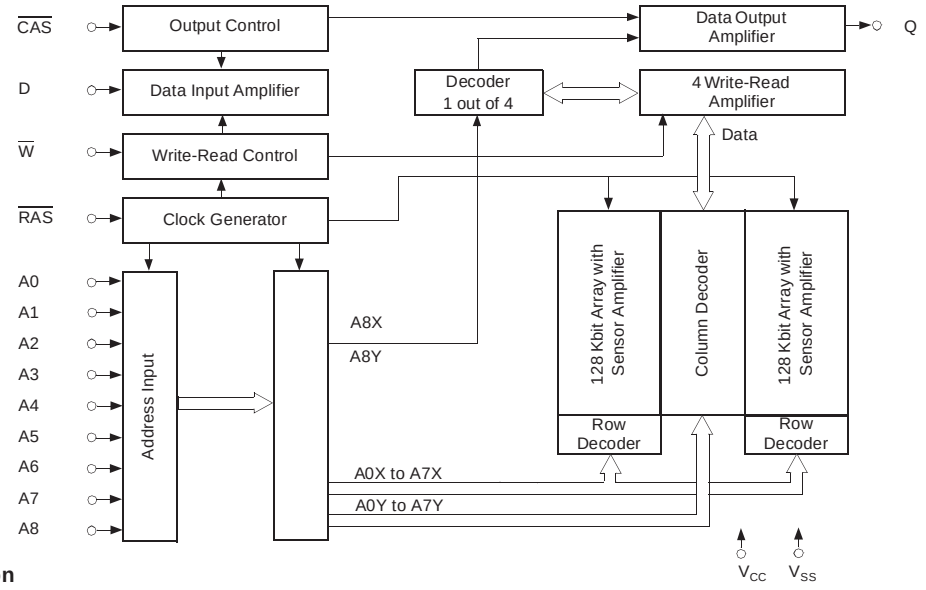
Pin Configuration



Pin Description

Signal Name	Signal Description
A0 - A8	Address Inputs
D	Data Input
$\overline{W}$	Read, Write Control
$\overline{RAS}$	Row Address Strobe
UCC	Power Supply Voltage
USS	Ground
$\overline{CAS}$	Column Address Strobe
Q	Data Output
n.c.	no connected

Block Diagram



Operation

Function		RAS	CAS	W	Address		Data	
					R	C	D	Q
Stand-by		H	X	X	X	X	X	High-Z
Read		L	L	H	Row	Column	X	Output Data
Write		L	L	L	Row	Column	Input Data	High-Z
Read-Write		L	L	H → L	Row	Column	Input Data	Output Data
FPM Read	1st cycle	L	H → L	H	Row	Column	X	Output Data
	2nd cycle	L	H → L	H		Column	X	Output Data
FPM Write	1st cycle	L	H → L	L	Row	Column	Input Data	High-Z
	2nd cycle	L	H → L	L		Column	Input Data	High-Z
FPM Read-Write	1st cycle	L	H → L	H → L	Row	Column	Input Data	Output Data
	2nd cycle	L	H → L	H → L		Column	Input Data	Output Data
RAS only Refresh		L	H	X	Row		X	High-Z
HIDDEN Refresh*)	Read	L → H → L	L	H	Row	Column	X	Output Data
	Write	L → H → L	L	L	Row	Column	Input Data	High-Z

*) Transfer of Refresh Address required

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).
All characteristics are valid in the power supply voltage range and operating temperature range indicated below.

Absolute Maximum Ratings	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	-0.5	7.0	V
Input Voltage [1)]	V_I	-1.0	7.0	V
Output Voltage [1)]	V_O	-1.0	7.0	V
Output Current	I_O	-50	50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_a	0	70	°C
Storage Temperature	T_{stg}	-55	125	°C

Remarks: see page 7

Recommended Operating Conditions	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
Input Low Voltage [1)]	V_{IL}	-1.0	0.8	V
Input High Voltage	V_{IH}	2.4	5.5	V

Remark: see page 7

Capacitances	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance A0 to A8, D	V_{CC} = 5.0 V V_I = V_{SS} f = 1 MHz T_a = 25 °C	C_{I1}		6	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		C_{I2}		7	pF
Output Capacitance		C_O		7	pF

All pins not under test must be connected with ground by capacitors.

Static Characteristics	Conditions	Symbol	Min.		Max.		Unit
			07	08	07	08	
Power Supply Current (average value of $\overline{RAS}$-$\overline{CAS}$ cycles) 2)	$t_{cW} = t_{cWmin}$ $t_{cR} = t_{cRmin}$	I_{CC1}			70	60	mA
Refresh Current (average value of $\overline{RAS}$ cycles) 2)	$t_{cW} = t_{cWmin}$ $t_{cR} = t_{cRmin}$ $\overline{CAS} = V_{IH}$	I_{CC2}			70	60	mA
FPM Current (average value of FPM cycles) 2)	$t_{cPG} = t_{cPGmin}$ $\overline{RAS} = V_{IL}$	I_{CC3}			50	40	mA
Stand-by Current (TTL Level)	$\overline{RAS} = \overline{CAS} = V_{IH}$	I_{CC4}			2	2	mA
Stand-by Current (CMOS Level)	$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V	I_{CC5}			1	1	mA
Output High Voltage	$I_{OH} = -5$ mA	V_{OH}	2.4	2.4			V
Output Low Voltage	$I_{OL} = 4.2$ mA	V_{OL}			0.4	0.4	V
Input Leakage Current at any input, all other pins = 0 V	$V_I = 0$ V to 5.5 V	I_I	-10	-10	10	10	µA
Output Leakage Current Q = High-Z	$V_O = 0$ V to 5.5 V $\overline{RAS} = \overline{CAS} = V_{IH}$	I_O	-10	-10	10	10	µA

Remarks: see page 7

Dynamic Characteristics 3)	Symbol		Min.		Max.		Unit
	Alt.	IEC	07	08	07	08	
❒ ALL CYCLES							
Transition Time (Rise and Fall) 4)	t_T	t_t	3	3	50	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	$t_{w(RASH)}$	50	60			ns
$\overline{CAS}$ Precharge Time	t_{CP}	$t_{w(CASH)}$	10	10			ns
Row Address Set-up Time	t_{ASR}	$t_{su(RA-RAS)}$	0	0			ns
Column Address Set-up Time	t_{ASC}	$t_{su(CA-CAS)}$	0	0			ns
Row Address Hold Time	t_{RAH}	$t_{h(RAS-RA)}$	10	10			ns
Column Address Hold Time	t_{CAH}	$t_{h(CAS-CA)}$	15	15			ns
Column Address Hold Time ref. to $\overline{RAS}$	t_{AR}	$t_{h(RAS-CA)}$	55	60			ns
Output Buffer Turn-off Delay 5)	t_{OFF}	$t_{v(CAS)}$	0	0	20	20	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	$t_{CASH-RASL}$	5	5			ns
$\overline{RAS}$ to Column Address Delay Time 6)	t_{RAD}	t_{RAS-CA}	15	15	35	40	ns
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	$t_{CA-RASH}$	35	40			ns
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	$t_{CASL-QX}$	0	0			ns
Refresh Period	t_{REF}	t_{rf}			4	4	ms
❒ READ							
Random Read Cycle Time 12)	t_{RC}	t_{cR}	130	150			ns
Access Time from $\overline{RAS}$ 7), 8)	t_{RAC}	$t_{a(RAS)}$			70	80	ns
Access Time from Column Address 7), 8)	t_{AA}	$t_{a(CA)}$			35	40	ns
Access Time from $\overline{CAS}$ 7), 8)	t_{CAC}	$t_{a(CAS)}$			20	20	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	$t_{w(RASL)}$	70	80	10000	10000	ns
$\overline{CAS}$ Pulse Width	t_{CAS}	$t_{w(CASL)}$	20	20	10000	10000	ns
Read Command Set-up Time	t_{RCS}	$t_{su(R-CAS)}$	0	0			ns
Read Command Hold Time ref. to $\overline{RAS}$ 9)	t_{RRH}	$t_{h(RAS-R)}$	0	0			ns
Read Command Hold Time 9)	t_{RCH}	$t_{h(CAS-R)}$	0	0			ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time 6)	t_{RCD}	$t_{RASL-CASL}$	20	20	50	60	ns
$\overline{CAS}$ Hold Time	t_{CSH}	$t_{RASL-CASH}$	70	80			ns
$\overline{RAS}$ Hold Time	t_{RSH}	$t_{CASL-RASH}$	20	20			ns
❒ WRITE							
Random Write Cycle Time 12)	t_{RC}	t_{cW}	130	150			ns
$\overline{RAS}$ Pulse Width	t_{RAS}	$t_{w(RASL)}$	70	80	10000	10000	ns
$\overline{CAS}$ Pulse Width	t_{CAS}	$t_{w(CASL)}$	20	20	10000	10000	ns
Write Command Pulse Width	t_{WP}	$t_{w(W)}$	15	15			ns

Remarks: see page 7

Dynamic Characteristics [3]	Symbol		Min.		Max.		Unit
	Alt.	IEC	07	08	07	08	
❒ WRITE (continuation)							
Write Command Set-up Time [10]	t_{WCS}	$t_{su(W-CAS)}$	0	0			ns
Data Set-up Time ref. to $\overline{CAS}$ [11]	t_{DS}	$t_{su(D-CAS)}$	0	0			ns
Data Set-up Time ref. to $\overline{W}$ [11]	t_{DS}	$t_{su(D-W)}$	0	0			ns
Write Command Hold Time	t_{WCH}	$t_{h(CAS-W)}$	15	15			ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	$t_{h(W-RAS)}$	20	20			ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	$t_{h(W-CAS)}$	20	20			ns
Data Hold Time ref. to $\overline{RAS}$	t_{DHR}	$t_{h(RAS-D)}$	55	60			ns
Data Hold Time ref. to $\overline{CAS}$	t_{DH}	$t_{h(CAS-D)}$	15	15			ns
Data Hold Time ref. to $\overline{W}$	t_{DH}	$t_{h(W-D)}$	15	15			ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time [6]	t_{RCD}	$t_{RASL-CASL}$	20	20	50	60	ns
$\overline{CAS}$ Hold Time	t_{CSH}	$t_{RASL-CASH}$	70	80			ns
$\overline{RAS}$ Hold Time	t_{RSH}	$t_{CASL-RASH}$	20	20			ns
❒ READ-WRITE							
Read-Write Cycle Time [12]	t_{RWC}	t_{cRW}	155	175			ns
$\overline{RAS}$ Pulse Width	t_{RAS}	$t_{w(RASL)RW}$	95	105	10000	10000	ns
$\overline{CAS}$ Pulse Width	t_{CAS}	$t_{w(CASL)RW}$	45	45	10000	10000	ns
$\overline{CAS}$ Hold Time	t_{CSH}	$t_{(RASL-CASH)RW}$	95	105			ns
$\overline{RAS}$ to $\overline{WRITE}$ Delay Time [10]	t_{RWD}	t_{RAS-W}	70	80			ns
$\overline{CAS}$ to $\overline{WRITE}$ Delay Time [10]	t_{CWD}	t_{CAS-W}	20	20			ns
Column to $\overline{WRITE}$ Delay Time [10]	t_{AWD}	$t_{(CA-W)RW}$	35	40			ns
❒ FPM							
Fast Page Mode Cycle Time [12]	t_{PC}	t_{cPG}	50	50			ns
$\overline{RAS}$ Pulse Width	t_{RASP}	$t_{w(RASL)}$	70	80	100000	100000	ns
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	$t_{a(CASH)}$	35	40			ns
❒ HIDDEN-REFRESH							
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	t_{CHR}	$t_{RASL-CASH}$	15	15			ns

Remarks: see page 7

Remarks:

1) The Input Low Voltage must not drop below -0.3 V for more than 40 ns.

2) The current is inversely proportional to the cycle time; the max. current is measured in the shortest cycle time.

3) For test conditions see test configuration for functional test and timing diagrams.

4) V_{IHmin} and V_{ILmax} are reference levels for time measurement of the input signals; transition times are measured between V_{IH} and V_{IL}.

5) $t_{v(CAS)}$ and $t_{v(RAS)}$ define the time at which the data output goes to High-Z; this time is not related to any level.

6) $t_{RASL-CASLmax}$ and t_{RAS-CA} are given as reference points only; they do not represent restrictive conditions.

7) The access time is determined by the three times $t_{a(RAS)}$, $t_{a(CAS)}$ and $t_{a(CA)}$:

- if $t_{RASL-CASL} < t_{RASL-CASLmax}$ and $t_{RAS-CA} < t_{RAS-CAmax}$ $\mathbf{t_{a(RAS)}}$ is valid,

- if $t_{RASL-CASL} > t_{RASL-CASLmax}$ and $t_{su(CA-CAS)} < (t_{a(CA)max} - t_{a(CAS)max})$ $\mathbf{t_{a(CA)}}$ is valid,

- if $t_{RASL-CASL} > t_{RASL-CASLmax}$ and $t_{su(CA-CAS)} > (t_{a(CA)max} - t_{a(CAS)max})$ $\mathbf{t_{a(CAS)}}$ is valid.

8) Measured with a load equivalent to 2 TTL loads.

9) In a READ cycle either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be kept.

10) $t_{su(W-CAS)}$, t_{RAS-W}, t_{CAS-W} and $t_{su(A)}$ do not represent restrictive parameters:

- if $t_{su(W-CAS)} \geq t_{su(W-CAS)min}$, the cycle is a WRITE cycle ($\overline{CAS}$-controlled) and the data output remains in High-Z throughout the whole $\overline{CAS}$ cycle,

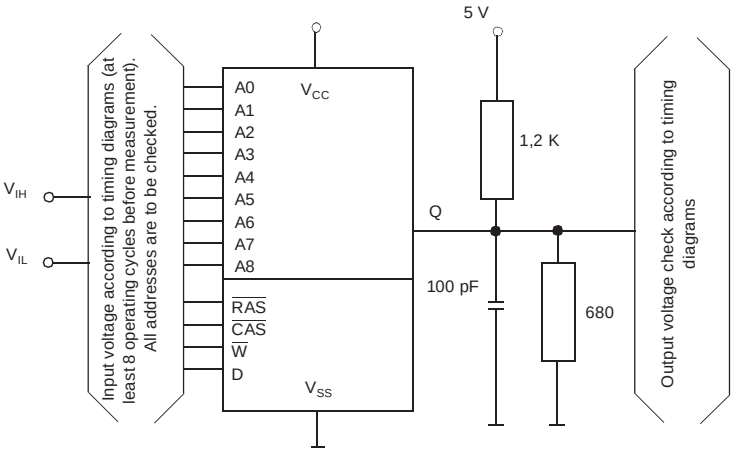
- if $t_{CAS-W} > t_{CAS-Wmin}$, $t_{RAS-W} > t_{RAS-Wmin}$ and $t_{su(CA-W)RW} > t_{su(CA-W)RWmin}$, the cycle is a READ-WRITE cycle and the content of the cell is available at the data output,

- if none of these conditions is satisfied, the condition of the data output (at access time) is indeterminate, since a WRITE cycle ($\overline{W}$-controlled) is carried out.

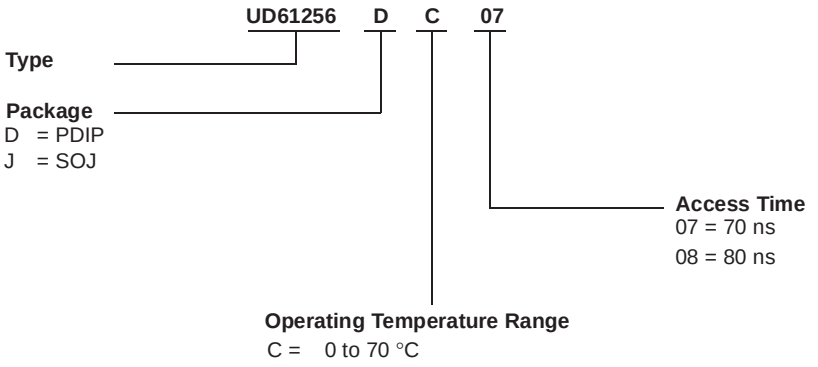
11) These parameters refer to $\overline{CAS}$ in the WRITE cycle ($\overline{CAS}$-controlled) and to $\overline{W}$ during WRITE ($\overline{W}$-controlled) or to $\overline{W}$ in the READ-WRITE cycle, resp.

12) The values of t_{cmin} are used for indication of the particular cycle time in which full function is guaranteed in the temperature range from 0 to 70 °C. Values below the one shown above may cause permanent damage to the component.

Test Configuration for Functional Check

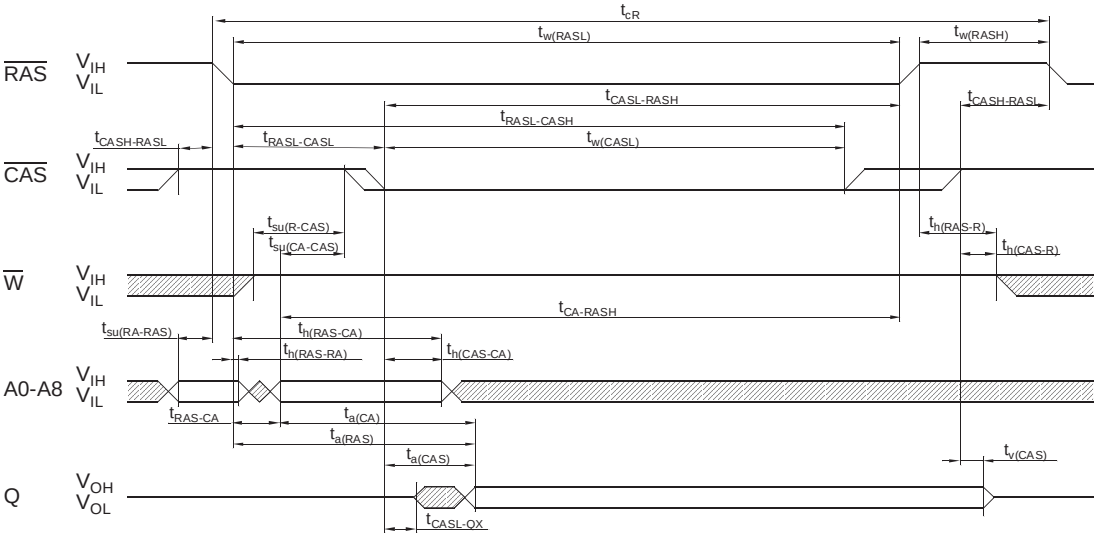


IC Code Numbers

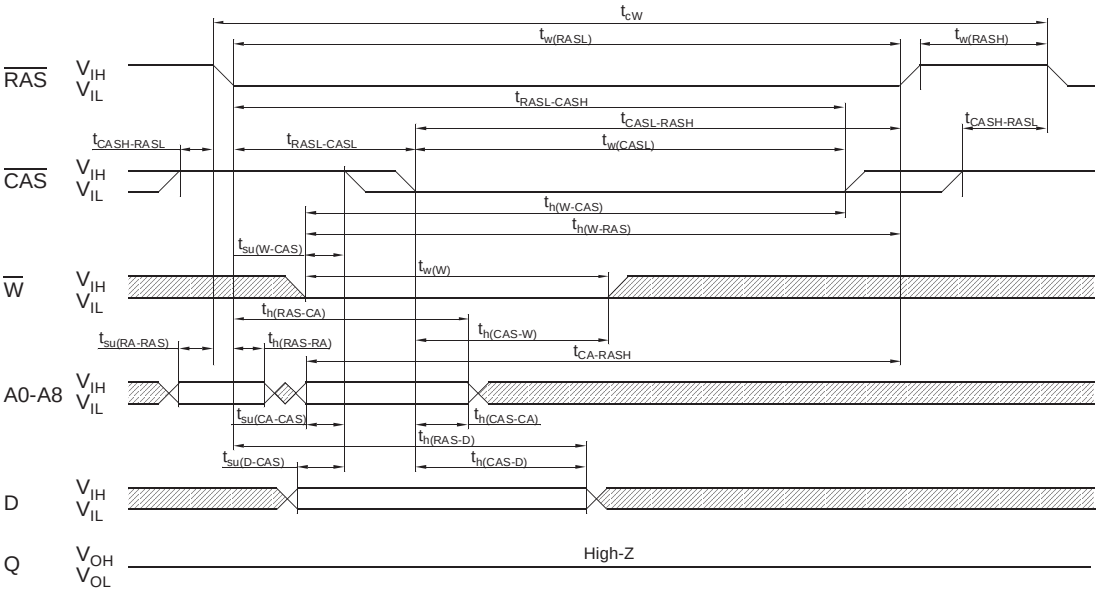


The date of manufacture is given by the 4 last digits of the mark, the 2 first digits indicating the year, and the last 2 digits the calendar week.

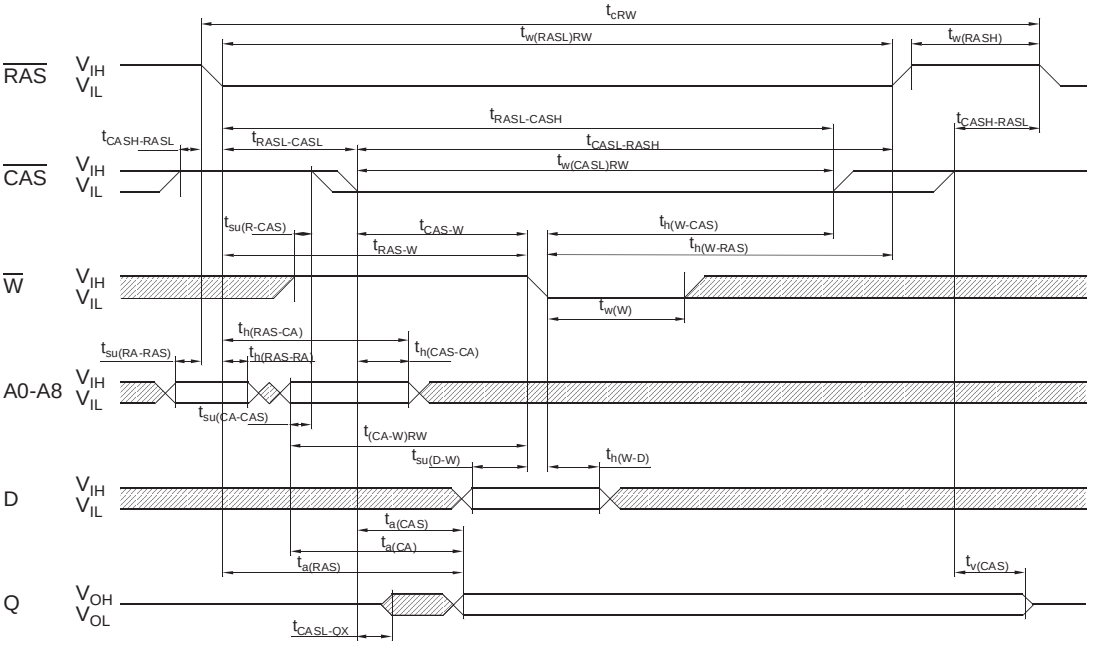
Read



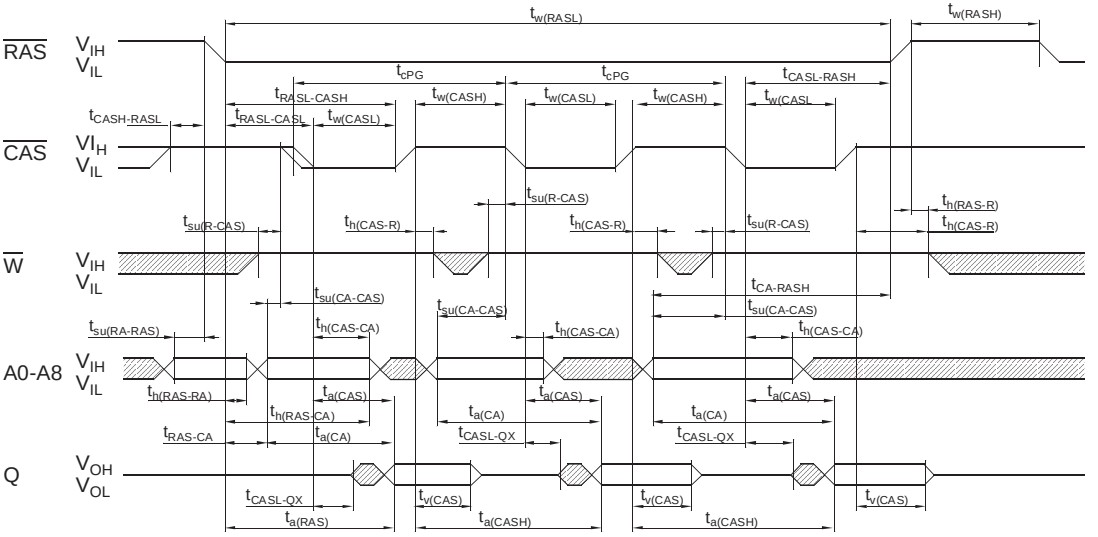
Write ($\overline{\text{CAS}}$-controlled)



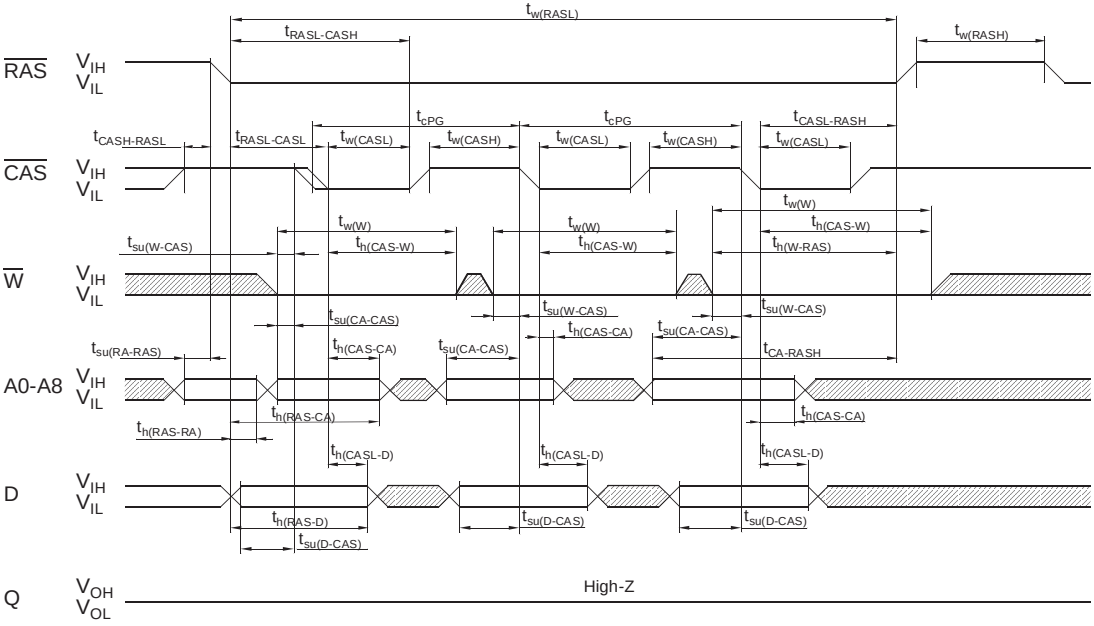
Read-Write



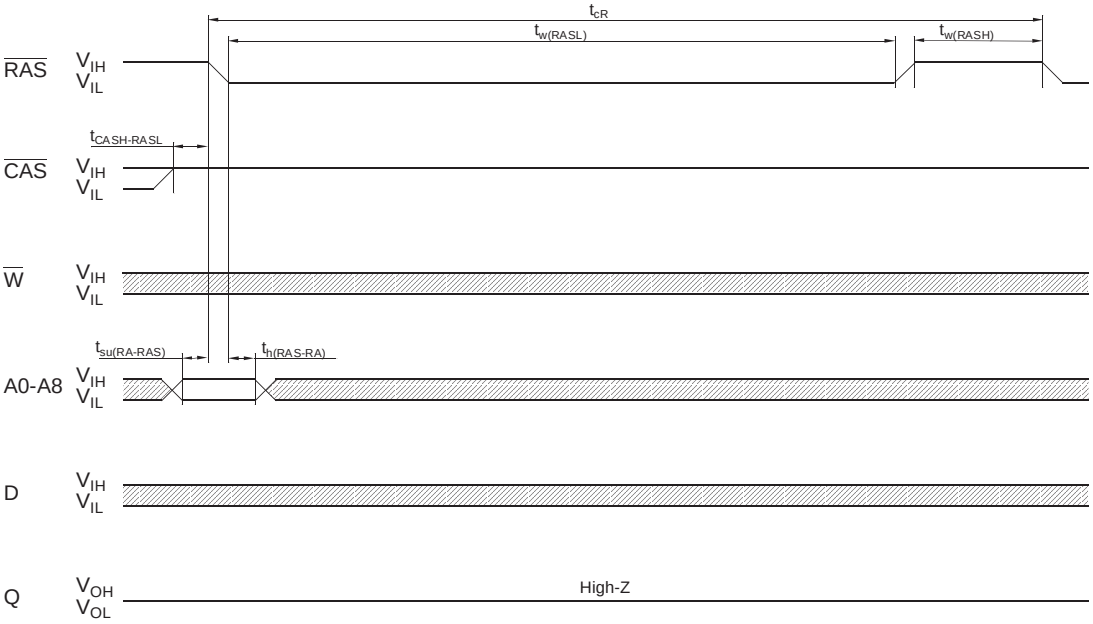
FPM Read



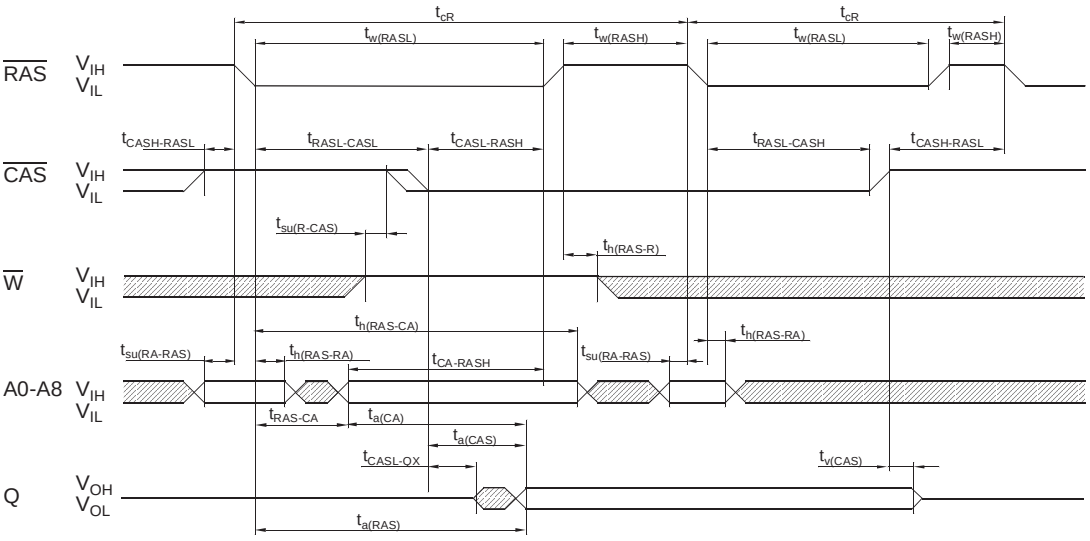
FPM Write ($\overline{CAS}$-controlled)



$\overline{RAS}$ only Refresh



HIDDEN-Refresh with address transfer



Memory Products 1998
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