

Dual Line ESD Protection Diode Array

UESD6V8S2B SOT523

General Description

The UESD6V8S2B of TVS diode array is designed to protect sensitive electronics from damage or latch-up due to ESD. For use in applications where board space is at a premium. It is unidirectional device and may be used on lines where the signal polarities are above ground, each device will protect up to two lines.

TVS diodes are solid-state devices feature large cross-sectional area junctions for conducting high transient currents, specifically for transient suppression. It offers desirable characteristics for board level protection including fast response time, low operating, low clamping voltage, and no device degradation.

The UESD6V8S2B may be used to meet the immunity requirements of IEC 61000-4-2, $\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge and MIL-STD-883 METHOD 3015, $\pm 8\text{KV}$ HBM. The small package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

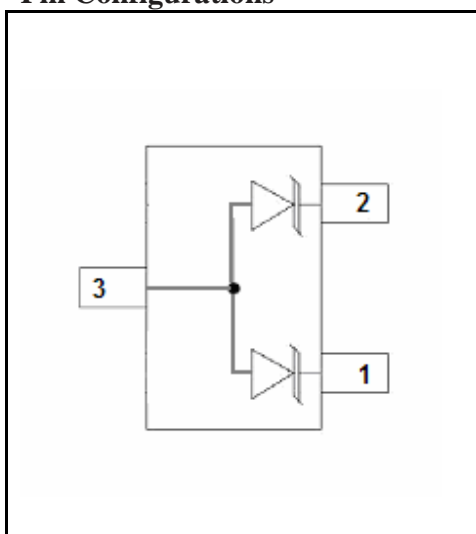
Applications

Cellular Handsets & Accessories
 Cordless Phones
 Personal Digital Assistants (PDA's)
 Notebooks & Handhelds
 Portable Instrumentation
 Digital Cameras
 Peripherals
 MP3 Players

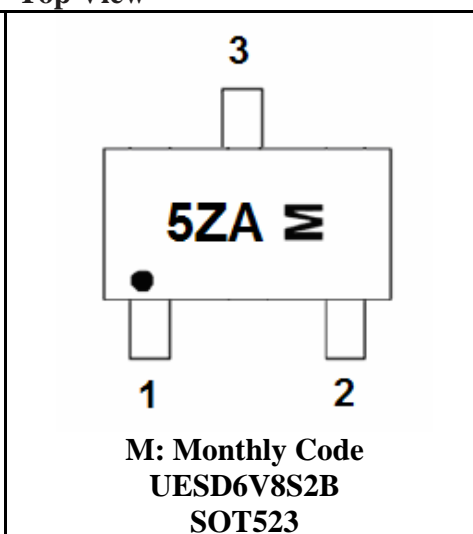
Features

Transient protection for data & power lines to
 IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
 MIL-STD-883 3015 (HBM) $\pm 8\text{ kV}$
 Protect two I/O lines
 Working Voltages: 5V
 Low Leakage current
 Low operating and clamping voltage
 Solid-state silicon avalanche technology

Pin Configurations



Top View



Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UESD6V8S2B	5.0V	SOT523	2	5ZA	3000/7 Inch Reel

Absolute Maximum Ratings

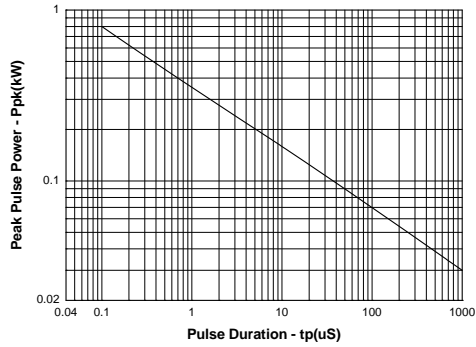
RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20 \mu s$)	P_{PK}	140	Watts
Peak Pulse Current ($t_p = 8/20 \mu s$)	I_{PP}	11	A
Lead Soldering Temperature	T_L	260(10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Electrical Characteristics

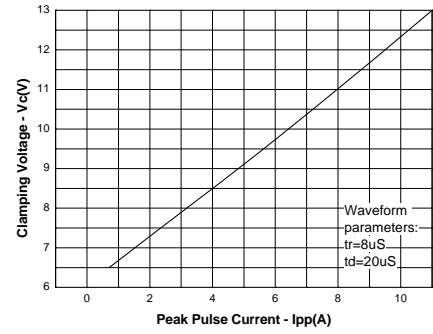
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	6	6.8	7.2	V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T=25^\circ C$			0.1	μA
Clamping Voltage	V_C	$I_{PP} = 5A, t_p = 8/20\mu S$			9.1	V
		$I_{PP} = 11A, t_p = 8/20\mu S$			13	
Junction Capacitance	C_J	Pin 1,2 to 3 $V_R = 0V, f = 1MHz$		40	50	pF
Junction Capacitance	C_J	Pin 1,2 to 3 $V_R = 2.5V, f = 1MHz$		30	40	pF
Reverse dynamic resistance	$R_{dyn,rev}$	$I_{PP} = 1A \sim 5A$		0.6		Ω
Forward dynamic resistance	$R_{dyn,fwd}$			0.5		Ω

Typical Operating Characteristics

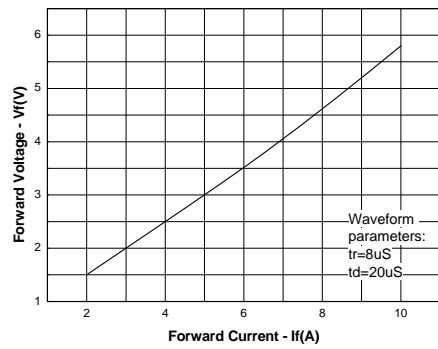
Non-Repetitive Peak Pulse Power vs. Pulse Time



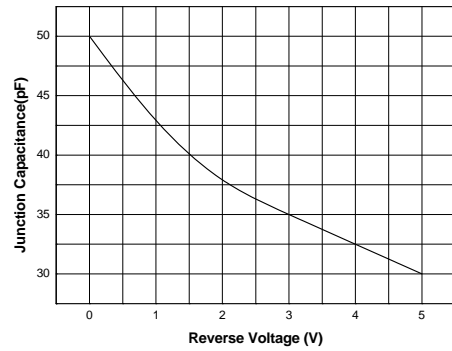
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage



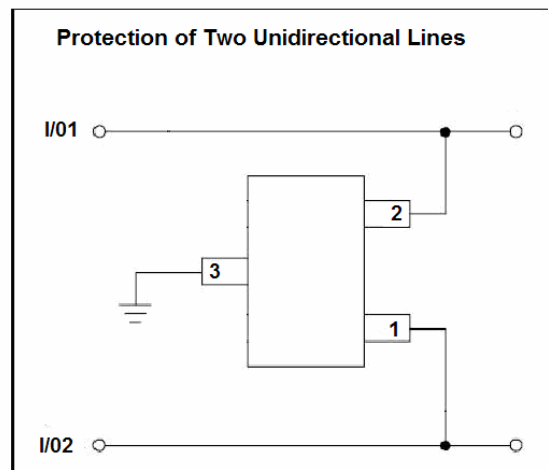
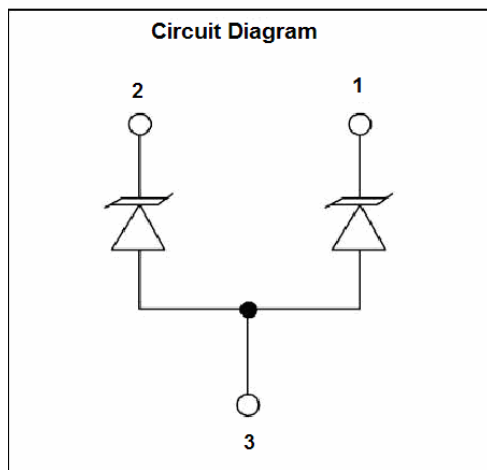
Applications Information

UESD6V8S2B ESD protection diode is designed to protect dual data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode should be placed towards the line that is to be protected.

Device Connection for Protection of Dual Data Lines

The Dual TVS Diode Array is designed to protect up to two unidirectional data lines. The device is connected as follows:

Unidirectional protection of two I/O lines is achieved by connecting pins 1 and 2 to the data lines. Pin 3 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.



Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
- Keep parallel signal paths to a minimum.
- Avoid running protection conductors in parallel with unprotected conductor.
- Minimize all printed-circuit board conductive loops including power and ground loops.
- Avoid using shared transient return paths to a common ground point.

Package Information

UESD6V8S2B SOT523

Outline Drawing

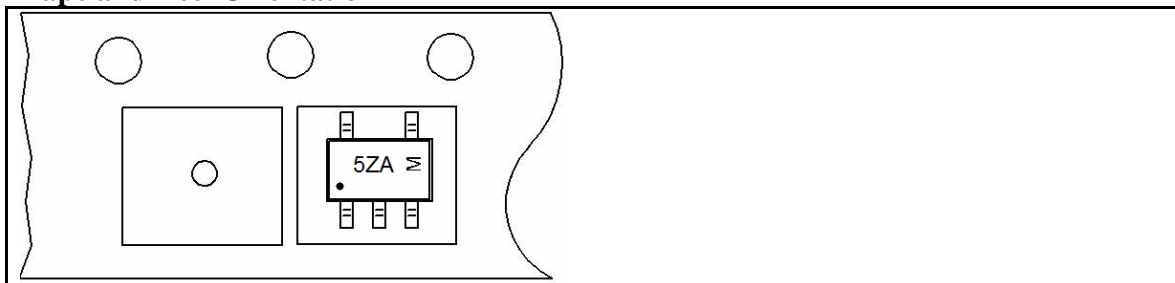
SOT-523			
Dim	Min	Max	Typ
A	0.15	0.30	0.22
B	0.75	0.85	0.80
C	1.45	1.75	1.60
D	—	—	0.50
G	0.90	1.10	1.00
H	1.50	1.70	1.60
J	0.00	0.10	0.05
K	0.60	0.80	0.75
L	0.10	0.30	0.22
M	0.10	0.20	0.12
N	0.45	0.65	0.50
α	0°	8°	—
All Dimensions in mm			

Land Pattern

NOTES:

- Compound dimension: 1.60×0.80 ;
- Unit: mm;
- General tolerance $\pm 0.05\text{mm}$ unless otherwise specified;
- The layout is just for reference.

Tape and Reel Orientation



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