

ULC7534P5

Description

The ULC7534P5 is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from over-voltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

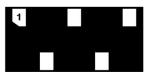
Feature

- ♦ 75 Watts Peak Pulse Power per Line (tp=8/20µs)
- Protects Four High Speed Lines
- Low Clamping Voltage
- RoHS Compliant
- ◆ IEC61000-4-2(ESD):±17kV (air discharge) ±15kV (contact discharge);
- ♦ IEC61000-4-4 (EFT) 40A (5/50 η s)
- ♦ IEC61000-4-5 (LIGHTING) 3A (8/20 μ s)

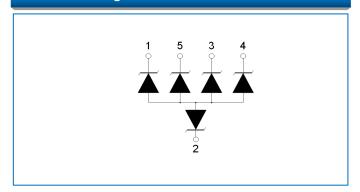
Applications

- ◆ USB 3.0 / USB 3.1 Interfaces
- ♦ HDMI 1.4 / HDMI 2.0 Interfaces
- ♦ Video Graphics Cards
- ♦ Notebooks, Desktops, and Servers
- Portable Instrumentation
- ♦ Industrial Controls
- Peripherals

DFN2010P5



Functional Diagram



Mechanical Data

- ◆ DFN2010P5 (2.0x1.0x0.5mm) Package
- Molding Compound Flammability Rating: UL 94V-O
- Weight 3.5 Millgrams (Approximate)
- ◆ Quantity Per Reel: 3,000pcs
- Reel Size : 7 inch
- Lead Finish : Lead FreeDevice Marking: UL5A

Mechanical Characteristics

Symbol	Parameter	Value	Units
Ррр	Peak Pulse Power (tp=8/20µs waveform)	75	Watts
TJ	Operating Junction Temperature Range	-40 to +125	°C
T _{STG}	Storage Temperature Range	-55 to +150	°C
T∟	Soldering Temperature, T max = 10s	260	°C



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Electrical Characteristics (@ 25℃ Unless Otherwise Specified)

Characteristics	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Reverse Working Voltage	V _{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I _T =1mA	6			V
Reverse Leakage Current	I _R	V _{RWM} =5V ; T=25°C			0.1	μA
Junction capacitance	CJ	I/O To GND;V _R =0V , f=1MHz ;		0.2		pF
Positive Clamping		I _{PP} =1A , T _P =8/20μS ;			15	V
Voltage	Vc	I _{PP} =3A , T _P =8/20μS ;			25	

Characteristic Curves

Fig1. Power Derating Curve

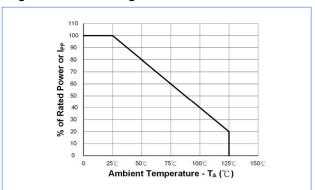


Fig3. Clamping Voltage vs. Peak Pulse Current (tp=8/20us)

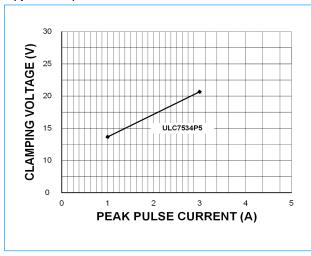


Fig2. Insection Loss (S21)

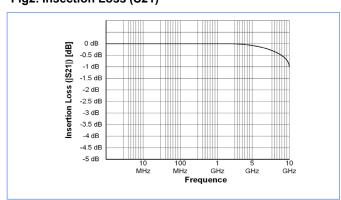
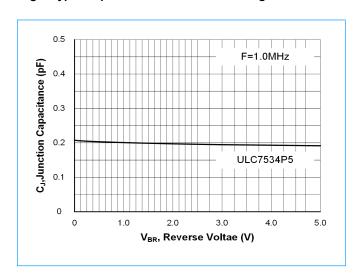


Fig4. Typic Capacitance vs. Reverse Voltage

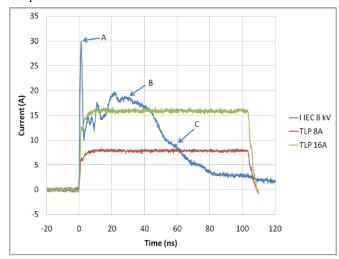




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Transmission Line Pulse (TLP)

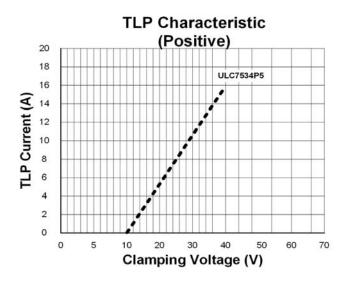
Transmission Line Pulse (TLP) is a measurement technique used in the Electrostatic Discharge (ESD) arena to characterize performance attributes of devices under ESD stresses. TLP is able to obtain current versus voltage (I–V) curves in which each data point is obtained with a 100 ns long pulse, with currents up to 40 A. TLP was first used in the ESD field to study human body model (HBM) in integrated circuits, but it is an equally valid tool in the field of system level ESD. The applicability of TLP to system level ESD is illustrated in Figure 1, which compares an 8 kV IEC 61000–4–2 current waveform with TLP current pulses of 8 and 16 A. The current levels and time duration for the pulses are similar and the initial rise time for the TLP pulse is comparable to the rise time of the IEC 61000–4–2's initial current spike. This application note will give a basic introduction to TLP measurements and explain the datasheet parameters extracted from TLP for SDI Technology's protection products.



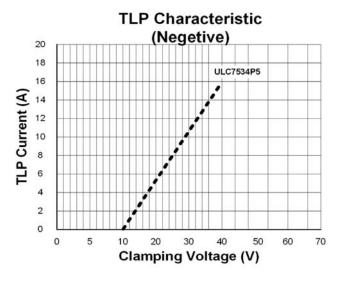
Comparison of a Current
Waveform of IEC 61000-4-2
with TLP Pulses at 8 and 16 A.

The IEC 61000–4–2 ESD waveforms is true to the Standard and is shown here as captured on an oscilloscope. The points A, B, and C show the points on the waveforms specified in IEC 61000–4–2.

TLP Characteristic (Positive)



TLP Characteristic (Negetive)



Please refer to www.unsemi.com.tw for current information.

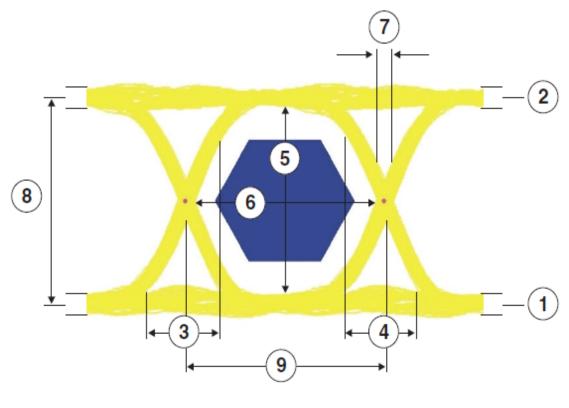


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Eye Diagram

- 1 Zero Level: measure of the mean value of the logical 0.
- One Level: measure of the mean value of the logical 1.
- Rise Time: measure of the transition time of the data from the 10% level to the 90% level on the upward slope.
- Fall Time: measure of the transition time of the data from the 90% level to the 10% level on the downward slope.
- 5 Eye Height: measure of the vertical opening. Determine eye closure due to noise.
- Eye Width: measure of the horizontal opening.

 Determine influence of jitter on the eye opening.
- 7 Deterministic Jitter: deviation of a transition from its ideal time caused by reflections relative to other transitions.
- 8 Eye Amplitude : difference between the logic 0 level and the logic 1 level histogram mean value.
- 9 Bit Rate: inverse of the bit period.



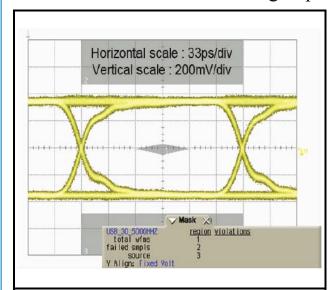
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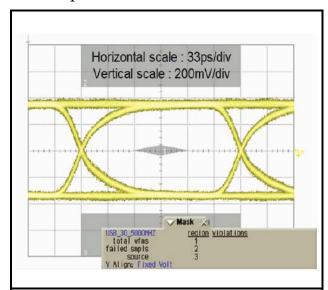
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Eye Diagram at 5Gbps and 10Gbps

High Speed Test: 5Gbps

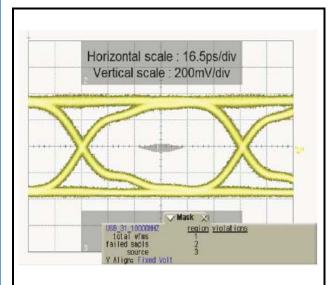


Eye Diagram -- USB 3.0 mask at 5.0Gbps. Without Component

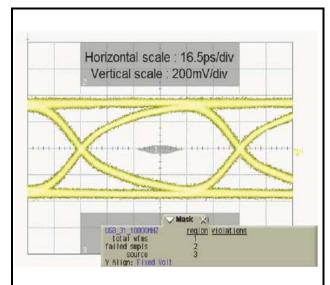


Eye Diagram -- USB 3.0 mask at 5.0Gbps. With Component

High Speed Test: 10Gbps



Eye Diagram -- USB 3.1 mask at 10.0Gbps. Without Component

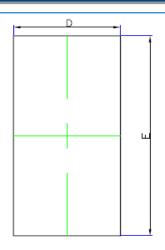


Eye Diagram -- USB 3.1 mask at 10.0Gbps. With Component

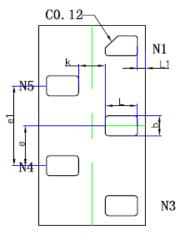


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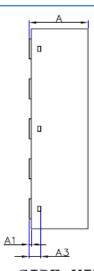
DFN2010P5 Package Outline & Dimensions



TOP VIEW

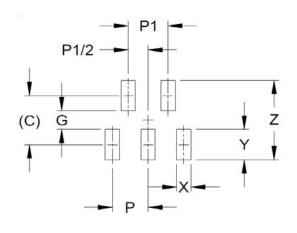


BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min.	Max.	Min.	Max.	
Α	0.340	0.400	0.013	0.016	
A1	-0.004	0.046	0.000	0.002	
A3	0.110REF.		0.004REF.		
D	0.900	1.100	0.035	0.043	
E	1.900	2.100	0.075	0.083	
k	0.250REF.		0.010REF.		
b	0.150	0.250	0.006	0.010	
е	0.400BSC.		0.016BSC.		
e1	0.800BSC.		0.031BSC.		
L	0.224	0.376	0.009	0.015	
L1	0.075REF.		0.003REF.		

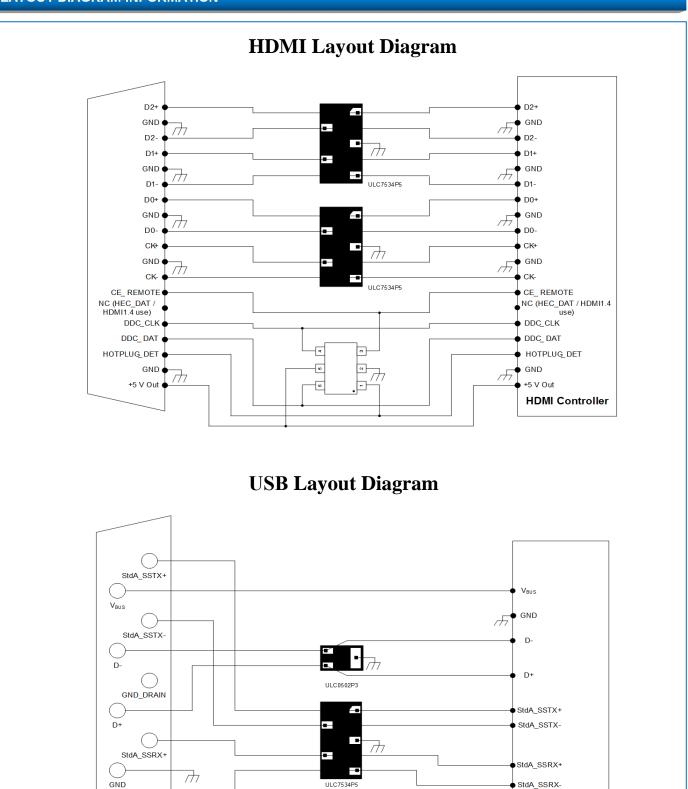


DIMENSIONS		
DIM	MILLIMETERS	
С	(0.65)	
G	0.25	
Р	0.45	
P1	0.50	
X	0.18	
Y	0.40	
Z	1.05	



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LAYOUT DIAGRAM INFORMATION



StdA_SSRX-

USB Controller