

MOS FIELD EFFECT TRANSISTOR μ PA1728

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The μ PA1728 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

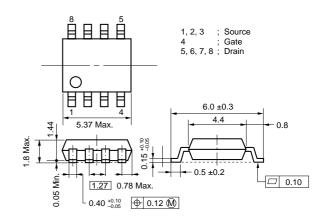
FEATURES

- Single chip type
- Low On-state Resistance
- ★ RDS(on)1 = 19 m Ω (TYP.) (Vgs = 10 V, ID = 4.5 A)
- ★ RDS(on)2 = 23 m Ω (TYP.) (VGS = 4.5 V, ID = 4.5 A)
- ★ RDS(on)3 = 24 m Ω (TYP.) (VGS = 4.0 V, ID = 4.5 A)
- ★ Low Ciss : Ciss = 1700 pF (TYP.)
 - · Built-in G-S protection diode
 - Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1728	Power SOP8

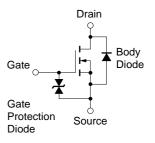
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	60	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC)	ID(DC)	±9	Α
Drain Current (Pulse) Note1	ID(pulse)	±36	Α
Total Power Dissipation (T _A = 25 °C) Note2	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to + 150	°C
Single Avalanche Current Note3	IAS	9	Α
Single Avalanche Energy Note3	Eas	8.1	mJ

EQUIVALENT CIRCUIT



Notes 1. PW \leq 10 μ s, Duty cycle \leq 1 %

- 2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm
- 3. Starting Tch = 25°C, RG = 25 Ω , TGS = 20 V \rightarrow 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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90 %

10 %

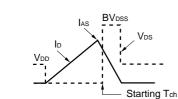


★ ELECTRICAL CHARACTERISTICS (TA = 25 °C, All terminals are connected.)

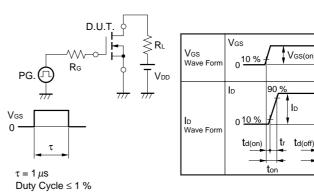
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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, Ip = 4.5 A		19	26	mΩ
	RDS(on)2	Vgs = 4.5 V, ID = 4.5 A		23	29	mΩ
	RDS(on)3	Vgs = 4.0 V, ID = 4.5 A		24	34	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 4.5 A	6.0	12		S
Drain Leakage Current	Ipss	V _{DS} = 60 V, V _{GS} = 0 V			10	μΑ
Gate to Source Leakage Current	lgss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Input Capacitance	Ciss	V _{DS} = 10 V		1700		pF
Output Capacitance	Coss	V _G S = 0 V		270		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		130		pF
Turn-on Delay Time	td(on)	ID = 4.5 A		17		ns
Rise Time	tr	V _{GS(on)} = 10 V		69		ns
Turn-off Delay Time	td(off)	V _{DD} = 30 V		77		ns
Fall Time	tf	$R_G = 10 \Omega$		31		ns
Total Gate Charge	Q _G	ID = 9 A		31		nC
Gate to Source Charge	Qgs	V _{DD} = 48 V		4.4		nC
Gate to Drain Charge	QgD	Vgs = 10 V		9.1		nC
Body Diode Forward Voltage	VF(S-D)	IF = 9 A, VGS = 0 V		0.82		V
Reverse Recovery Time	t rr	IF = 9 A, VGS = 0 V		41		ns
Reverse Recovery Charge	Qrr	di/dt = 100A/μs		76		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

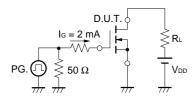
$\begin{array}{c|c} D.U.T. \\ \hline PG. \\ \hline \\ V_{GS} = 20 \rightarrow 0 \ V \end{array} \begin{array}{c} D.U.T. \\ \hline \\ \hline \\ \end{array} \begin{array}{c} V_{DD} \\ \hline \\ \end{array}$



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



NEC μ PA1728

[MEMO]

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