

# MOS FIELD EFFECT TRANSISTOR

# $\mu$ PA1730TP

## SWITCHING

## P-CHANNEL POWER MOS FET

### DESCRIPTION

The  $\mu$ PA1730TP which has a heat spreader is a P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

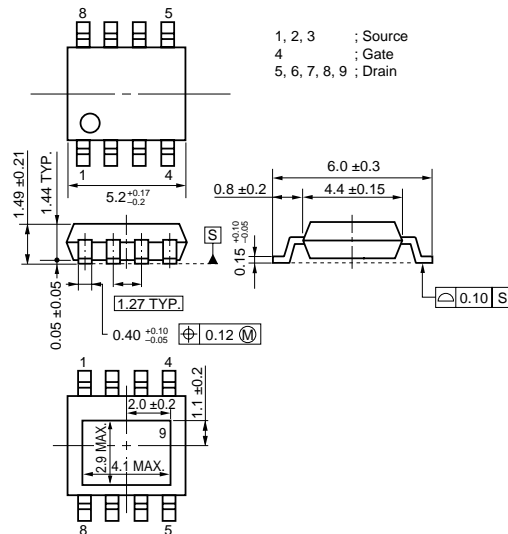
### FEATURES

- Low on-state resistance  
 $R_{DS(on)1} = 9.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -6.5 \text{ A)}$   
 $R_{DS(on)2} = 13.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -6.5 \text{ A)}$   
 $R_{DS(on)3} = 15.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -6.5 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 3800 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power HSOP8)

### ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA1730TP	Power HSOP8

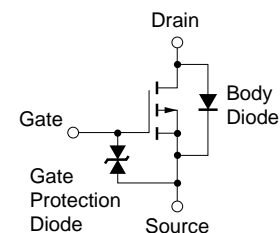
### PACKAGE DRAWING (Unit: mm)



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , Unless otherwise noted, All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-30	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\mp 20$	V
Drain Current (DC)	$I_{D(DC)1}$	$\mp 28$	A
Drain Current (DC) <sup>Note1</sup>	$I_{D(DC)2}$	$\mp 15$	A
Drain Current (pulse) <sup>Note2</sup>	$I_{D(pulse)}$	$\mp 100$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	40	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>Note1</sup>	$P_{T2}$	3	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	-15	A
Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	22.5	mJ

### EQUIVALENT CIRCUIT



- Notes**
1. Mounted on a glass epoxy board (1 inch x 1 inch x 0.8 mm),  $PW = 10 \text{ sec.}$
  2.  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$
  3. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = -15 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = -20 \rightarrow 0 \text{ V}$

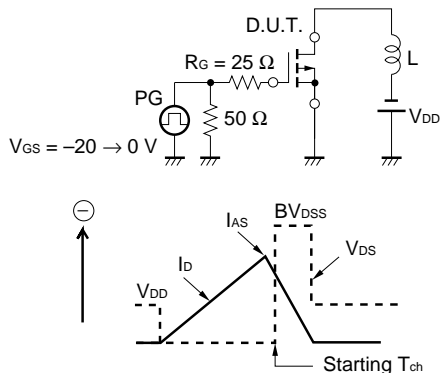
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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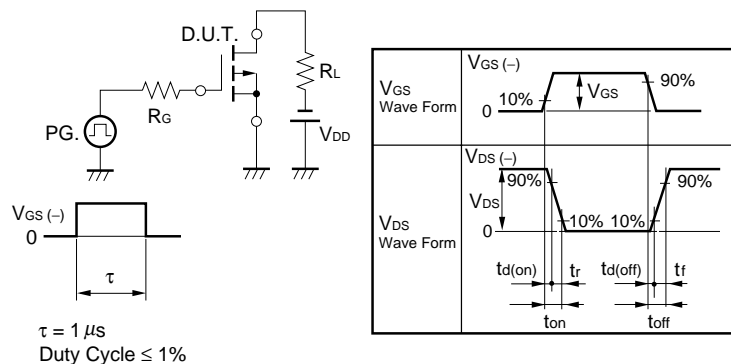
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, Unless otherwise noted, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V			-1	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -6.5 A	11.0	23.0		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -6.5 A		7.6	9.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -6.5 A		10.3	13.5	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -6.5 A		11.3	15.0	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V		3800		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		1200		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		500		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, I <sub>D</sub> = -6.5 A		15		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = -10 V		20		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		130		ns
Fall Time	t <sub>f</sub>			50		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -24 V		70		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -10 V		9		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -13.0 A		17		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 13 A, V <sub>GS</sub> = 0 V		0.80		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 13 A, V <sub>GS</sub> = 0 V		53		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		57		nC

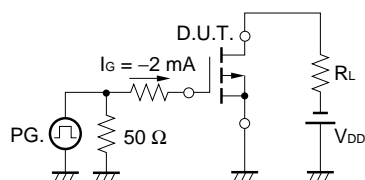
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

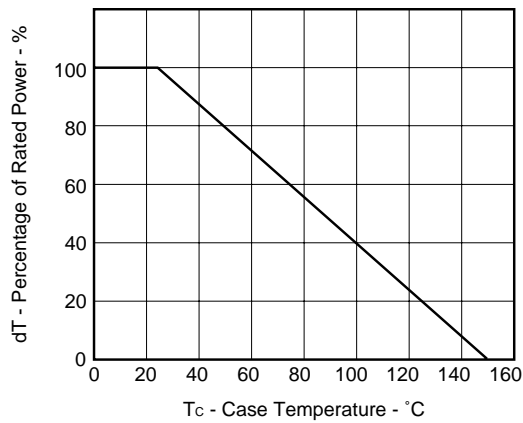


**TEST CIRCUIT 3 GATE CHARGE**

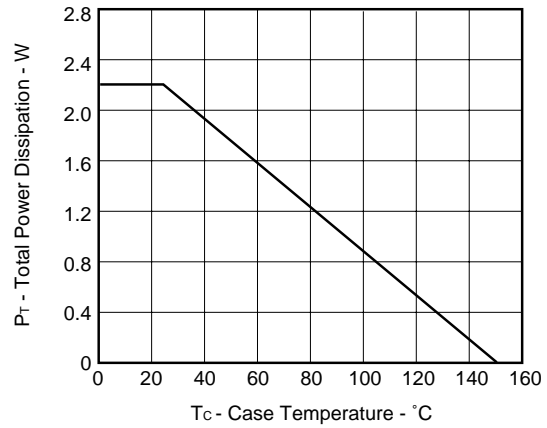


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

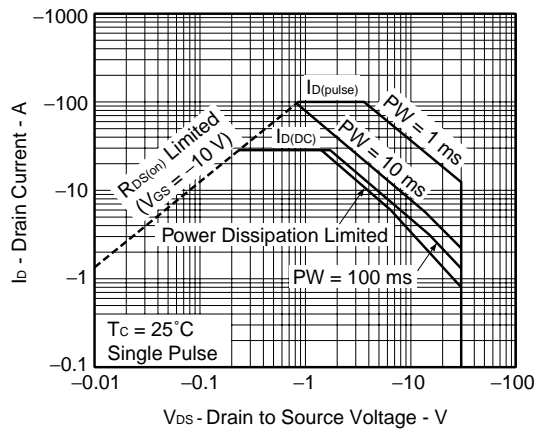
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



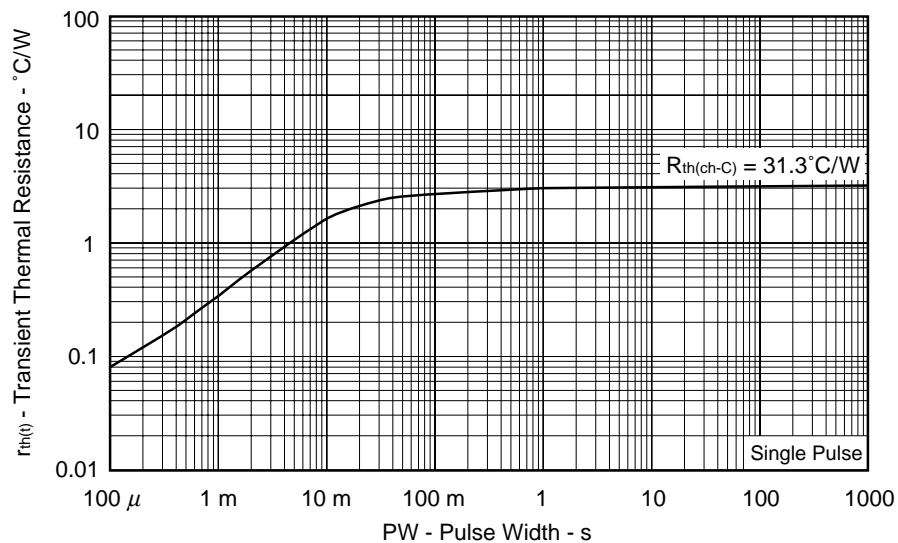
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



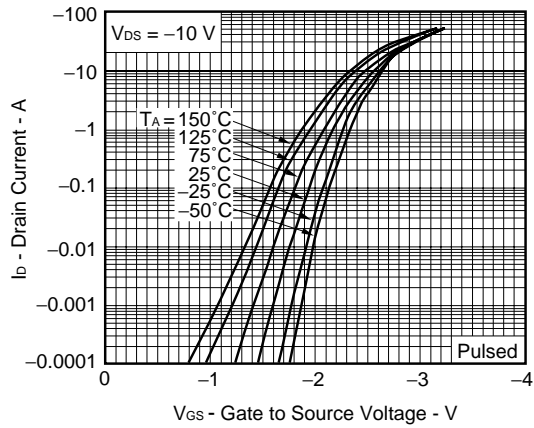
FORWARD BIAS SAFE OPERATING AREA



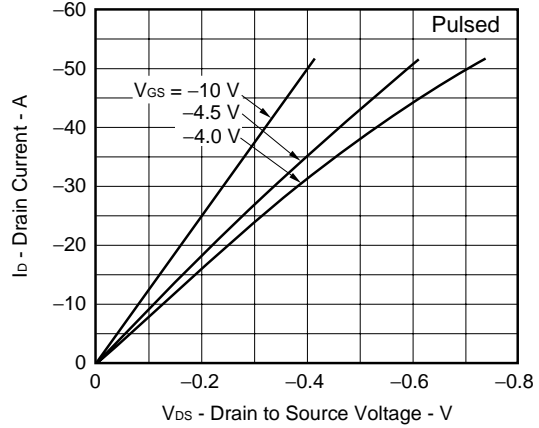
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



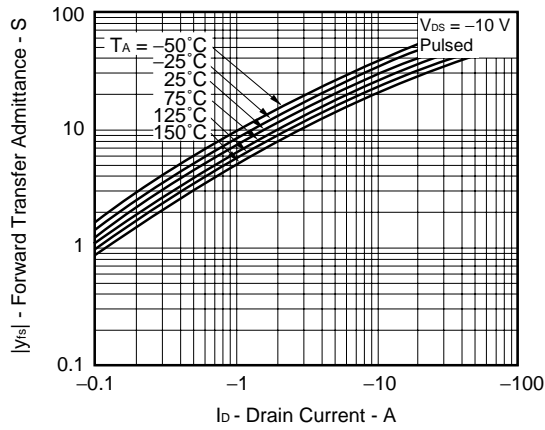
FORWARD TRANSFER CHARACTERISTICS



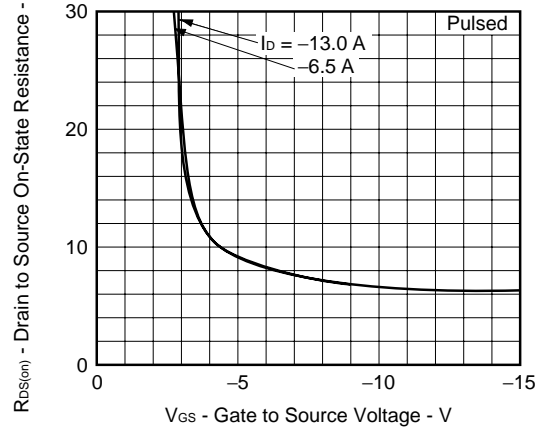
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



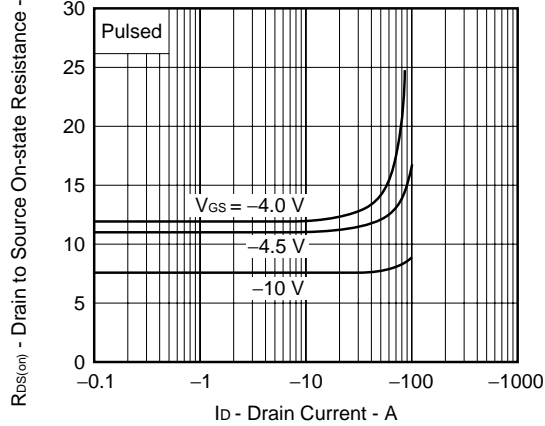
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



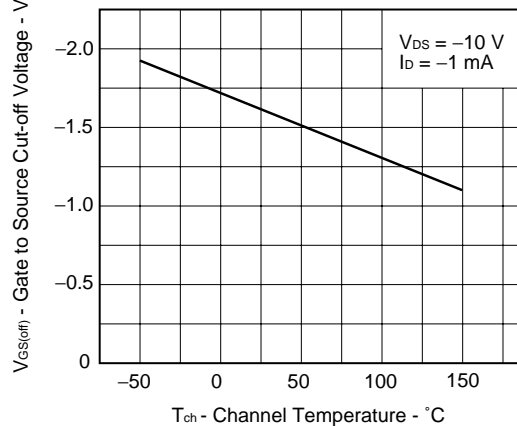
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

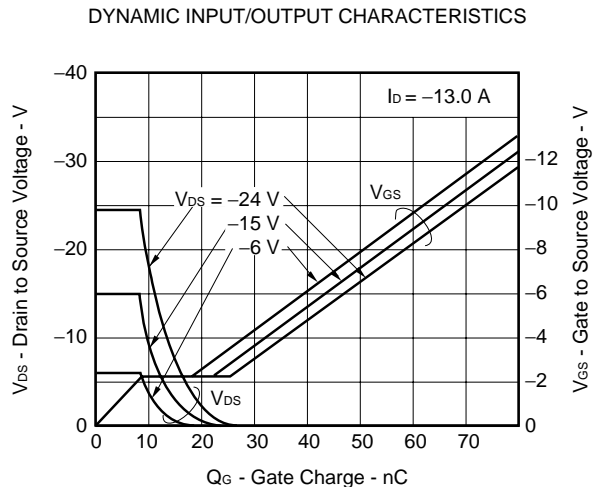
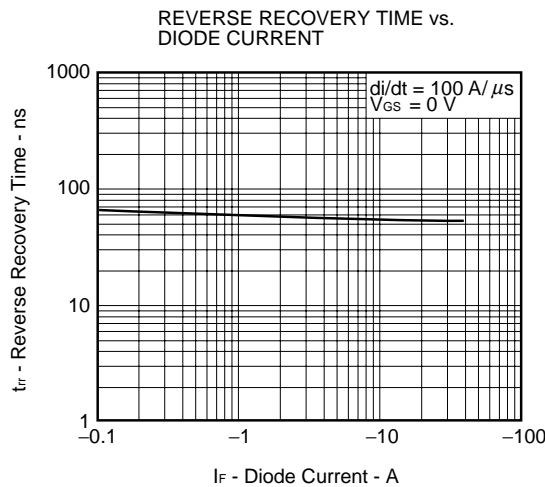
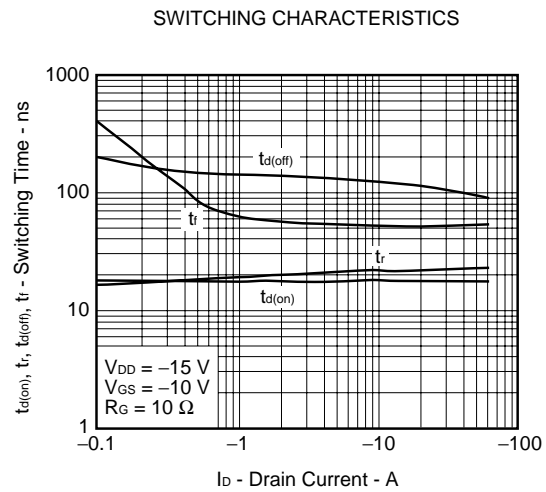
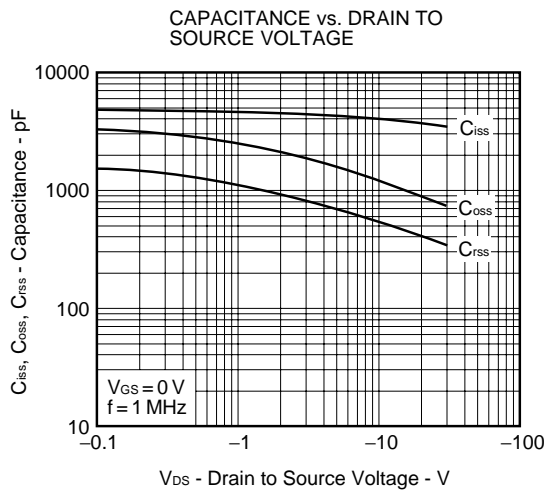
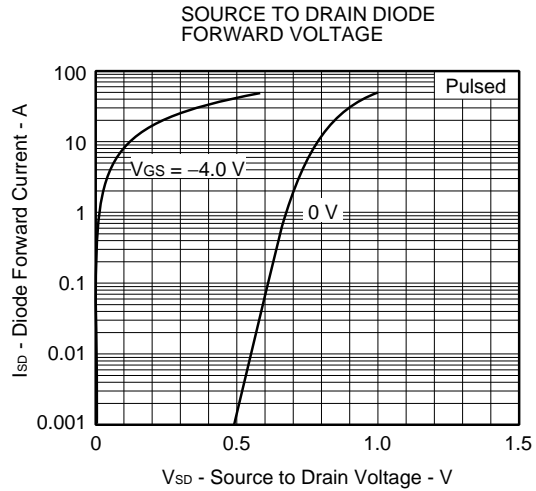
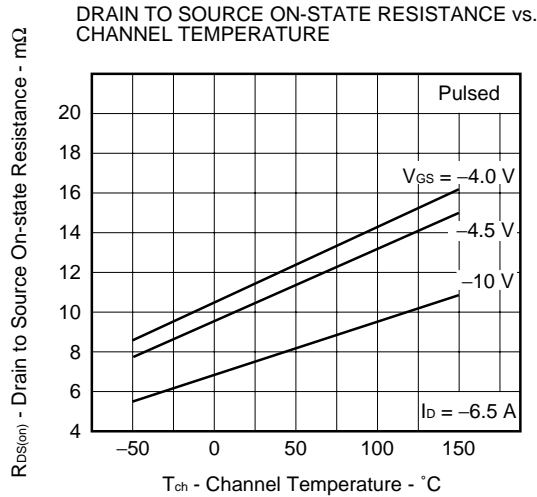


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE





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