DATA SHEET

NEC

BIPOLAR ANALOG + DIGITAL INTEGRATED CIRCUIT

μPB1008K

REFERENCE FREQUENCY 27.456 MHz, 2ndIF FREQUENCY 132 kHz RF/IF FREQUENCY DOWN-CONVERTER + PLL FREQUENCY SYNTHESIZER IC FOR GPS RECEIVER

DESCRIPTION

The μPB1008K is a silicon monolithic integrated circuit for GPS receiver. This IC is designed as double conversion RF block integrated Pre-Amplifier + RF/IF down-converter + PLL frequency synthesizer on 1 chip.

This IC has IQ recovery function, builds a 2-bit A/D converter in both I channels and Q channels, respectively, and carries them in 36-pin plastic QFN package.

This IC is manufactured using our 30 GHz f_{max} UHS0 (Ultra High Speed Process) silicon bipolar process.

FEATURES

- Double conversion : f_{REFin} = 27.456 MHz, $f_{1stIFin}$ = 175.164 MHz, $f_{2ndIFin}$ = 132 kHz
- Integrated RF block : Pre-Amplifier + RF/IF frequency down-converter + PLL frequency synthesizer
  : The 2-bit A/D converter is unified to single chip.
- Needless to input counter data : fixed division internal prescaler
  - VCO side division : ÷102 (÷8, ÷12.75 serial prescaler)
  - Reference division : ÷2
- Supply voltage : V_{CC} = 2.7 to 3.3 V
- Low current consumption : I_{CC} = 18.0 mA TYP. @ V_{CC} = 3.0 V
- Gain adjustable externally : Gain control voltage pin (control voltage up vs. gain down)
- Power-save function : Power-save dark current I_{CC}(PD) = 10 μA MAX.
- High-density surface mountable : 36-pin plastic QFN

APPLICATIONS

- Consumer use GPS receiver of reference frequency 27.456 MHz, 2nd IF frequency 132 kHz (for general use)

ORDERING INFORMATION

Part Number	Package	Supplying Form
μPB1008K-E1	36-pin plastic QFN	• 12 mm wide embossed taping • Pin 1 indicates pull-out direction of tape • Qty 2.5 kpcs/reel

Remark To order evaluation samples, contact your nearby sales office.
Part number for sample order: μPB1008K

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

Document No. PU10282EJ01V0DS (1st edition)
Date Published November 2003 CP(K)
Printed in Japan

PRODUCT LINE-UP (T_A = +25°C, V_{CC} = 3.0 V)

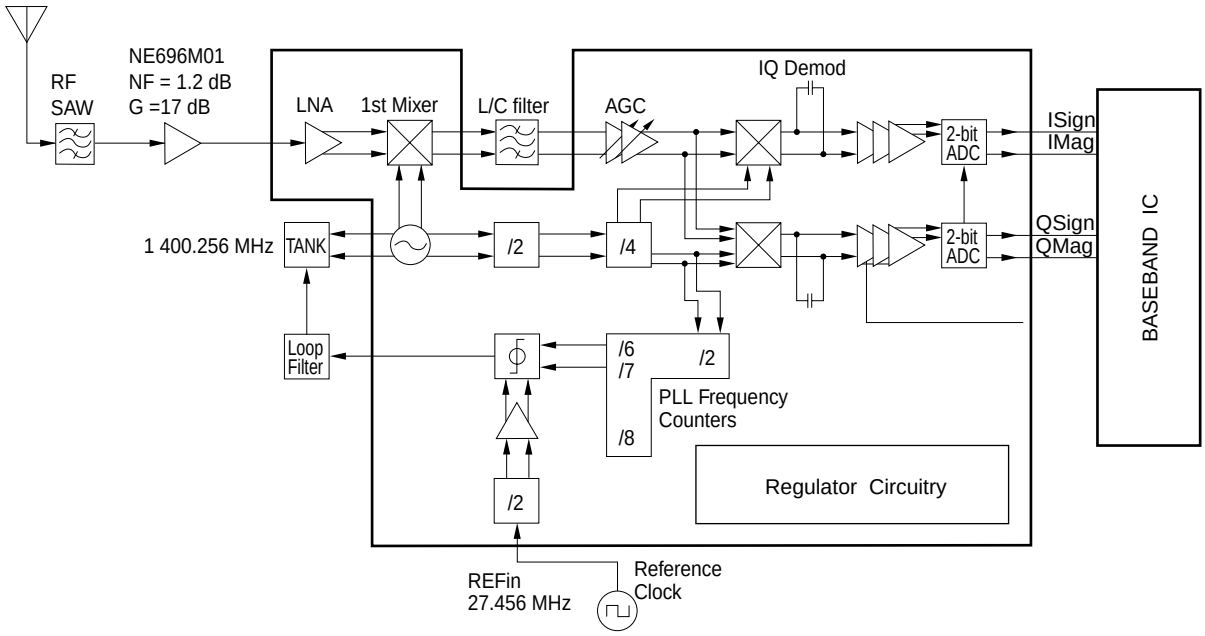
Type	Part Number	Functions (Frequency unit: MHz)	V_{CC} (V)	I_{CC} (mA)	CG (dB)	Package	Status
Clock Frequency Specific 1 chip IC	μPB1008K	Pre-amplifier + RFdown-converter + IQ down-converter + IF amplifier + 2-bit ADC + PLL synthesizer REF = 27.456 1stIF = 175.164/2ndIF = 0.132 On-chip 2-bit ADC	2.7 to 3.3	18.0	100 to 120	36-pin plastic QFN	New Device
	μPB1007K	Pre-amplifier + RF/IF down-converter + PLL synthesizer REF = 16.368 1stIF = 61.380/2ndIF = 4.092	2.7 to 3.3	25.0	100 to 120	36-pin plastic QFN	Available
	μPB1005K	REF = 16.368 1stIF = 61.380/2ndIF = 4.092				36-pin plastic QFN	Available

Remark Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail.
To know the associated products, please refer to their latest data sheets.

SYSTEM APPLICATION EXAMPLE

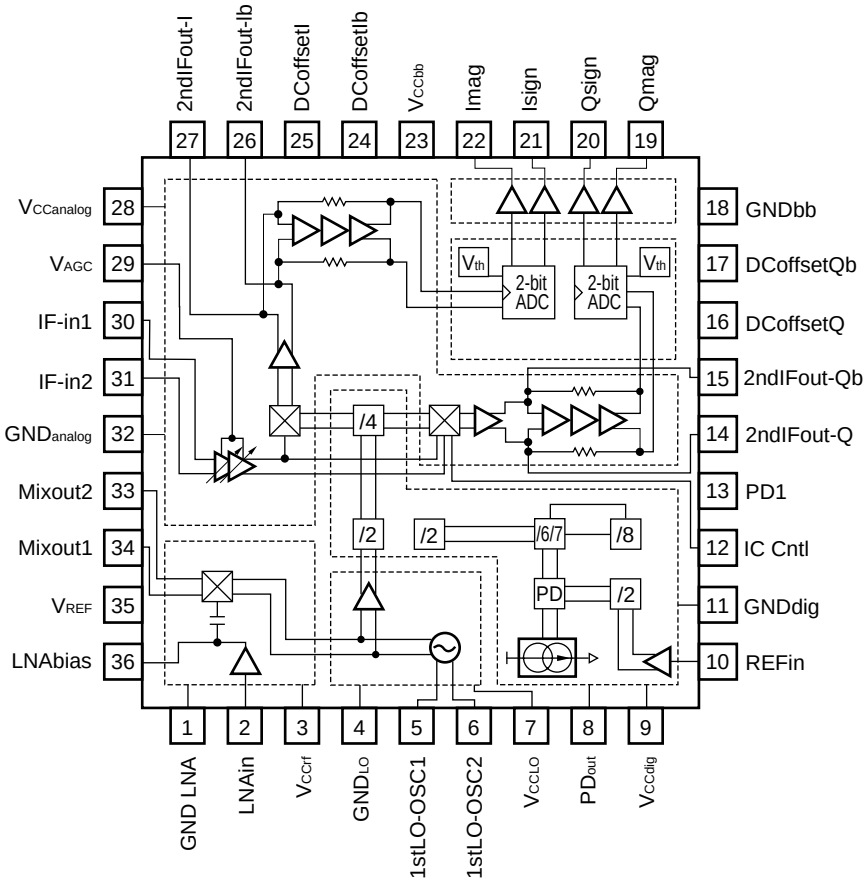
GPS receiver RF block diagram

Basic frequency in a figure is set to f_0= 1.023 MHz.

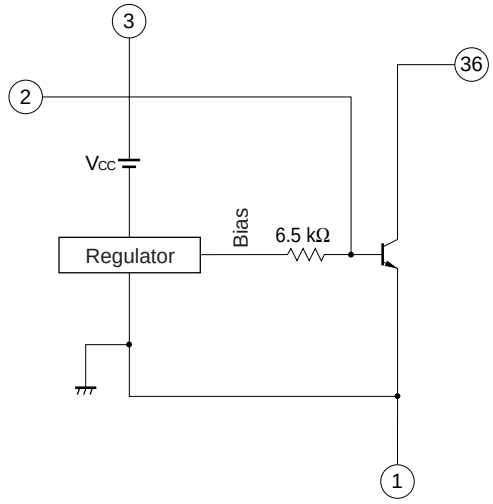
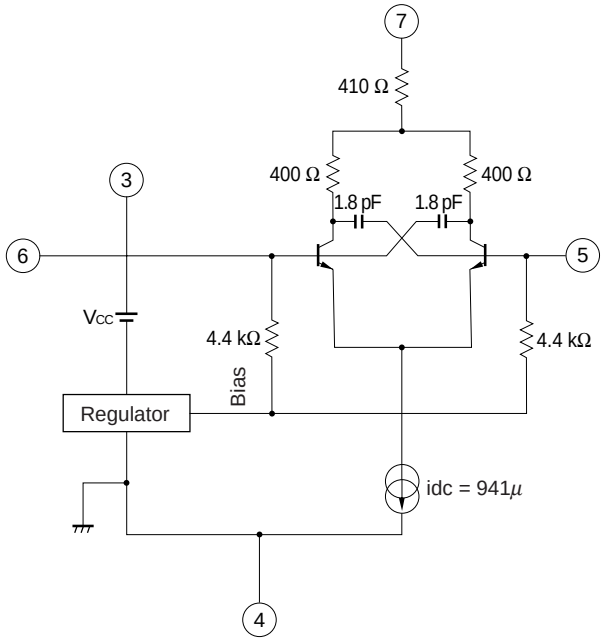
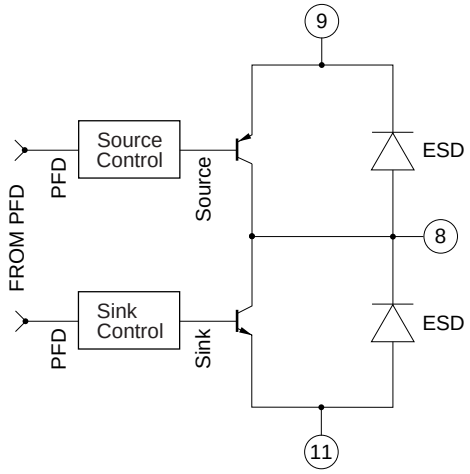


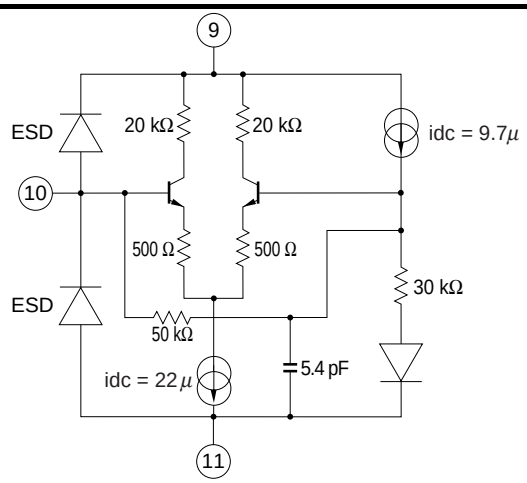
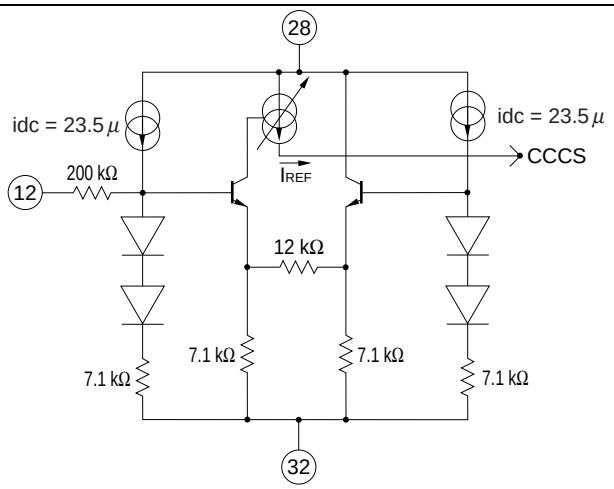
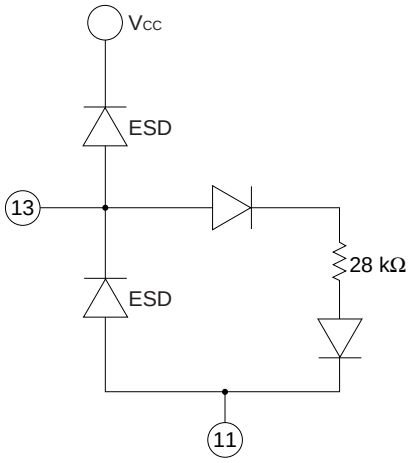
Caution This diagram schematically shows only the μPB1008K's internal functions on the system. This diagram does not present the actual application circuits.

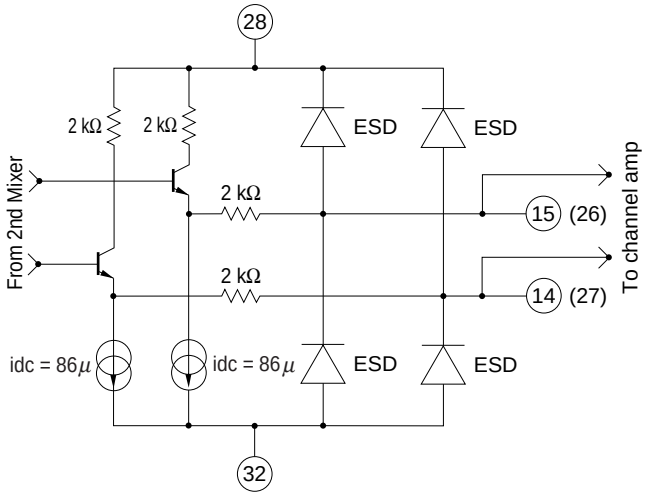
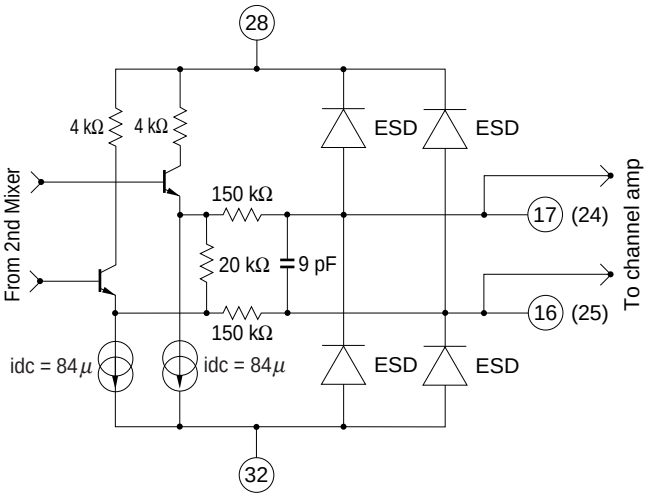
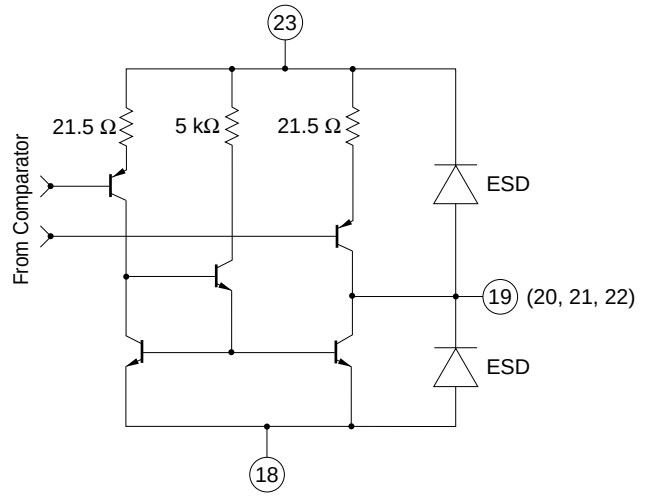
PIN CONNECTION AND INTERNAL BLOCK DIAGRAM

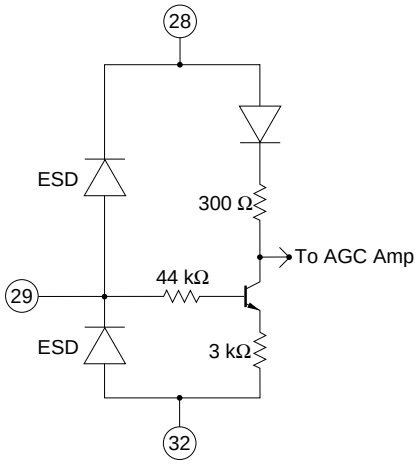
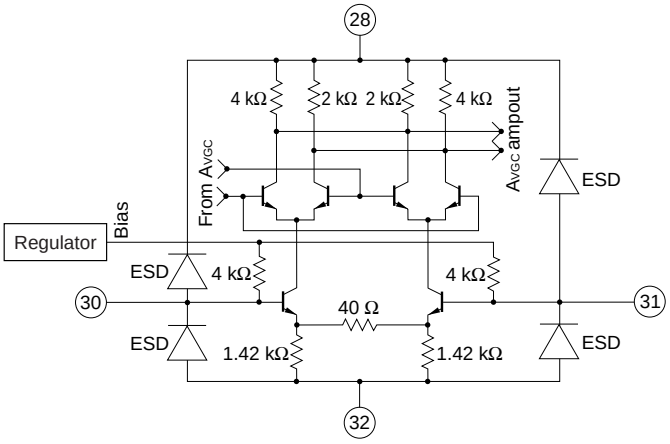


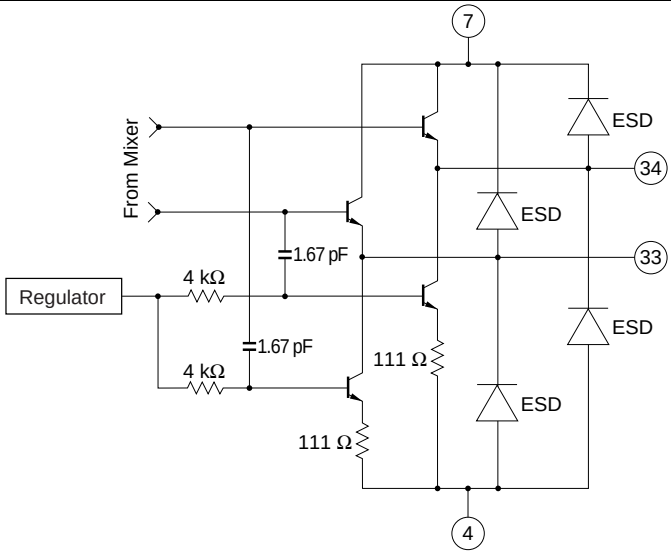
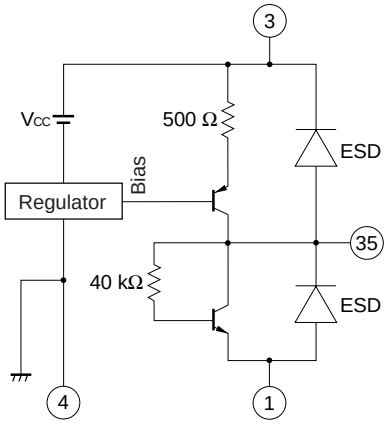
PIN EXPLANATION

Pin No.	Pin Name	Function and Application	Internal Equivalent Circuit
1	GND LNA	Ground pin of LNA.	
2	LNAin	Input pin of low noise amplifier. It is a single-ended open collector design. Capacitive coupling is required; external matching will improve gain or NF.	
3	V_{CCrf}	Supply voltage pin of LNA, RF mixer and VCO voltage regulator.	
4	GND_{LO}	Ground pin of 1stLO oscillator circuit and RF Mixer.	
5	1stLO-OSC1	Pin 5 & 6 are base pins of the differential amplifier for 1stLO oscillator. These pins requre an LC (varacator) tank circuit to oscilate at around 1 400 MHz.	
6	1stLO-OSC2		
7	V_{CCLO}	Supply voltage pin of oscillator circuit for 1stLO oscillator and RF mixer.	
8	PD_{out}	This is a cirrent mode charge pump output. For connection to a passive RC loop filter for driving external varactor diode of 1stLO oscillator.	
9	V_{CCdig}	Supply voltage pin of digital portion of the chip.	

Pin No.	Pin Name	Function and Application	Internal Equivalent Circuit
10	REFin	Input pin of reference frequency buffer. This pin should be equipped with external 27 MHz oscillator (e.g. TCXO).	
11	GNDdig	Ground pin of digital portion of the chip.	
12	IQ cntl	The voltage on this pin controls the Q channel IF amplifier gain control of ±2 dB can be achieved for 0 to 3 V. Leave open-circuited if not used.	
13	PD1	Standby mode control. Low = whole chip OFF & High = Whole chip ON.	

Pin No.	Pin Name	Function and Application	Internal Equivalent Circuit
14	2ndIFout-Q	Differential output pins of quadrature demodulator Q output. Adding a lowpass shunt capacitor between these pins will define the IF bandwidth.	
15	2ndIFout-Qb		
16	DCoffsetQ	DC offset compensation pin for C arm. A low pass capacitor shunt to pin 17 is required.	
17	DCoffsetQb	DC offset compensation pin for Q-bar arm. A low pass capacitor shunt to pin 16 is required.	
18	GNDbb	Ground pin of CMOS output driver.	
19	Qmag	Digitizd Q signal. Magnitude bit of 2-bit ADC output.	
20	Qsign	Digitizd Q signal. Sign bit of 2-bit ADC output.	
21	Isign	Digitizd I signal. Magnitude bit of 2-bit ADC output.	
22	Imag	Digitizd I signal. Magnitude bit of 2-bit ADC output.	
23	V_{CCbb}	Supply voltage pin of CMOS output driver.	

Pin No.	Pin Name	Function and Application	Internal Equivalent Circuit
24	DCoffsetIb	DC offset compensation pin for I-bar arm. A low pass capacitor shunt to pin 25 is required.	See pin 16 & 17 schematic
25	DCoffsetI	DC offset compensation pin for I-bar arm. A low pass capacitor shunt to pin 24 is required.	
26	2ndIFout-Ib	Differential output pins of quadrature demodulator I output. Adding a lowpass shunt capacitor between these pins will define the IF bandwidth.	See pin 14 & 15 schematic
27	2ndIFout-I		
28	$V_{CCanalog}$	Supply voltage pin of analog portion of the chip.	
29	V_{AGC}	Gain control voltage pin of IF amplifier. This voltage performs reverse control, (i.e., V_{AGC} up → gain down). If this pin is left open, then it is default at maximum gain.	
30	IF-in1	Differential input pins of 1stIF AGC amplifier.	
31	IF-in2		
32	GND_{analog}	Ground pin of analog portion of the chip.	

Pin No.	Pin Name	Function and Application	Internal Equivalent Circuit
33	Mixout2	Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50 Ω output load.	
34	Mixout1		
35	V_{REF}	Base-emitter junction voltage with respect to ground. May be used for biasing an external discrete transistor. PTAT current.	
36	LNAbias	LNA output pin. External bias (V_{CC}) and matching for gain is required.	See pin 2 schematic

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Ratings	Unit
Supply Voltage	V_{CC}	T_A = +25°C	3.6	V
Total Circuit Current	$I_{CCTotal}$	T_A = +25°C	100	mA
Power Dissipation	P_D	T_A = +25°C **Note**	361	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C

Note Mounted on double-sided copper-clad 50 × 50 × 1.6 mm epoxy glass PWB

RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.3	V
Operating Ambient Temperature	T_A	–40	+25	+85	°C
RF Input Frequency	f_{RFin}	–	1 575.42	–	MHz
1st LO Oscillating Frequency	$f_{1stLOin}$	–	1 400.256	–	MHz
1st IF Input Frequency	$f_{1stIFin}$	–	175.164	–	MHz
2nd LO Input Frequency	$f_{2ndLOin}$	–	175.032	–	MHz
2nd IF Input Frequency	$f_{2ndIFin}$ $f_{2ndIFout}$	–	132	–	kHz
Reference Input Frequency	f_{REFin}	–	27.456	–	MHz

POWER DOWN CONTROL (PIN 13) VOLTAGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Down Voltage (Low Level)	V_{IL}	0	–	0.5	V
Power Down Voltage (High Level)	V_{IH}	2.0	–	V_{CC}	V

AGC CONTROL VOLTAGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
AGC Control Voltage	V_{AGC}	0.5	–	2.5	V

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.0 V)

CIRCUIT CURRENT

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Total Circuit Current	$I_{CCTotal}$	No signal	14.0	18.0	23.5	mA
Power-save Dark Current	I_{CC} (PD)	Pin 13 = 0 V	–	1	–	μA
Reference Block Circuit Current (Pin 3)	I_{CC} (rf)	No signal	0.4	0.5	0.7	mA
VCO Block Circuit Current (Pin 7)	I_{CC} (lo)	No signal	4.1	5.6	7.2	mA
PLL Block Circuit Current (Pin 9)	I_{CC} (pll)	No signal	2.7	3.6	4.7	mA
Baseband Block Circuit Current (Pin 23)	I_{CC} (bb)	No signal, open load	2.5	3.4	4.3	mA
IF Block Circuit Curent (Pin 28)	I_{CC} (if)	No signal	2.7	3.7	4.7	mA
Pre-Amplifier Open Connector Current (Pin 36)	I_{CC} (lna)	No signal	1.0	1.4	1.8	mA

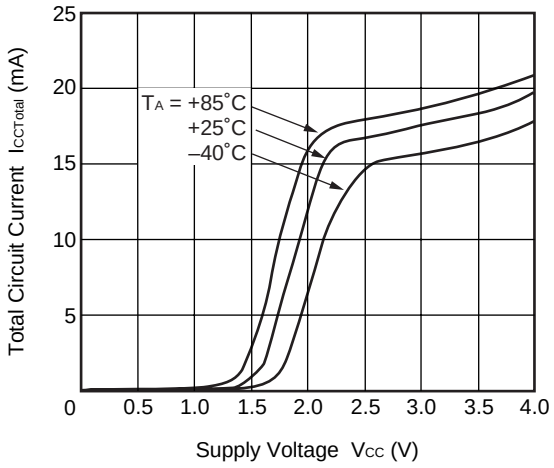
AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
RF Block (LNA, RFmixer) f_{RFin} = 1 575.42 MHz, $f_{1stLOin}$ = 1 400.256 MHz, P_{LO} = 0 dBm, f_{1stIF} = 175.164 MHz, P_{in15} = 3 V, Z_L = Z_{in} = 50 Ω						
Power conversion gain	$CG_{LNA-MIX}$	P_{RFin} = –60 dBm	18	23	28	dB
Noise Figure	$NF_{LNA-MIX}$	Input matched, DSB	–	5	–	dB
Input 1dB Compression Level	$P_{in\ (1dB)\ LNA-MIX}$	Input matched	–	–38	–	dBm
Local Signal Leak to IF	A_{LO-IF}		–	–35	–	dBm
Local Signal Leak to RF	A_{LO-RF}		–	–50	–	dBm
IF Block (AGC, IQ Mix, IFamp, ADC) $f_{1stIFin}$ = 175.164 MHz, $f_{2ndLOin}$ = 175.032 MHz, $f_{2ndIFout}$ = 132 kHz, Z_L = 2 kΩ, Z_{in} = 600 Ω						
I ch Magbit Output Pluse Duty	Duty-I ch	$P_{1stIFin}$ = –80 dBm, V_{AGC} = 0.5 V, V_{IQ-C} = 0 V	50	70	–	%
Q ch Magbit Output Pluse Duty	Duty-Q ch	$P_{2ndIFin}$ = –80 dBm, V_{AGC} = 0.5 V, V_{IQ-C} = 2.1 V	50	70	–	%
Input 1dB Compression Level	$P_{in\ (1dB)\ AGC}$	AGCamp + IQ MIX	–	–45	–	dBm
AGC Control range	A_{AGC}		25	45	–	dB
2ndLO Isoration (1stIFin)	$A_{2ndLO-1stIF}$	V_{AGC} = 0 V	–	–90	–	dB
IQ Balance Control Voltage	V_{IQ-C}	I_{ch} = Q_{ch}	–	2.1	2.8	V
IQ Balance Control Gain Range	A_{IQ-C}	Magbit Output Pulse Duty Cycle 50% (Q_{ch})	4.0	6.5	–	dB
PLL						
PLL Charge Pump High Side Current	I_{CPOH}	V_{CPout} = V_{CC}/2	–	200	–	μA
PLL Charge Pump Low Side Current	I_{CPOL}	V_{CPout} = V_{CC}/2	–	–200	–	μA
Phase Comparision Frequency	f_{PD}		–	13.728	–	MHz
VCO, REF Amp						
Reference Input Minimum Level	V_{REFin}		50	200	–	mVpp
Input Frequency of Reference Input	f_{REFin}		–	27.456	–	MHz
VCO Control Voltage	VT	PLL Locked	0.8	1.5	2.2	V
VCO C/N	C/N	Δ1 kHz	57	62	–	dBc/Hz

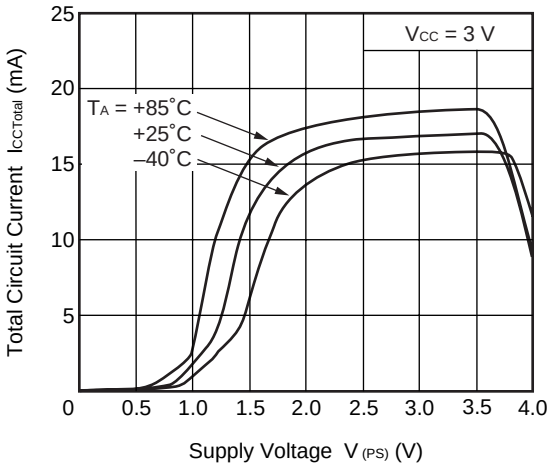
TYPICAL CHARACTERISTICS (Unless otherwise specified, T_A = +25°C, V_{CC} = 3.0 V)

— IC TOTAL —

TOTAL CIRCUIT CURRENT
vs. SUPPLY VOLTAGE



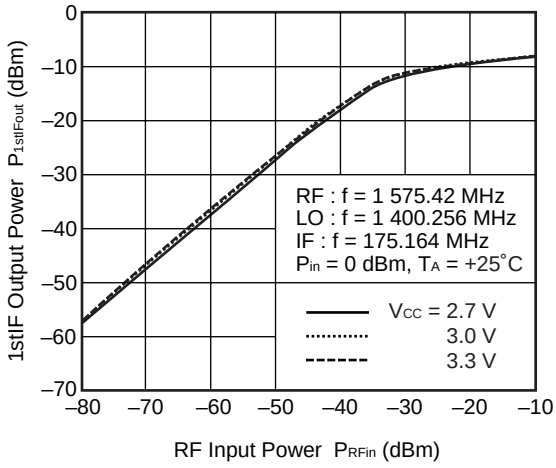
TOTAL CIRCUIT CURRENT vs. V (PS)



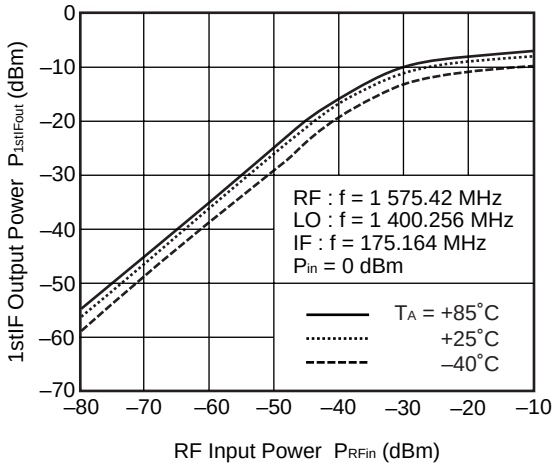
Remark The graphs indicate nominal characteristics.

— RF BLOCK (LNA + RF down converter) —

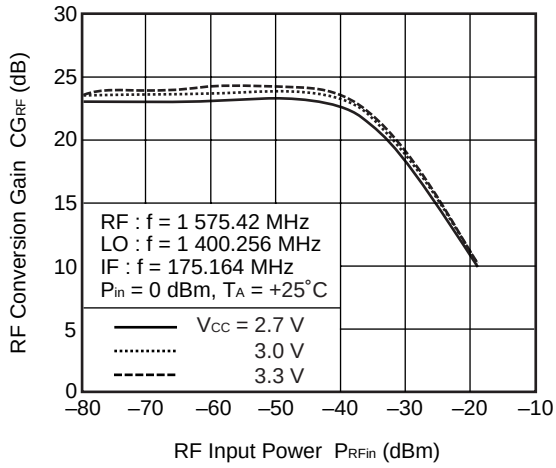
1stIF OUTPUT POWER
vs. RF INPUT POWER



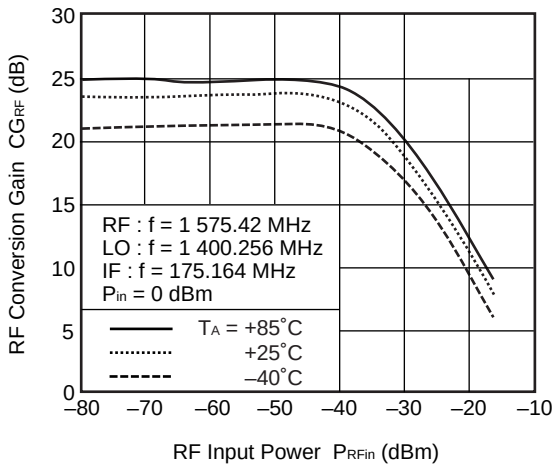
1stIF OUTPUT POWER
vs. RF INPUT POWER



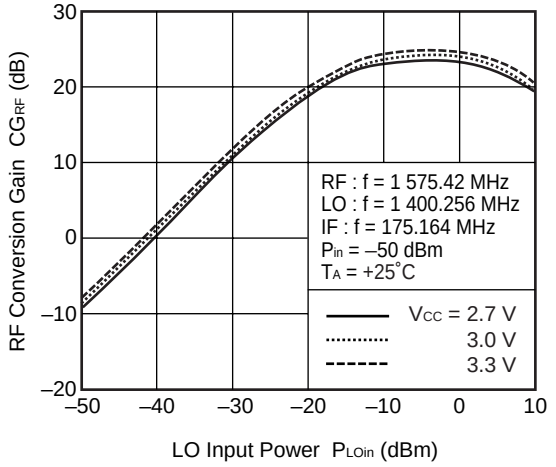
RF CONVERSION GAIN
vs. RF INPUT POWER



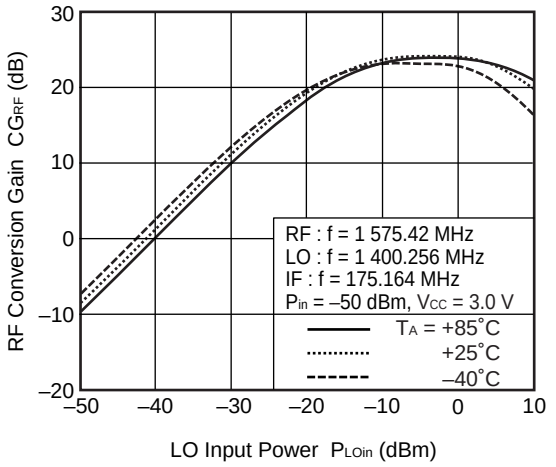
RF CONVERSION GAIN
vs. RF INPUT POWER



RF CONVERSION GAIN
vs. LO INPUT POWER

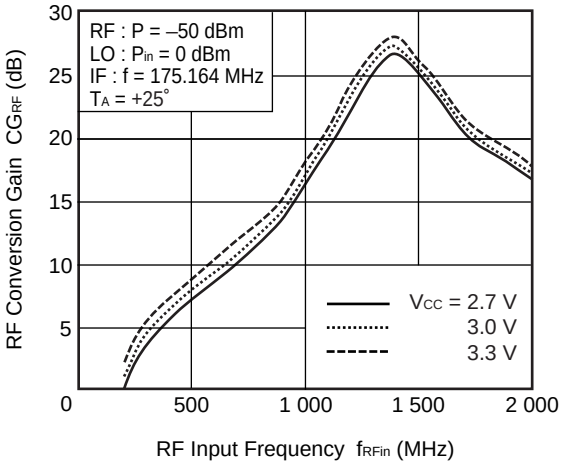


RF CONVERSION GAIN
vs. LO INPUT POWER

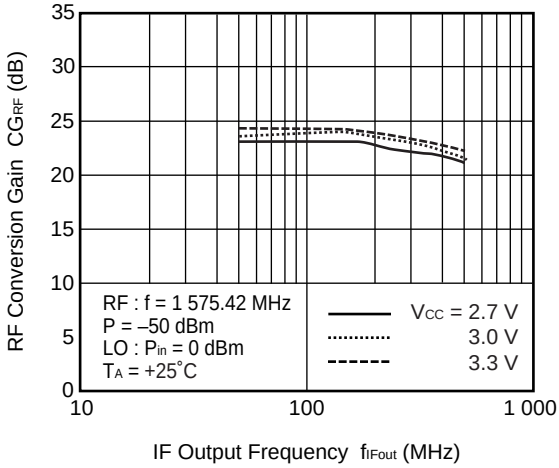


Remark The graphs indicate nominal characteristics.

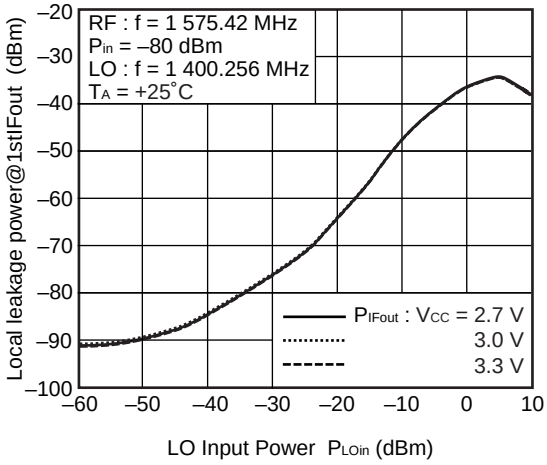
RF CONVERSION GAIN
vs. RF INPUT FREQUENCY



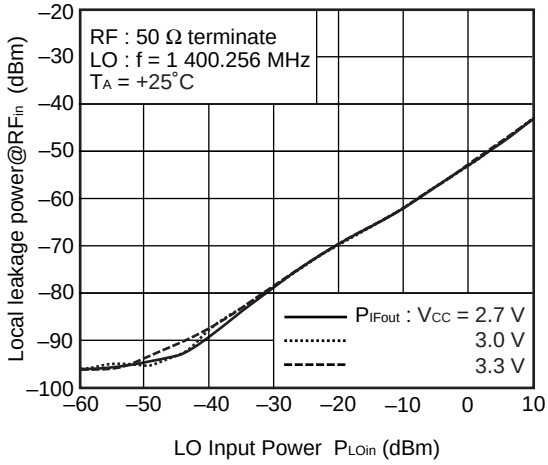
RF CONVERSION GAIN
vs. IF OUTPUT FREQUENCY



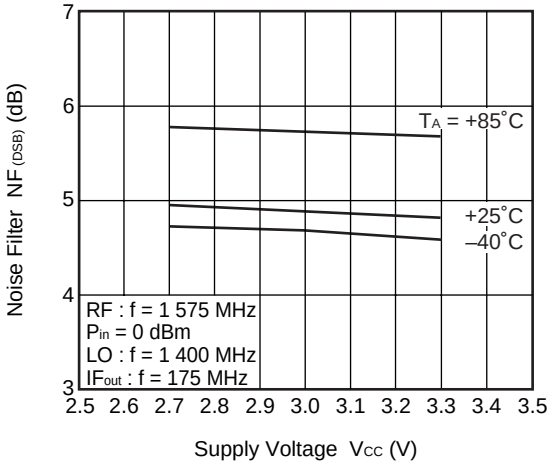
LOCAL LEAKAGE POWER@1stIFout
vs. LO INPUT POWER



LOCAL LEAKAGE POWER@RFin
vs. LO INPUT POWER



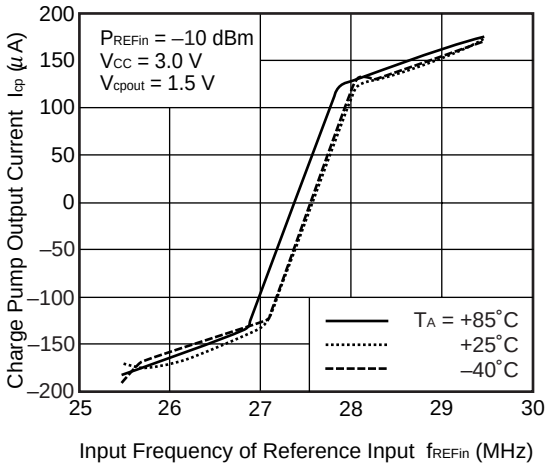
NOISE FILTER vs. SUPPLY VOLTAGE



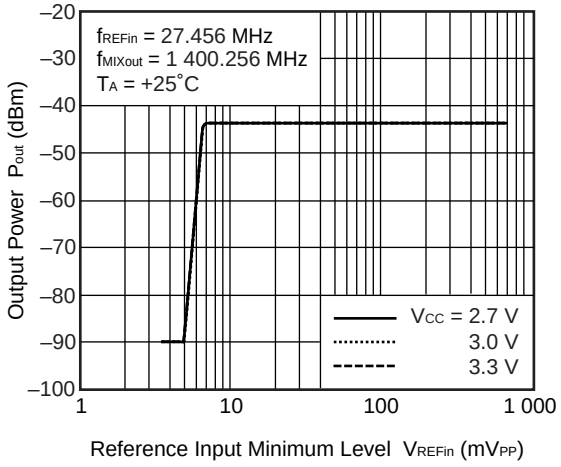
Remark The graphs indicate nominal characteristics.

— RF BLOCK (PLL/REF) —

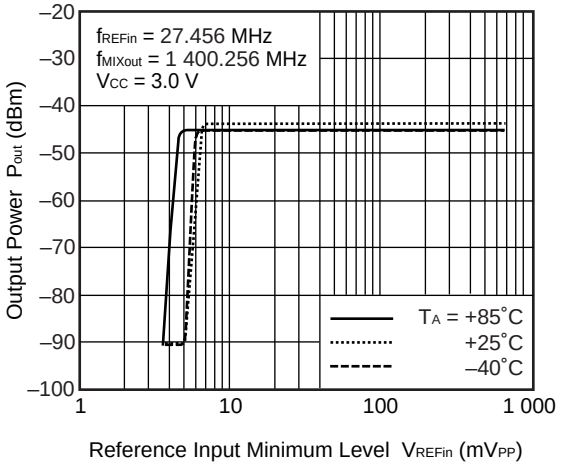
CHARGE PUMP OUTPUT CURRENT
vs. REFERENCE FREQUENCY



OUTPUT POWER
vs. REFERENCE INPUT MINIMUM LEVEL



OUTPUT POWER
vs. REFERENCE INPUT MINIMUM LEVEL

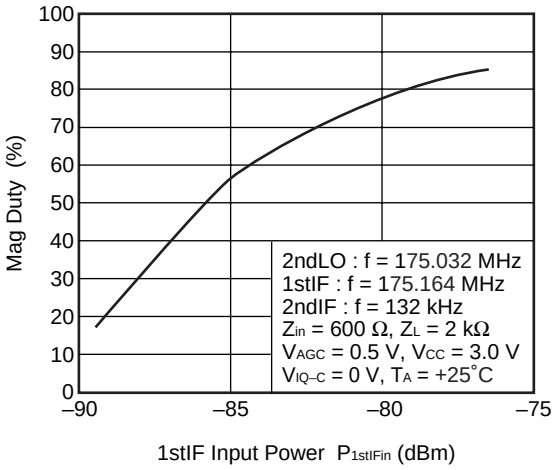


Remark The graphs indicate nominal characteristics.

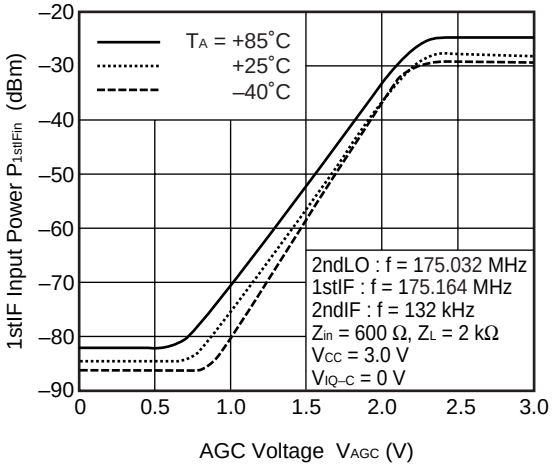
— IF BLOCK (AGCamp + IF MIX + IFamp + ADC) —

I CH

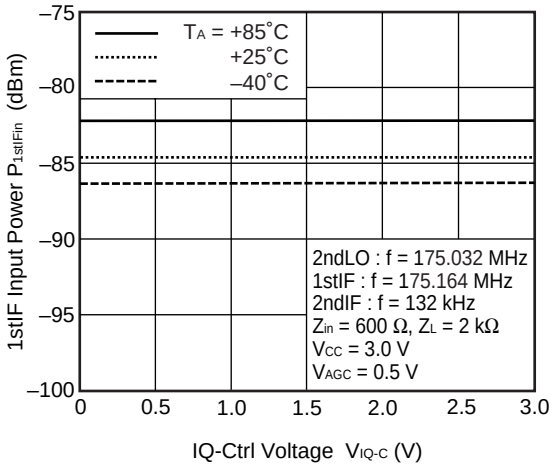
MAG DUTY vs. 1stIF INPUT POWER



P1stIFin (MAG DUTY 50%) vs. AGC VOLTAGE

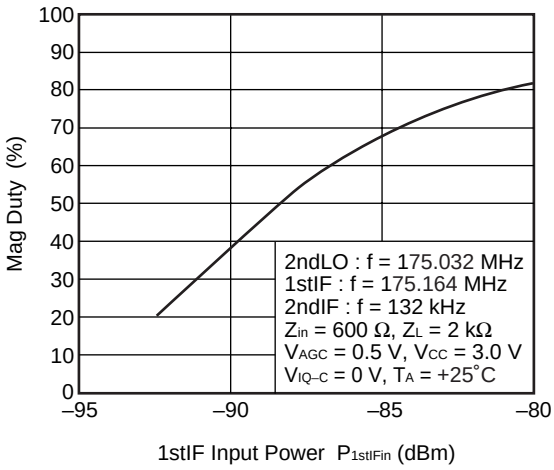


P1stIFin (MAG DUTY 50%) vs. IQ-CTRL VOLTAGE

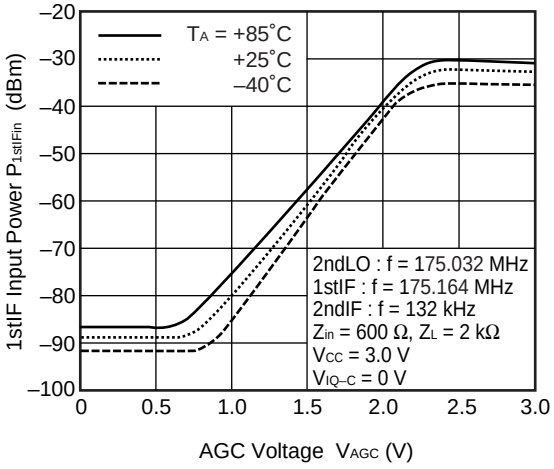


Q CH

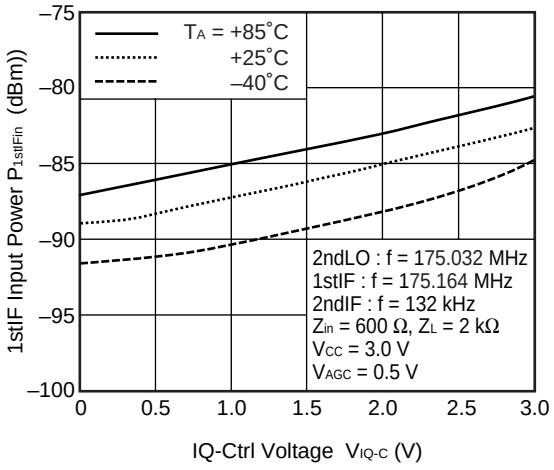
MAG DUTY vs. 1stIF INPUT POWER



P1stIFin (MAG DUTY 50%) vs. AGC VOLTAGE



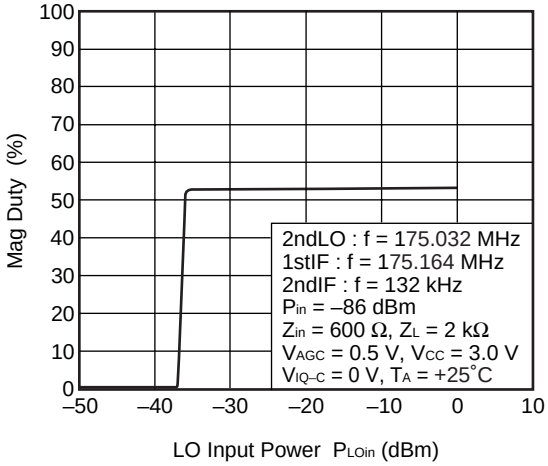
P1stIFin (MAG DUTY 50%) vs. IQ-CTRL VOLTAGE



Remark The graphs indicate nominal characteristics.

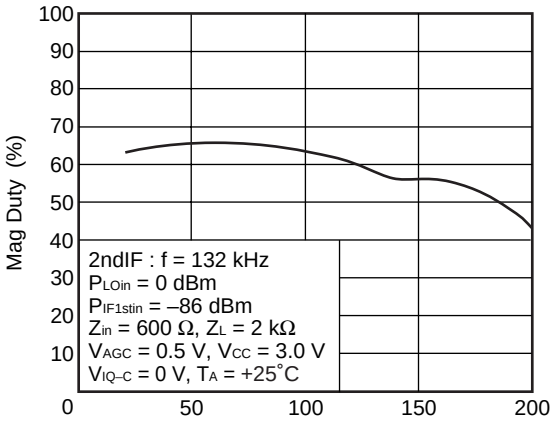
I CH

MAG DUTY vs. LO INPUT POWER



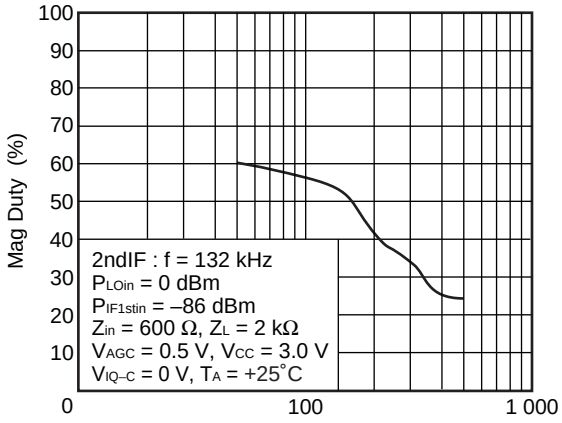
LO Input Power P_{LOin} (dBm)

MAG DUTY vs. 1stIF INPUT FREQUENCY



1stIF Input Frequency $f_{1stIFin}$ (MHz)

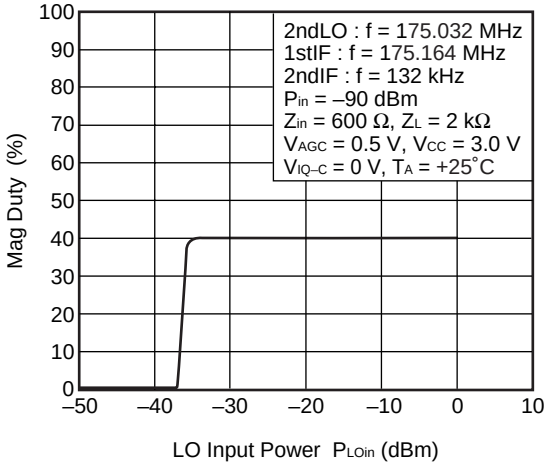
MAG DUTY vs. 2ndIF OUTPUT FREQUENCY



2ndIF Output Frequency $f_{2ndIFout}$ (MHz)

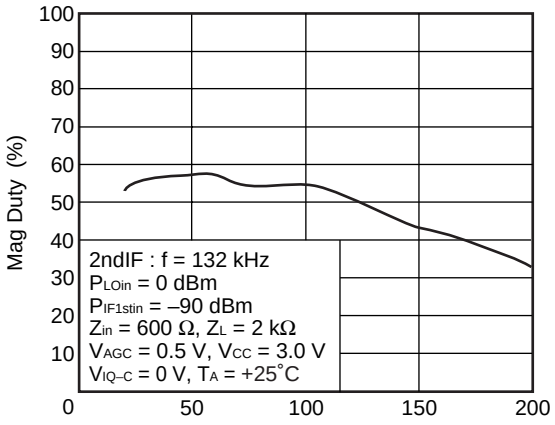
Q CH

MAG DUTY vs. LO INPUT POWER



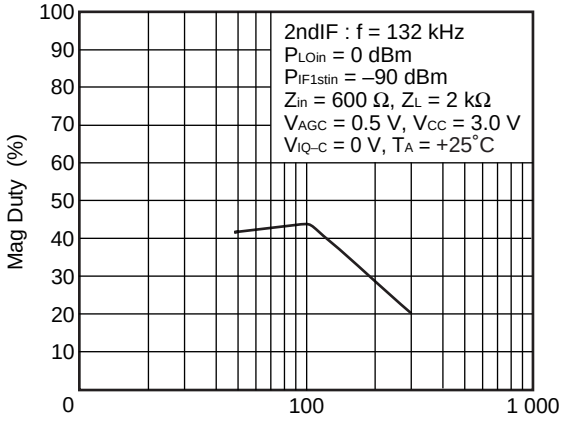
LO Input Power P_{LOin} (dBm)

MAG DUTY vs. 1stIF INPUT FREQUENCY



1stIF Input Frequency $f_{1stIFin}$ (MHz)

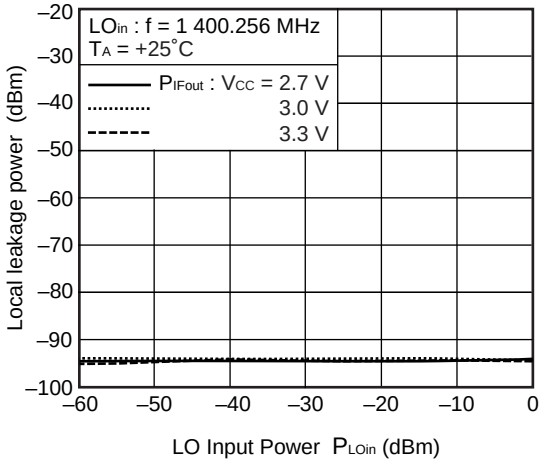
MAG DUTY vs. 2ndIF OUTPUT FREQUENCY



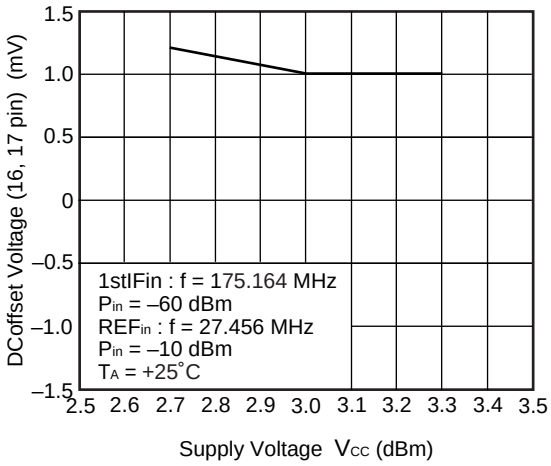
2ndIF Output Frequency $f_{2ndIFout}$ (MHz)

Remark The graphs indicate nominal characteristics.

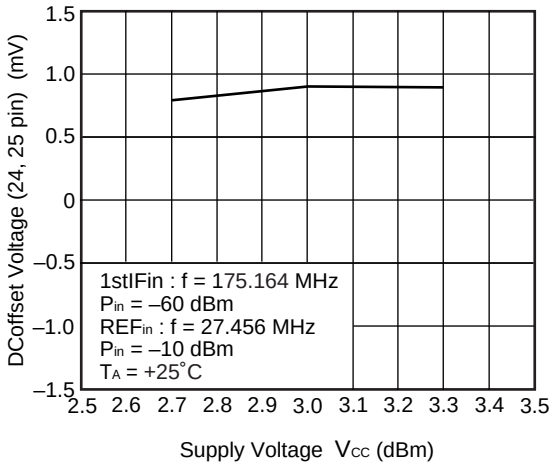
LOCAL LEAKAGE POWER vs. LO INPUT POWER



DCOFFSET VOLTAGE (16, 17 pin) vs. SUPPLY VOLTAGE



DCOFFSET VOLTAGE (24, 25 pin) vs. SUPPLY VOLTAGE

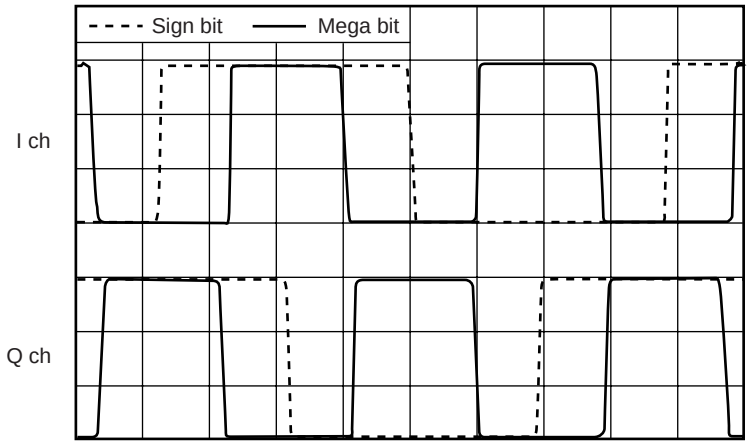


Remark The graphs indicate nominal characteristics.

— IF BLOCK (ADC) —

ADC OUTPUT WAVE FORM

(2ndIFin : f = 132 kHz, $P_{in\ (I\ ch)}$ = –45 dBm, $P_{in\ (Q\ ch)}$ = 49 dBm, V_{CC} = 3.0 V, T_A = +25°C)

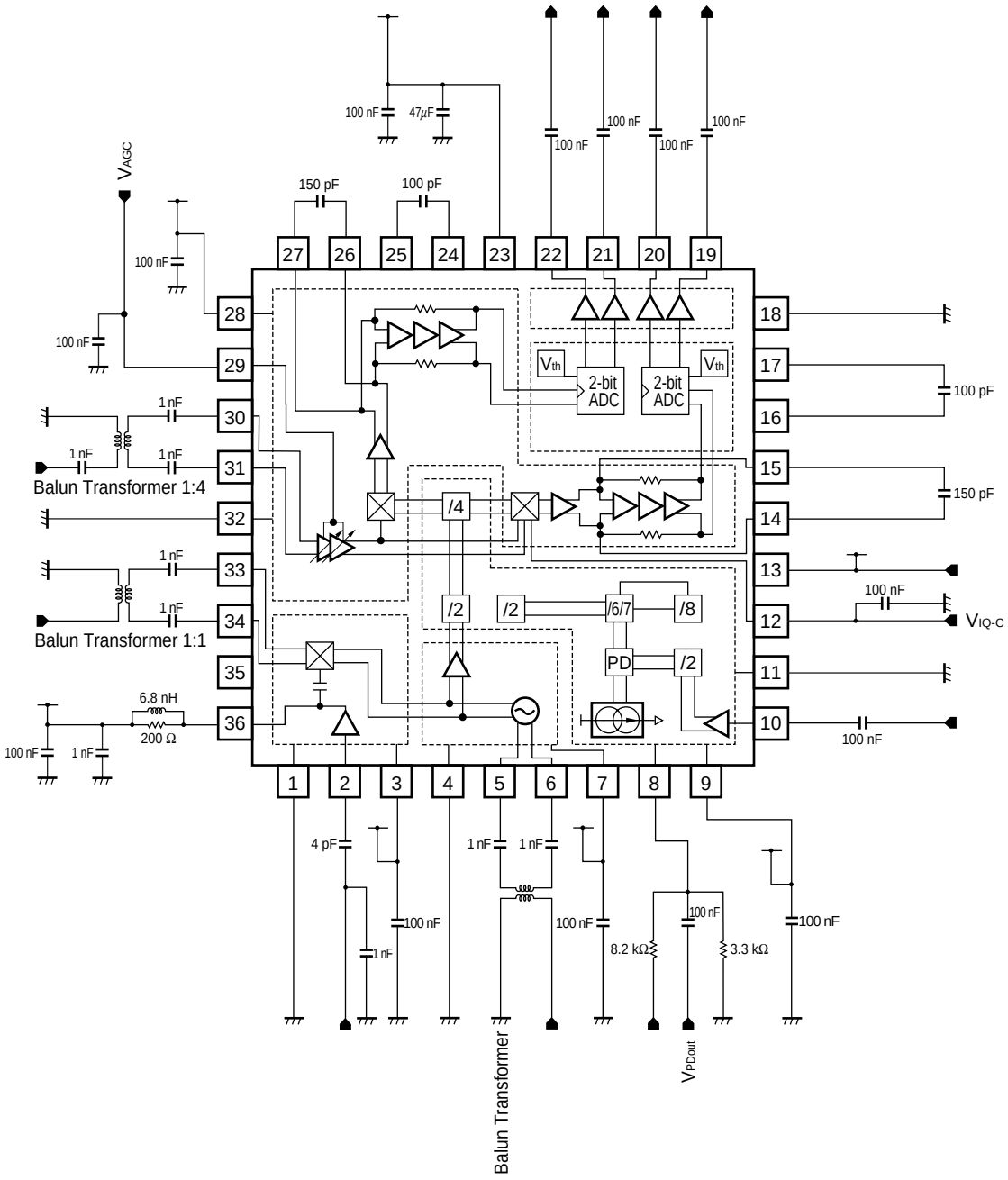


Remark The graphs indicate nominal characteristics.

MEASUREMENT CIRCUIT

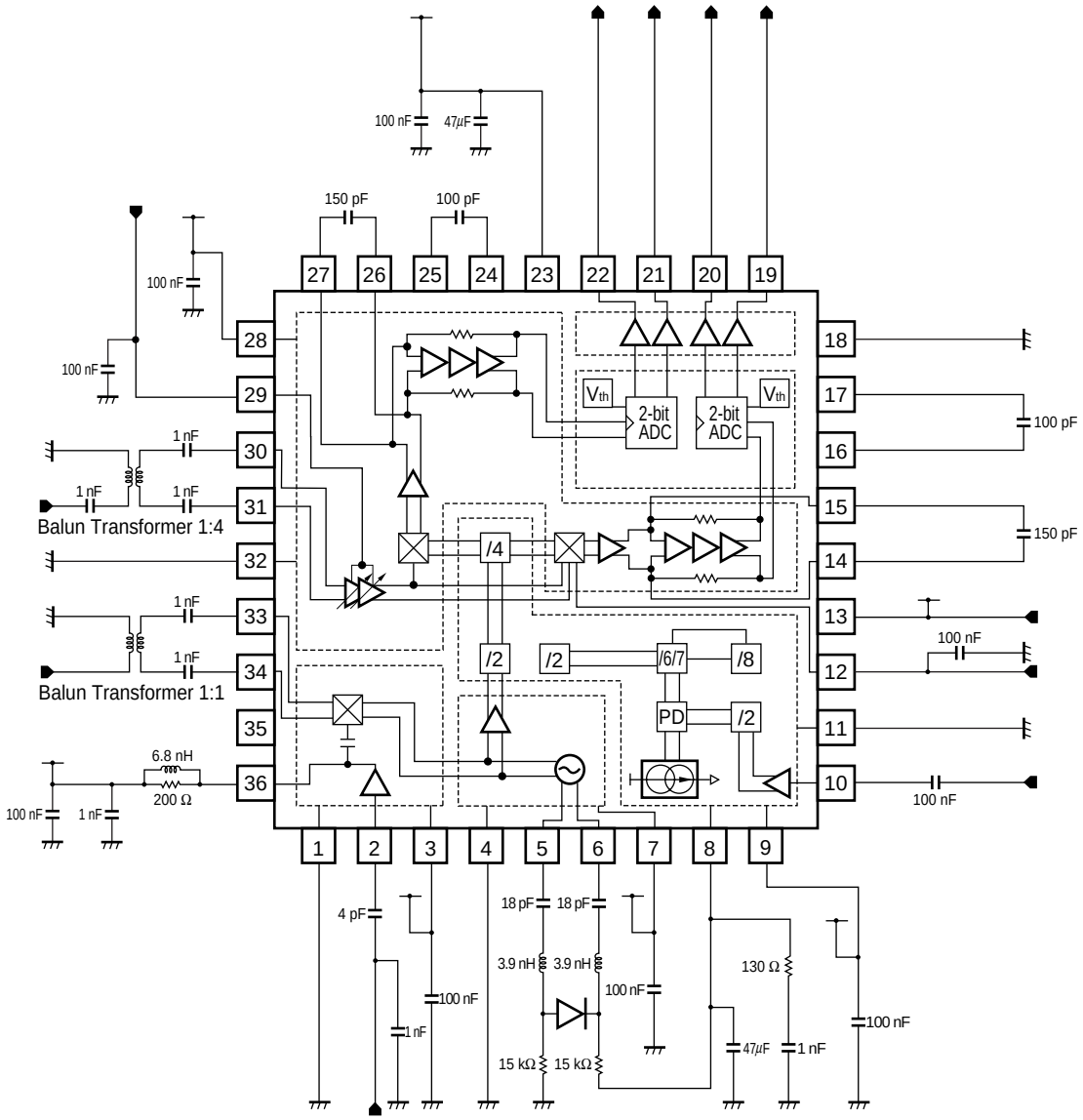
MEASUREMENT CIRCUIT 1

RF BLOCK (LNA + RF MIX) / IF BLOCK (AGCamp + IF MIX + IFamp + ADC)



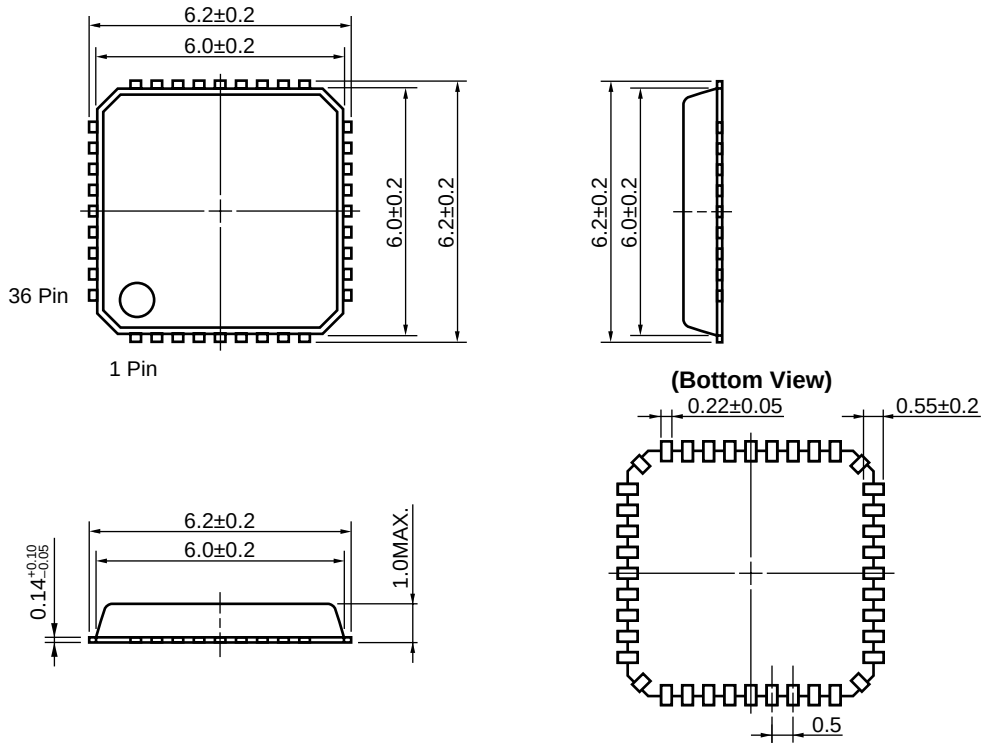
MEASUREMENT CIRCUIT 2

PLL LOCK TYPE (C/N, VT)



PACKAGE DIMENSIONS

36-PIN PLASTIC QFN (UNIT: mm)



Caution The island pins located on the corners are needed to fabricate products in our plant, but do not serve any other function. Consequently the island pins should not be soldered and should remain non-connection pins.

NOTES ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent abnormal oscillation).
(3) Keep the wiring length of the ground pins as short as possible.
(4) Connect a bypass capacitor to the V_{CC} pin.
(5) High-frequency signal I/O pins must be coupled with the external circuit using a coupling capacitor.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2%(Wt.) or below	IR260
VPS	Peak temperature (package surface temperature) Time at temperature of 200°C or higher Preheating time at 120 to 150°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 215°C or below : 25 to 40 seconds : 30 to 60 seconds : 3 times : 0.2%(Wt.) or below	VP215
Wave Soldering	Peak temperature (molten solder temperature) Time at peak temperature Preheating temperature (package surface temperature) Maximum number of flow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 120°C or below : 1 time : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (pin temperature) Soldering time (per side of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2%(Wt.) or below	HS350

Caution Do not use different soldering methods together (except for partial heating).

- **The information in this document is current as of November, 2003. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
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  - "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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M8E 00.4-0110

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