DATA SHEET



BIPOLAR ANALOG INTEGRATED CIRCUIT $\mu PC667$

10-BIT D/A CONVERTER

The μ PC667 is high-speed and high-precision 10-bit D/A converter. Clock rate of the μ PC667 is 60 Msps. Conversion precision of the μ PC667 is ±1.0 LSB.

FEATURES

Resolution 10-bit
 Clock rate 60 Msps
 Technology Bi-CMOS
 Power supply +5 V

D/A conversion method
 R-2R ladder resistance and segment summing system

Analog output form
 Voltage output type

· Built-in reference voltage generating circuit

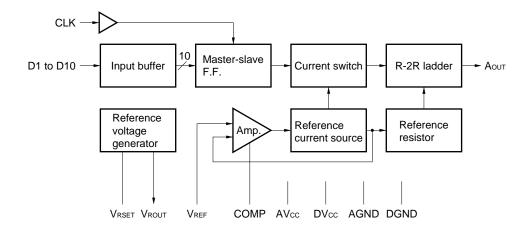
ORDERING INFORMATION

Part Number	Package
μPC667CT	30-pin plastic shrink DIP (400 mil)

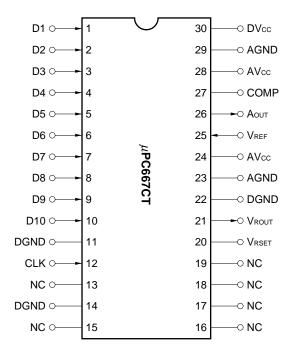
The information in this document is subject to change without notice.



BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



AGND : Ground for Analog Circuit

AOUT : Analog Output

AVcc : Power Supply for Analog Circuit

CLK : Clock

COMP : Phase Compensation

D1 to D10: Digital Signal

DGND : Ground for Digital CircuitDVcc : Power Supply for Digital Circuit

NC : No Connection
VREF : Reference Voltage

VROUT : Reference Voltage Output
VRSET : Reference Voltage Adjustment



PIN FUNCTIONS

Pin Name	Pin No.	Input/ Output	Function	Equivalent Circuit
D1 to D10	1 to 10	Input	Digital signal D1 is MSB, D10 is LSB.	DVcc DVcc DVcc DVcc DVcc DVcc DVcc DVcc
CLK	12	Input	Clock The rising edge of signal input to this pin triggers analog output.	DVcc DVcc 500 Ω T DGND DVcc DV
DVcc	30	_	Power supply for digital circuit	DVcc
DGND	11, 14, 22	_	Ground for digital circuit	O DGND
VRSET	20	_	Reference voltage adjustment Voltage adjusting pin for the incorporated reference voltage generating circuit. The output voltage of VROUT pin varies according to the voltage applied to this pin. When no adjustment is necessary, connect approx. 0.1 µF capacitance between this pin and GND pin.	AVcc AVcc $7.5 \text{ k}\Omega$ AVcc $2 \text{ k}\Omega$ $0.5 \text{ k}\Omega$ AVcc $0.5 \text{ k}\Omega$ AVcc $0.5 \text{ k}\Omega$ AVcc $0.5 \text{ k}\Omega$ AVcc $0.5 \text{ k}\Omega$
VROUT	21	Output	Reference voltage output Voltage output pin of the incorporated reference voltage generating circuit. This pin has high output impedance, and must be connected with a high impedance element.	Reference 7777 AGND voltage generator



Pin Name	Pin No.	Input/ Output	Function	Equivalent Circuit
VREF	25	Input	Reference voltage The output full-scale range is set according to the voltage applied to this pin. Apply standard 4.0 V. When no adjustment is necessary, connect the output from VROUT pin directly to this pin.	AVcc 5 kΩ AGND AGND AGND
Аоит	26	Output	Analog signal Analog signal output pin.	AVcc $AVcc$ AV
COMP	27	_	Phase compensation Phase compensating capacitor connection pin for full-scale amplifier. Approx. 0.1 μ F capacitor must be connected between this pin and AVcc pin.	AVcc AVcc AVcc AVcc AVcc AVcc AVcc AVcc
AVcc	24, 28	_	Power supply for analog circuit	AVcc
AGND	23, 29	_	Ground for analog circuit	O—————————————————————————————————————
NC	13, 15 to 19	_	No Connection	O



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Ratings	Unit
Supply voltage for digital circuit	DVcc	-0.3 to +6.0	V
Input voltage	Vı	-0.3 to Vcc +0.3	V
Operating ambient temperature	TA	-20 to +70	°C
Storage temperature	T _{stg}	-40 to +125	°C
Power dissipation	Po	0.8 (T _A = +60 °C)	W
Supply voltage for analog circuit	AVcc	DVcc -0.3 to DVcc +0.3	V

★ Caution Exposure to Absolute Maximum Rating for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage for digital circuit	DVcc		4.75	5.0	5.25	V
Supply voltage for analog circuit	AVcc		4.75	5.0	5.25	V
Reference voltage input pin voltage	VREF		3.8	4.0	4.2	V
High-level voltage of digital input	Vıн		2.0			V
Low-level voltage of digital input	VIL				0.8	V
Conversion clock frequency	fcLK				60	MHz
Phase compensation capacitance	Ссомр			1.0		μF



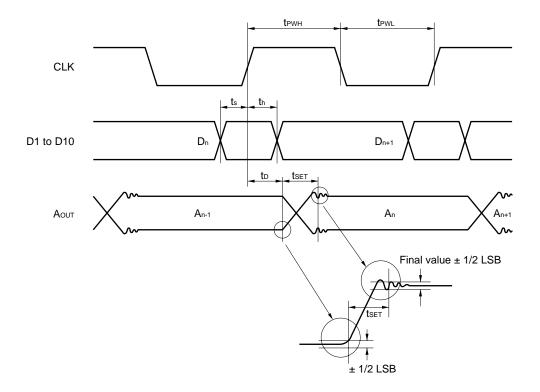
DC Characteristics and AC Characteristics ($T_A = -10 \text{ to } +70 ^{\circ}\text{C}$, $DVcc = AVcc = +5 \pm 0.25 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RSL			10		Bit
Integral linearity error	ILE	$T_A = 0$ to 60 °C, $V_{REF} = 4.0 \text{ V}$	-1.0		+1.0	LSB
Differential linearity error	DLE	$T_A = 0$ to 60 °C, $V_{REF} = 4.0 \text{ V}$	-1.0		+1.0	LSB
Supply current	Icc			50	71	mA
Set-up time	ts			3	7	ns
Hold time	t h			1.5	7	ns
Settling time	t set	$T_A = 25$ °C, $R_L = 375$ Ω , $V_{REF} = 4.0$ V		13		ns
Output delay time	t d	V _{REF} = 4.0 V		9	13	ns
Full-scale voltage output	Vofs	$V_{REF} = 4.0 \text{ V}, \text{ RL} > 100 \text{ k}\Omega$	4.95		5.0	V
Zero-scale voltage output	Vozs	$V_{REF} = 4.0 \text{ V}, \text{ RL} > 100 \text{ k}\Omega$	3.95	4	4.05	V
Output resistance	Zout	V _{REF} = 4.0 V	70	85	100	Ω
Internal reference voltage output voltage	VROUT	AVcc = 5.0 V	3.8	4.0	4.2	٧

- Cautions 1. As for the phase compensation capacitance, capacitor of 1 μ F should be connected between the phase compensation capacitance pin (COMP) and the power supply pin for analog circuit (AVcc).
 - 2. The internal reference voltage output pin (VROUT) and the reference voltage input pin (VREF) should be shorted.
 - 3. The power supply and GND lines for analog circuit (AVcc and AGND) and those for digital circuit (DVcc and DGND) should be located as separately as possible.

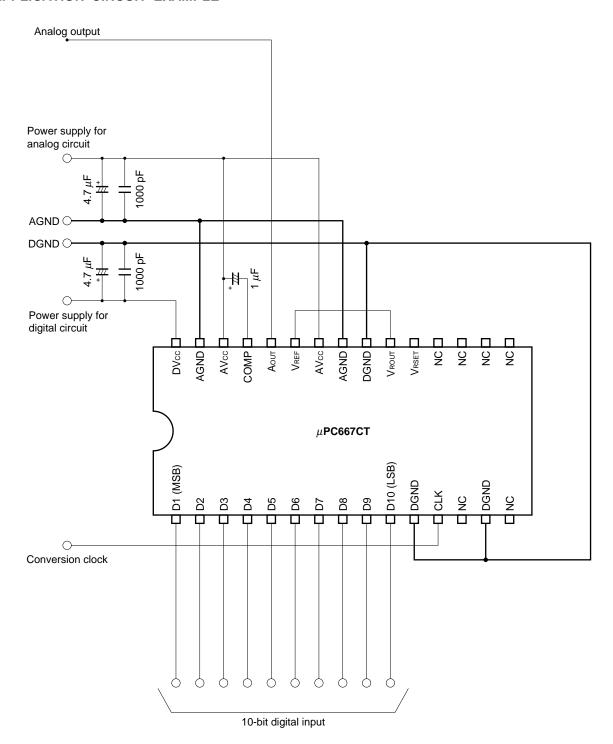


★ Timing Chart





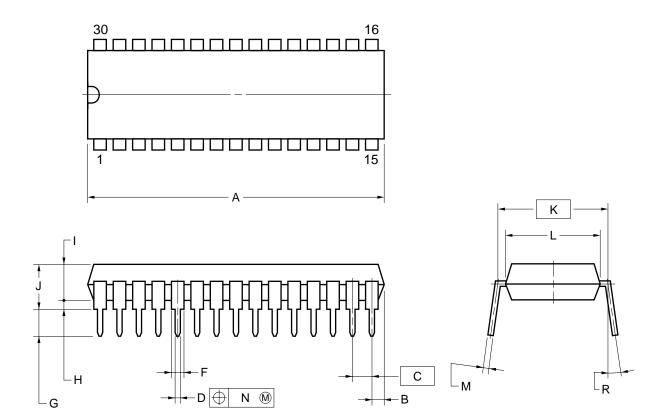
APPLICATION CIRCUIT EXAMPLE





PACKAGE DRAWING

30PIN PLASTIC SHRINK DIP (400 mil)



NOTES

- Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
Α	28.46 MAX.	1.121 MAX.
В	1.78 MAX.	0.070 MAX.
С	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	3.2±0.3	0.126±0.012
Н	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
М	0.25 ^{+0.10} -0.05	0.010+0.004
N	0.17	0.007
R	0~15°	0~15°

S30C-70-400B-1



RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Through-hole device

 μ PC667CT: 30-pin plastic Shrink DIP (400 mil)

Process	Conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial heating method	Terminal temperature: 300 °C or below, Heat time: 3 seconds or less (Per each lead).

Caution For through-hole devices, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

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[MEMO]

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

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Anti-radioactive design is not implemented in this product.

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