NEC

MOS INTEGRATED CIRCUIT
μPD16341

96-BIT AC-PDP DRIVER

★ DESCRIPTION

The μPD16341 is high withstand voltage CMOS driver designed for flat display panels such as PDPs, VFDs and ELs. It consists of a 96-bit bi-directional shift register, 96-bit latch and high withstand voltage CMOS driver. The logic block is designed to operate using a 5-V power supply interface enabling direct connection to a gate array or a microcontroller. In addition, the μPD16341 achieves low power dissipation by employing the CMOS structure while having a high withstand voltage output (120 V, +15/–25 mA MAX.).

FEATURES

- 2-/3-/4-/6-ch input port switching is possible using IBS1 and IBS2 pins
- Data control with transfer clock (external) and latch
- High-speed data transfer ($f_{MAX.}$ = 40 MHz MIN. at data latch)
  ($f_{MAX.}$ = 25 MHz MIN. at cascade connection)
- ★ High withstand output voltage: 120 V, +15/–25 mA MAX.
- 5-V CMOS input interface
- High withstand voltage CMOS structure

★ ORDERING INFORMATION

Part Number	Package
μPD16341	Module

Remark Consult an NEC sales representative regarding the module. Since the module characteristics is based on the module specifications, there may be differences between the contents written in this document and real characteristics.

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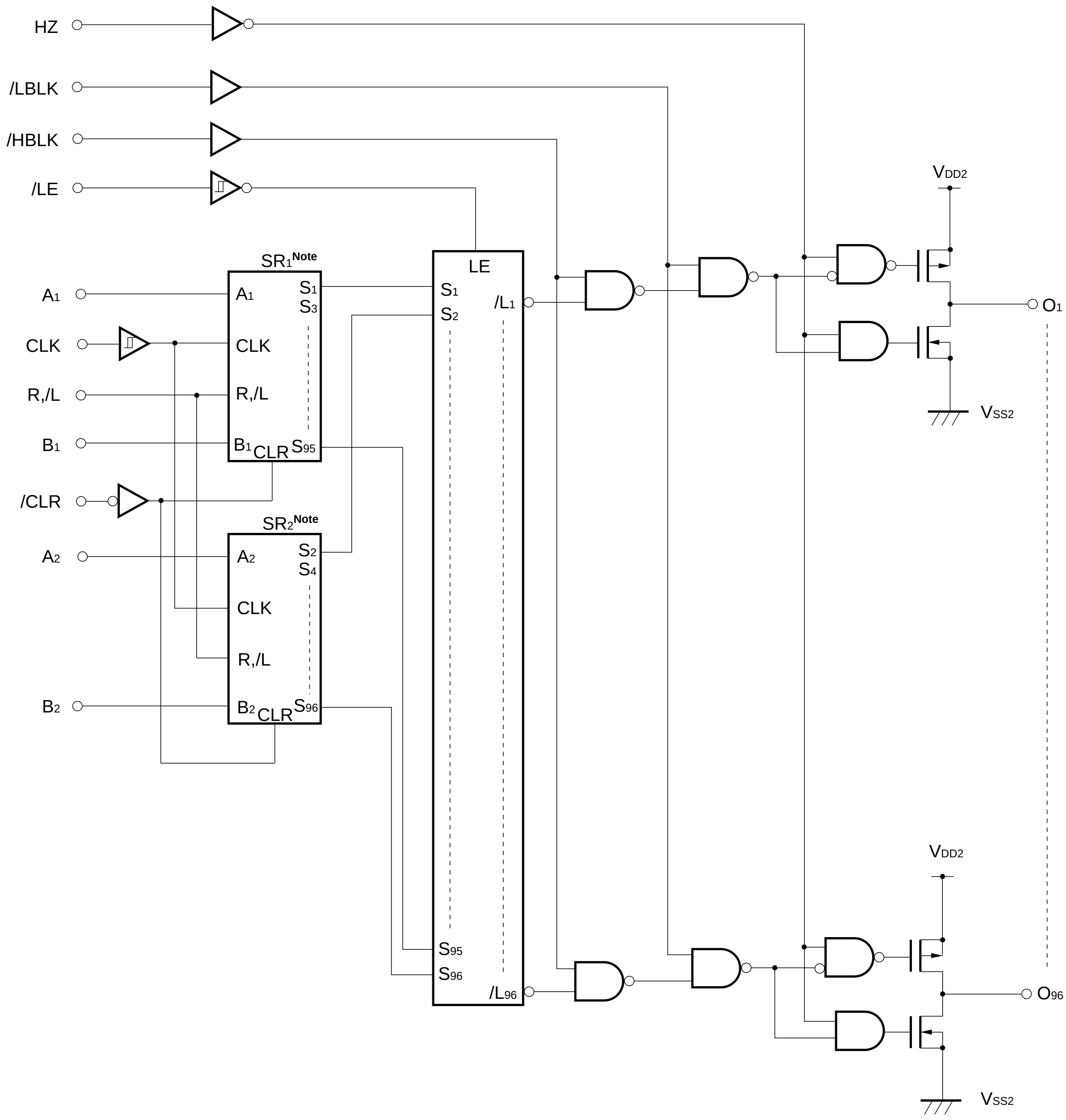
The mark ★ shows major revised points.

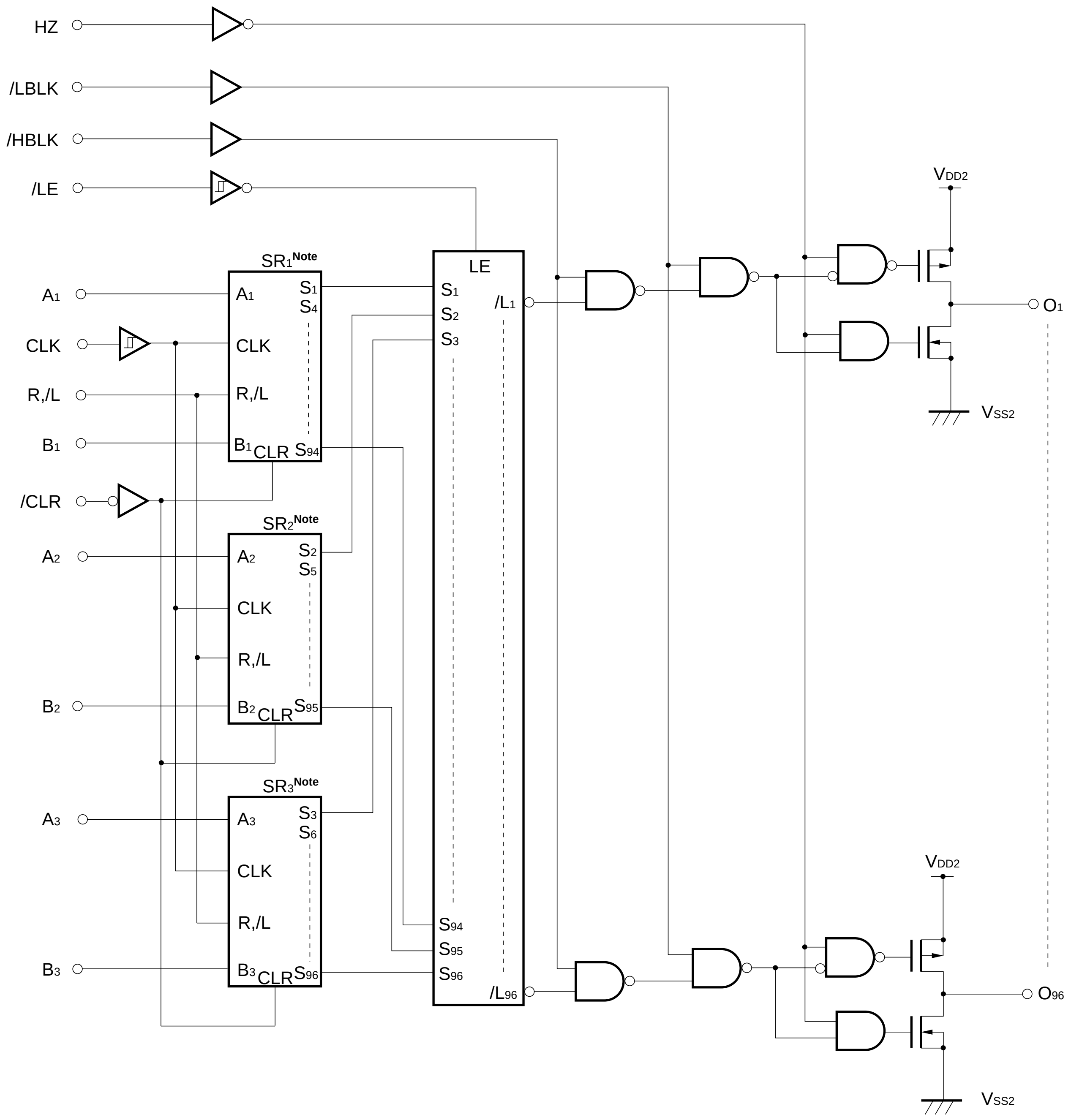
1. BLOCK DIAGRAM (1) (IBS1 = H, IBS2 = H, 2-BIT INPUT, 48-BIT LENGTH SHIFT REGISTER)



Note SRn: 48-bit shift register

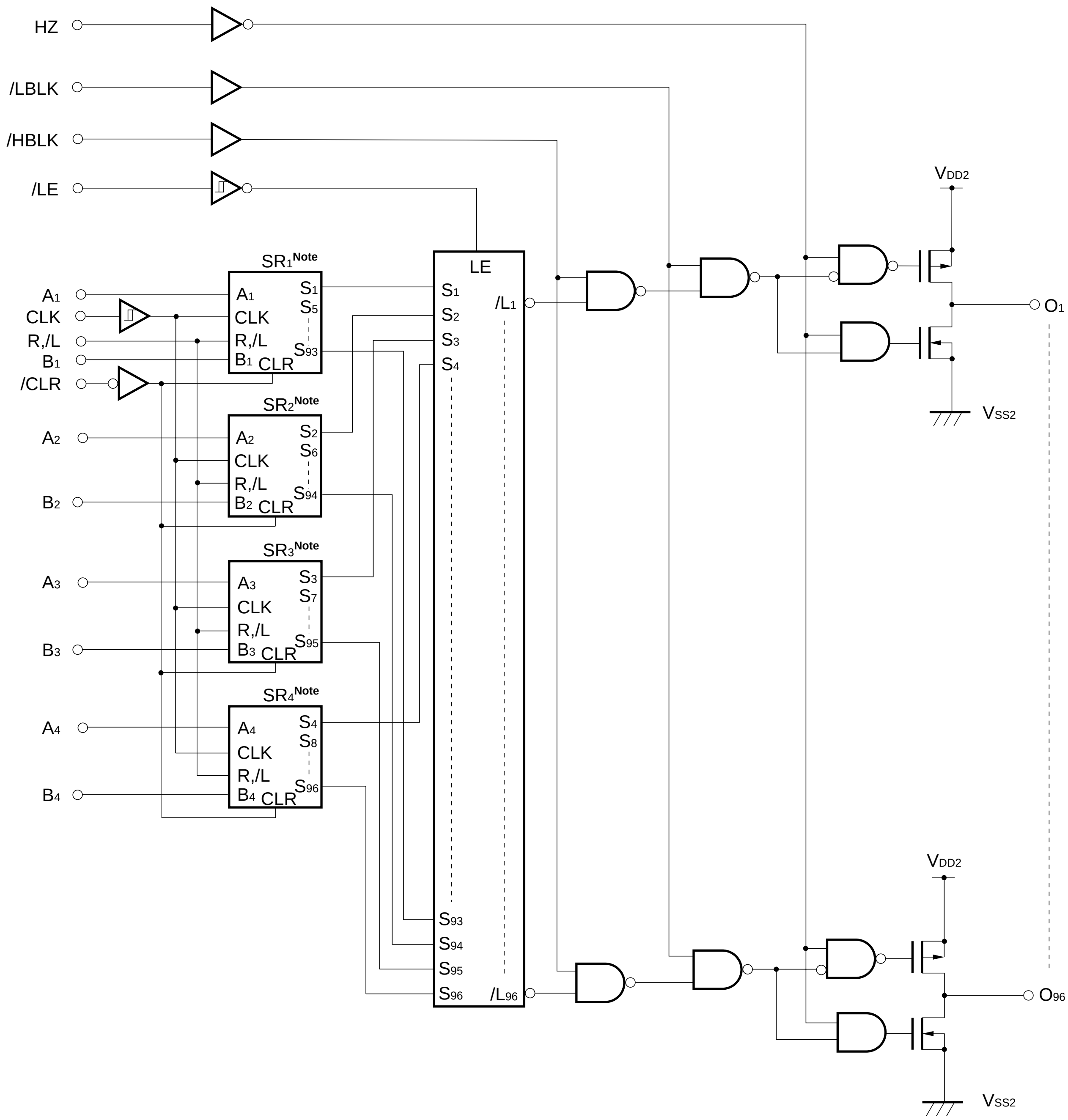
Remark /xxx indicates active low signal.

1. BLOCK DIAGRAM (2) (IBS1 = H, IBS2 = L, 3-BIT INPUT, 32-BIT LENGTH SHIFT REGISTER)



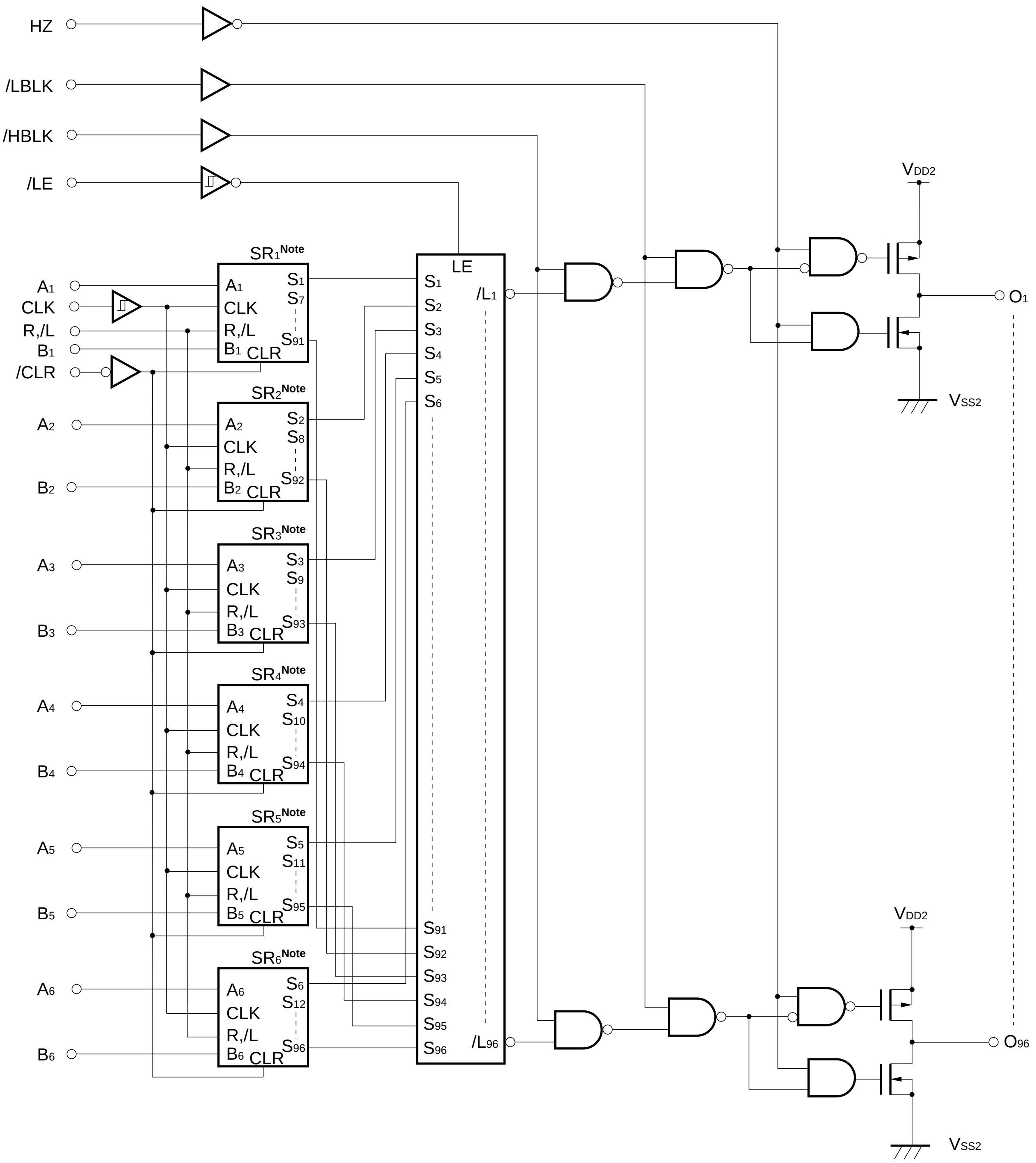
Note SRn: 32-bit shift register

1. BLOCK DIAGRAM (3) (IBS1 = L, IBS2 = H, 4-BIT INPUT, 24-BIT LENGTH SHIFT REGISTER)



Note SRn: 24-bit shift register

1. BLOCK DIAGRAM (4) (IBS1 = L, IBS2 = L, 6-BIT INPUT, 16-BIT LENGTH SHIFT REGISTER)



Note SRn: 16-bit shift register

2. PIN FUNCTIONS

Symbol	Pin Name	Description		
/LBLK	Low blanking input	/LBLK = L : All output = L		
/HBLK	High blanking input	/HBLK = L : All output = H		
/LE	Latch enable input	Latch executed on fall		
HZ	Output high impedance	Make all output high impedance by input H		
/CLR	Register clear input	Inputting the low level of this signal clears the entire contents of the shift register to low level.		
A_n	RIGHT data input/output Note	When R,/L = H, A_n : input B_n : output		
B_n	LEFT data input/output Note	When R,/L = L, A_n : output B_n : input		
CLK	Clock input	Shift executed on rise		
R,/L	Shift control input	Right shift mode when R,/L = H (In the case of 3-ch input) SR_1 : $A_1 \rightarrow S_1$.......$S_{94} \rightarrow B_1$ (Same direction for SR_2 and SR_3) Left shift mode when R,/L = L (In the case of 3-ch input) SR_1 : $B_1 \rightarrow S_{94}$.......$S_1 \rightarrow A_1$ (Same direction for SR_2 and SR_3) The shift direction is the same in the case of 2-/4-/6-ch input.		
IBS1,IBS2	Input mode switch	IBS1	IBS2	Input mode
		H	L	3-bit input, 32-bit length shift register
		L	L	6-bit input, 16-bit length shift register
		H	H	2-bit input, 48-bit length shift register
		L	H	4-bit input, 24-bit length shift register
O_1 to O_{96}	High withstand voltage output	120 V		
V_{DD1}	Logic power supply	5 V ± 10 %		
V_{DD2}	Driver power supply	20 to 110 V		
V_{SS1}	Logic ground	Connect to system ground		
V_{SS2}	Driver ground	Connect to system ground		

Note When input mode is 2-/3-/4-bit, set unused input and output pins “L” level.
To use for module, the back side of IC chip must be held at the V_{SS} (GND) level.

3. TRUTH TABLE

Shift Register Block

Input		Output		Shift Register
R,/L	CLK	A	B	
H	↑	Input	Output [Note1]	Right shift execution
H	H or L		Output	Hold
L	↑	Output [Note2]	Input	Left shift execution
L	H or L	Output		Hold

Notes 1. The data of S_{91} to S_{93} (in the case of 3-ch input) is shifted to S_{94} to S_{96} at the rising of the clock and then output from B_1 to B_3, respectively. This "shift → output" operation is the same in the case of 2-/4-/6-ch input.

2. The data of S_4 to S_6 (in the case of 3-ch input) is shifted to S_1 to S_3 at the rising of the clock and then output from A_1 to A_3, respectively. This "shift → output" operation is the same in the case of 2-/4-/6-ch input.

Latch Block

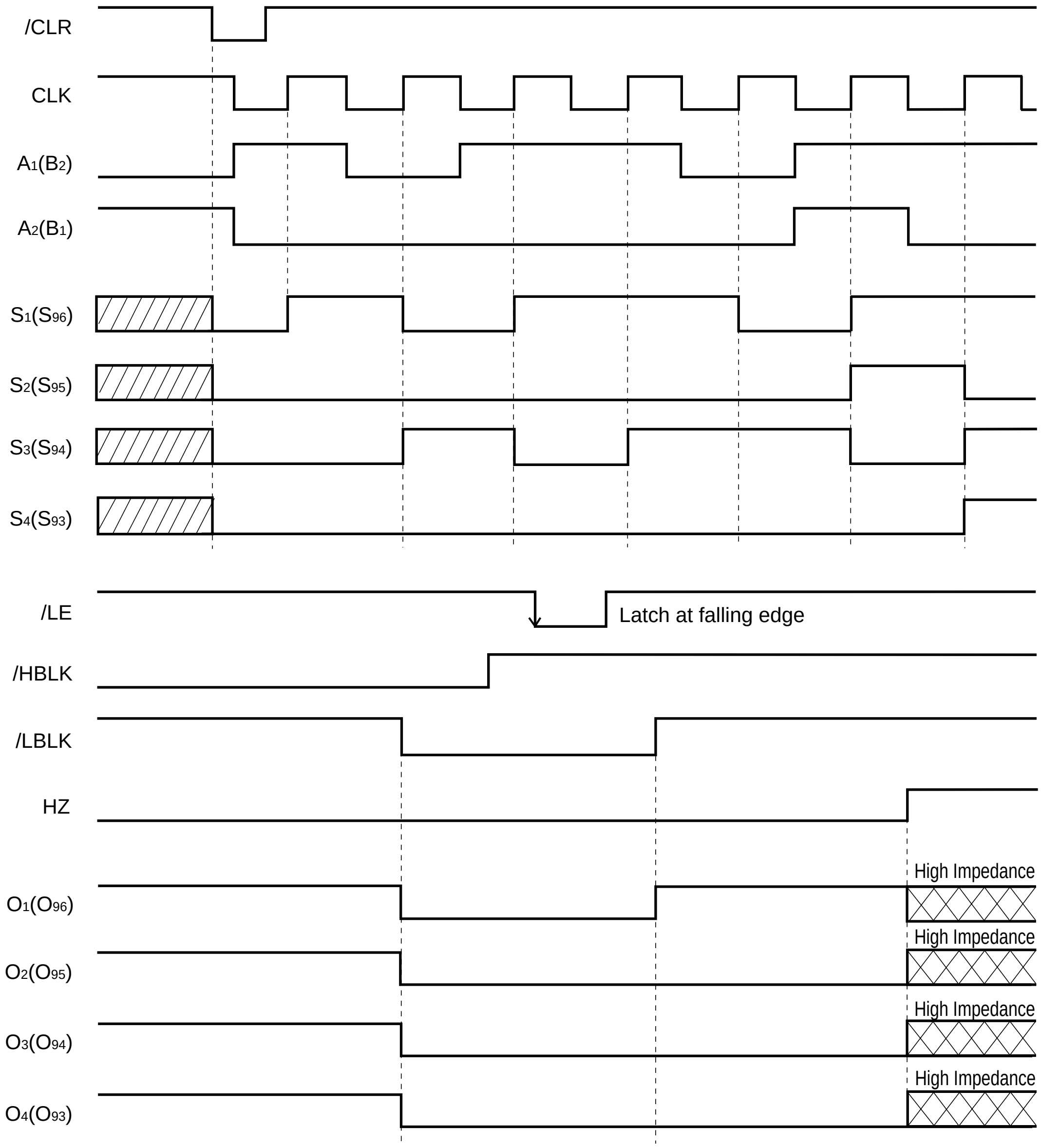
/LE	Output State of Latch Block (/L_n)
↓	Latch S_n data
H or L	Hold latch (output) data

Driver Block

A (B)	/HBLK	/LBLK	HZ	Output State of Driver Block
x	L	H	L	All driver output : H
x	x	L	L	All driver output : L
x	x	x	H	All driver output : High Impedance
L	H	H	L	L
H	H	H	L	H

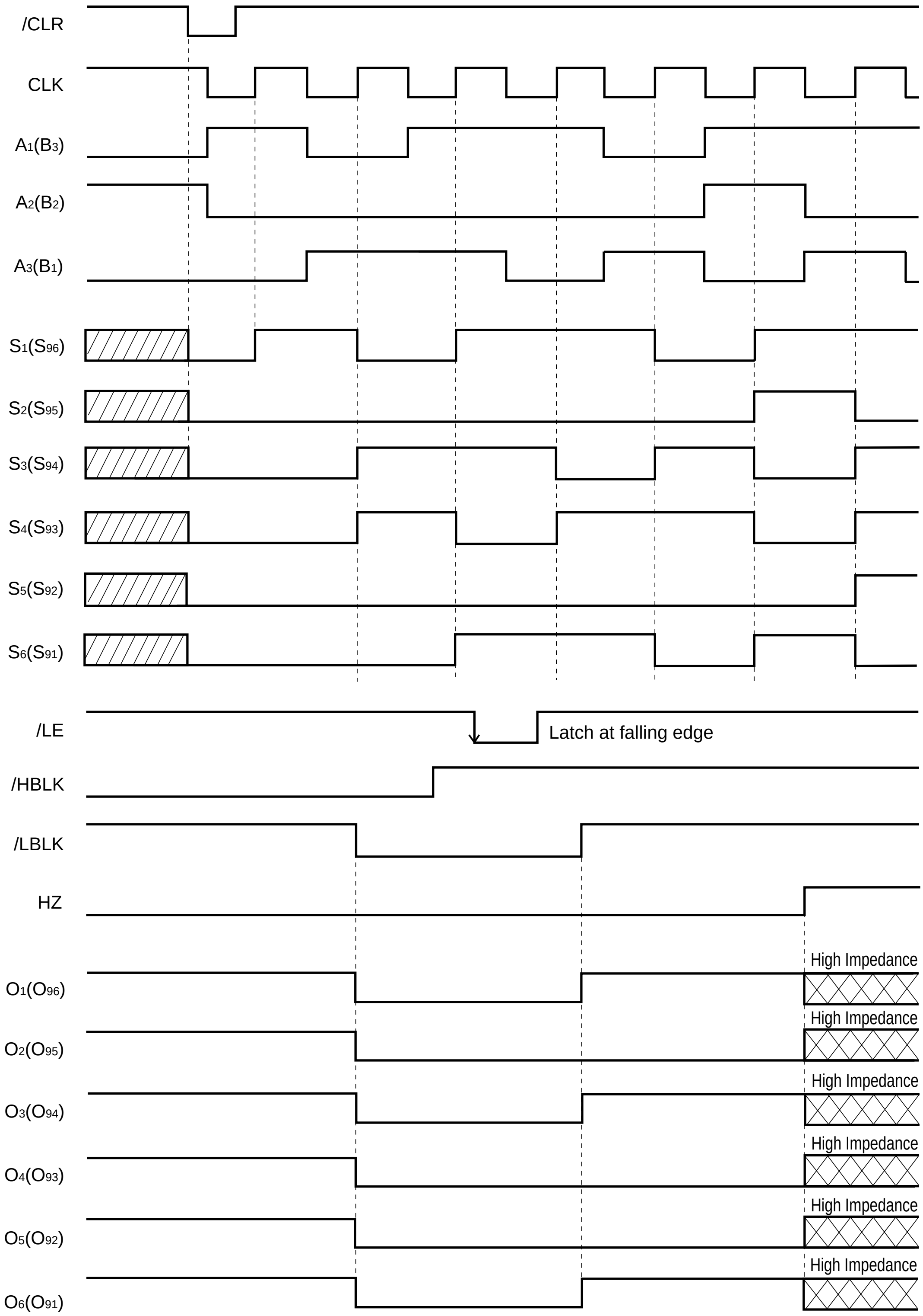
Remark x : H or L, H : High level, L : Low level

4. TIMING CHART (1) (IBS1 = H, IBS2 = H: 2-BIT INPUT, RIGHT SHIFT)



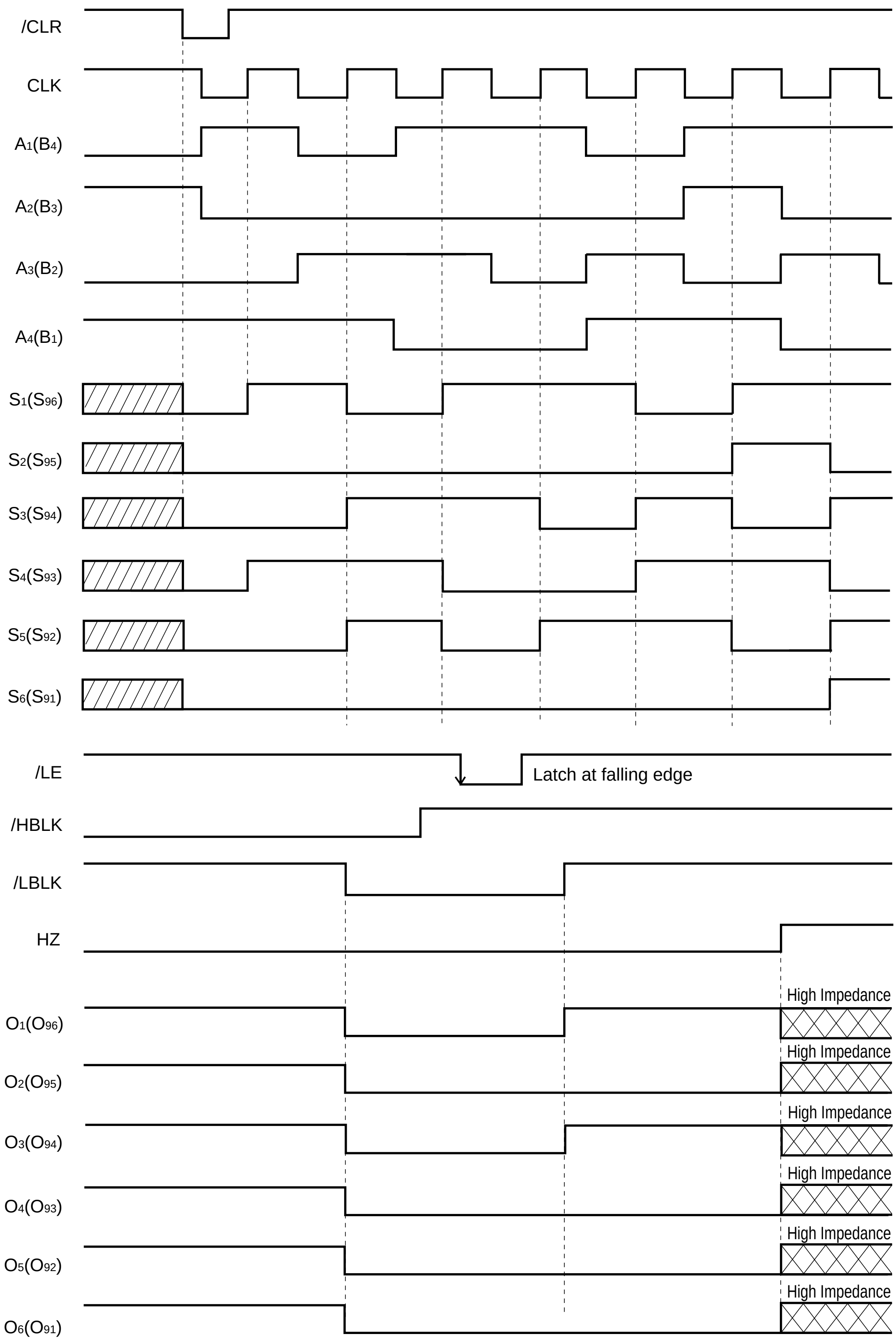
Remark Values in parentheses are when R,/L = L.

4. TIMING CHART (2) (IBS1 = H, IBS2 = L: 3-BIT INPUT, RIGHT SHIFT)



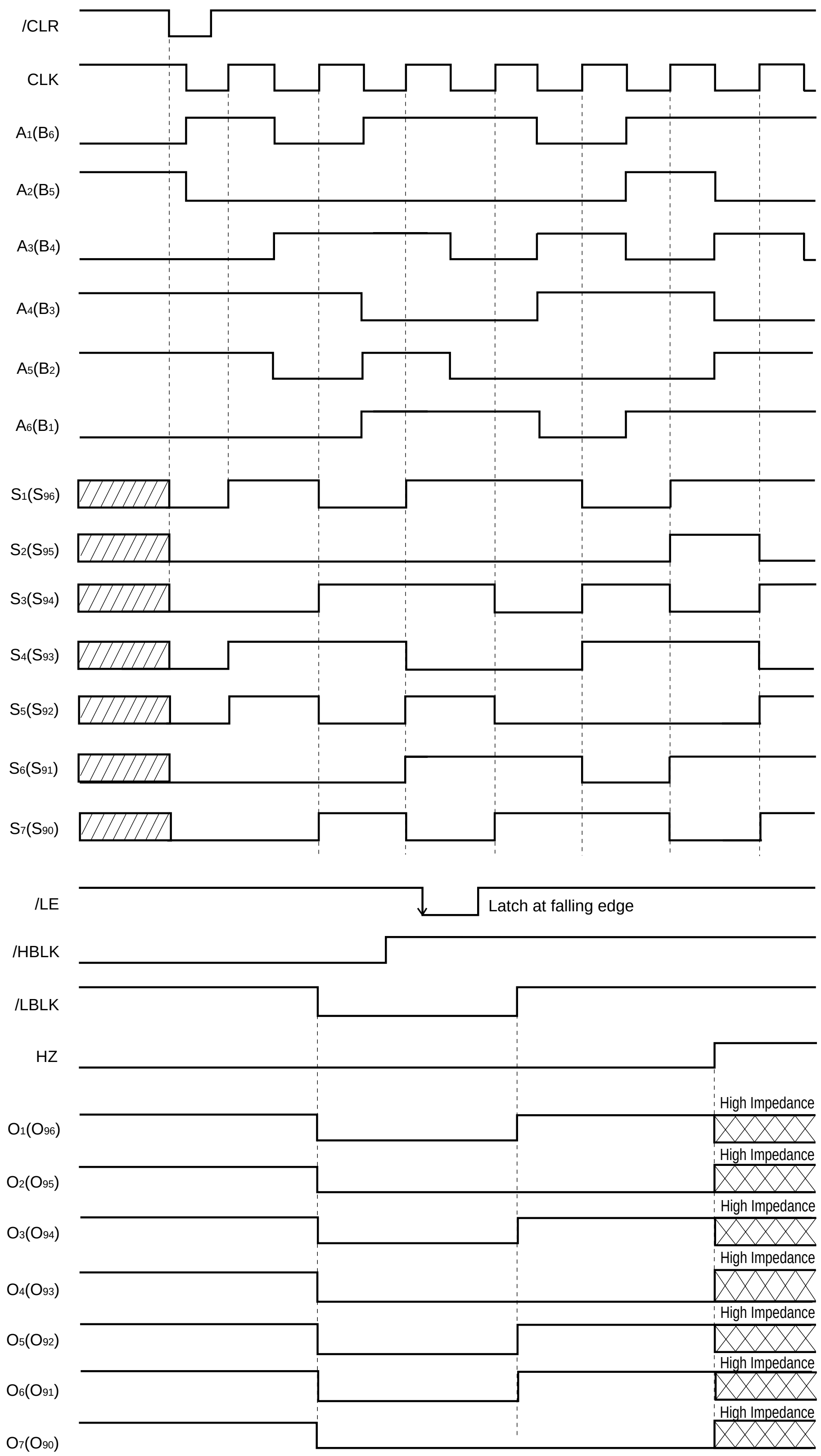
Remark Values in parentheses are when R,/L = L.

4. TIMING CHART (3) (IBS1 = L, IBS2 = H: 4-BIT INPUT, RIGHT SHIFT)



Remark Values in parentheses are when R,/L = L.

4. TIMING CHART (4) (IBS1 = L, IBS2 = L: 6-BIT INPUT, RIGHT SHIFT)



Remark Values in parentheses are when R,/L = L.

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, $V_{SS1} = V_{SS2}$ = 0 V)

	Parameter	Symbol	Conditions	Ratings	Unit
	Logic Supply Voltage	V_{DD1}		–0.5 to +6.0	V
	Driver Supply Voltage	V_{DD2}		–0.5 to +120	V
	Logic Input Voltage	V_I		–0.5 to V_{DD1} + 0.5	V
★	Driver Output Current	I_{O2}		+15 / –25	mA
	Operating Junction Temperature	T_J		+125	°C
	Storage Temperature	T_{stg}		–65 to +150	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –40 to +85 °C, $V_{SS1} = V_{SS2}$ = 0 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Logic Supply Voltage	V_{DD1}		4.5	5.0	5.5	V
	Driver Supply Voltage	V_{DD2}		20		110	V
	High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
	Low-Level Input Voltage	V_{IL}		0		0.2 V_{DD1}	V
★	Driver Output Current	I_{OH2}				–20	mA
		I_{OL2}				13	mA

Electrical Characteristics (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 110 V, $V_{SS1} = V_{SS2}$ = 0 V)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
	High-Level Output Voltage	V_{OH1}	Logic, I_{OH1} = –1.0 mA		0.9 V_{DD1}		V_{DD1}	V
	Low-Level Output Voltage	V_{OL1}	Logic, I_{OL1} = 1.0 mA		0		0.1 V_{DD1}	V
★	High-Level Output Voltage	V_{OH21}	O_1 to O_{96}	I_{OH2} = –0.4 mA	109			V
		V_{OH22}		I_{OH2} = –4.3 mA	105			V
★	Low-Level Output Voltage	V_{OL21}		I_{OL2} = 1.6 mA			1.0	V
		V_{OL22}		I_{OL2} = 13 mA			10	V
	Input Leakage Current	I_{IL}	$V_1 = V_{DD1}$ or V_{SS1}				±1.0	μA
	High-Level Intput Voltage	V_{IH}			0.7 V_{DD1}			V
	Low-Level Input Voltage	V_{IL}					0.2 V_{DD1}	V
	Static Current Dissipation	I_{DD1}	Logic, T_A = –40 to +85 °C				500	μA
			Logic, T_A = 25 °C				300	μA
		I_{DD2}	Driver, T_A = –40 to +85 °C				1000	μA
			Driver, T_A = 25 °C				100	μA

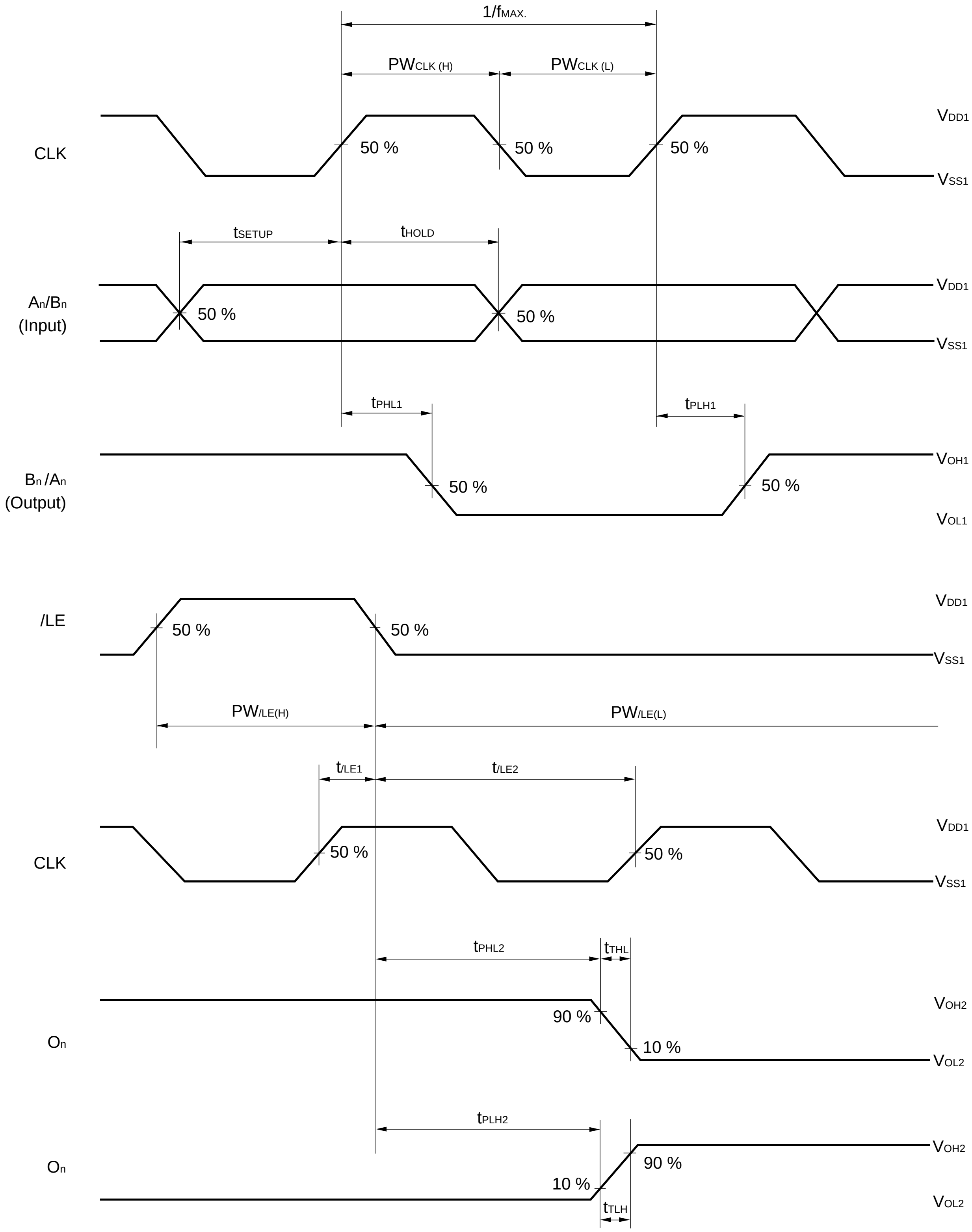
Switching Characteristics (T_A = +25 °C, V_{DD1} = 5.0 V, V_{DD2} = 110 V, V_{SS1} = V_{SS2} = 0 V, Logic C_L = 15 pF, Driver C_L = 50 pF, t_r = t_f = 6.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Propagation Delay Time	t_{PHL1}	CLK ↑ → A/B			34	ns
	t_{PLH1}				34	ns
	t_{PHL2}	/LE ↓ → O_1 to O_{96}			180	ns
	t_{PLH2}				180	ns
	t_{PHL3}	/HBLK → O_1 to O_{96}			165	ns
	t_{PLH3}				165	ns
	t_{PHL4}	/LBLK → O_1 to O_{96}			160	ns
	t_{PLH4}				160	ns
	t_{PHZ}	HZ → O_1 to O_{96}			300	ns
	t_{PZH}	R_L = 10 kΩ			180	ns
	t_{PLZ}				300	ns
	t_{PZL}				180	ns
★ Rise Time	t_{TLH}	O_1 to O_{96}			360	ns
	t_{TLZ}	O_1 to O_{96}			3	μs
	t_{TZH}	R_L = 10 kΩ			360	ns
★ Fall Time	t_{THL}	O_1 to O_{96}			450	ns
	t_{THZ}	O_1 to O_{96}			3	μs
	t_{TZL}	R_L = 10 kΩ			450	ns
Maximum Clock Frequency	$f_{MAX.}$	When data is read, duty = 50 %	40			MHz
		Cascade connection : Duty = 50 %	25			MHz
Input Capacitance	C_I				15	pF

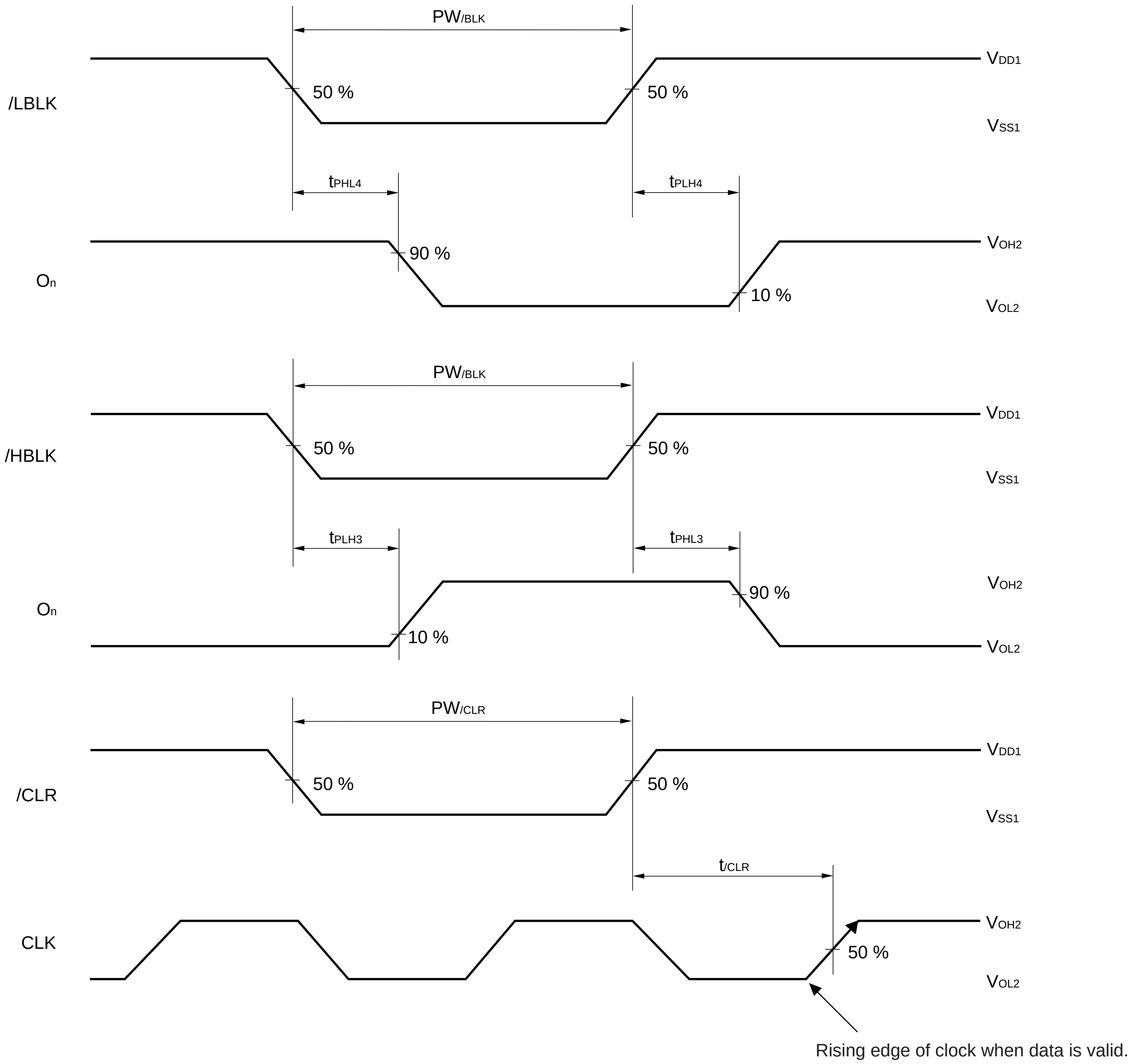
Timing Requirement (T_A = –40 to +85 °C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 6.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	$PW_{CLK(H)}$, $PW_{CLK(L)}$		12			ns
Latch Enable Pulse Width	$PW_{/LE}$		12			ns
★ Blank Pulse Width	$PW_{/BLK}$	/HBLK, /LBLK	600			ns
HZ Pulse Width	PW_{HZ}	R_L = 10 kΩ	3.3			μs
/CLR Pulse Width	$PW_{/CLR}$		12			ns
Data Setup Time	t_{SETUP}		4			ns
Data Hold Time	t_{HOLD}		6			ns
Latch Enable Time	$t_{/LE1}$		12			ns
	$t_{/LE2}$		12			ns
/CLR Timing	$t_{/CLR}$		6			ns

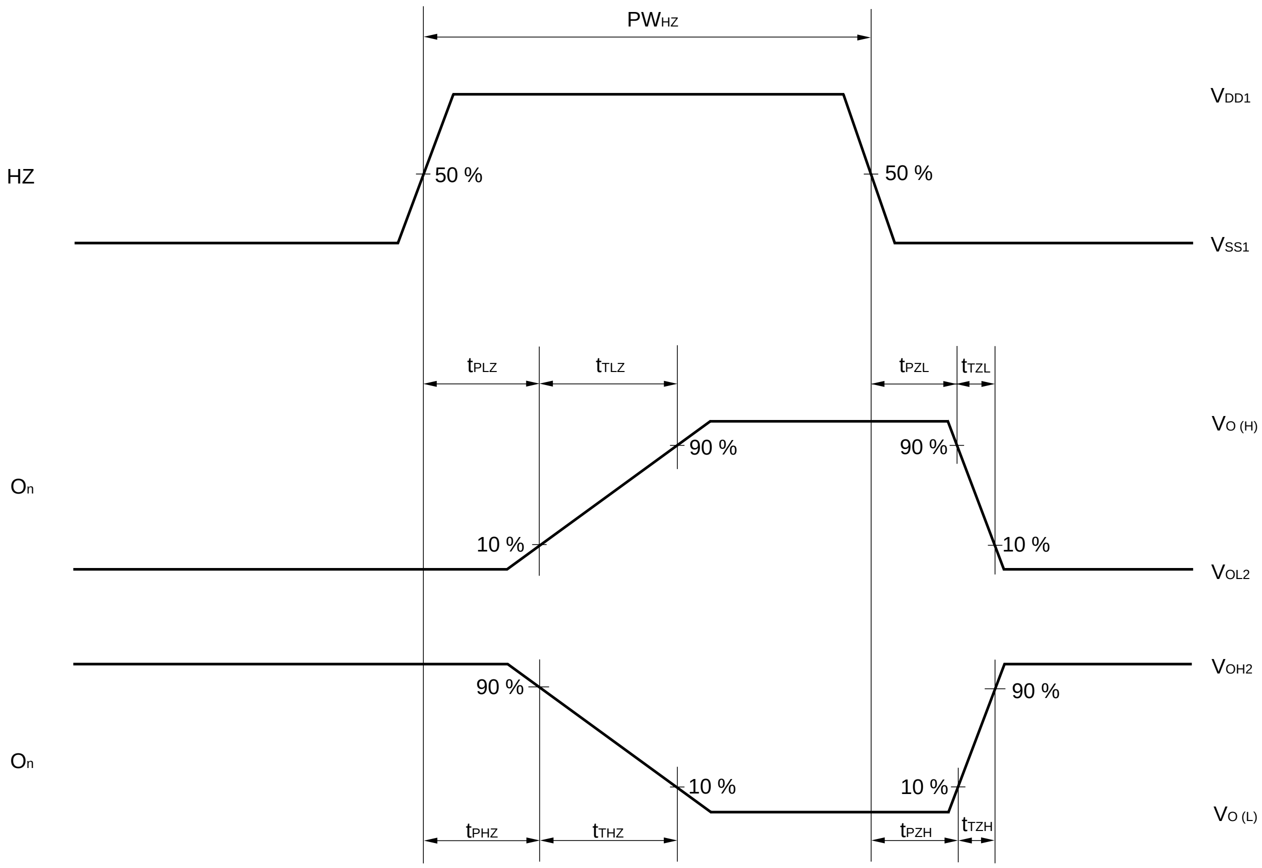
6. Switching Characteristics Waveform (1/3)



6. Switching Characteristics Waveform (2/3)



6. Switching Characteristics Waveform (3/3)



[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System(C10983E)

Quality Grades to NEC's Semiconductor Devices(C11531E)