

96-BIT AC-PDP DRIVER

★ DESCRIPTION

The μ PD16341 is high withstand voltage CMOS driver designed for flat display panels such as PDPs, VFDs and ELs. It consists of a 96-bit bi-directional shift register, 96-bit latch and high withstand voltage CMOS driver. The logic block is designed to operate using a 5-V power supply interface enabling direct connection to a gate array or a microcontroller. In addition, the μ PD16341 achieves low power dissipation by employing the CMOS structure while having a high withstand voltage output (120 V, +15/-25 mA MAX.).

FEATURES

- 2-/3-/4-/6-ch input port switching is possible using IBS1 and IBS2 pins
- Data control with transfer clock (external) and latch
- High-speed data transfer (f_{MAX.} = 40 MHz MIN. at data latch)
(f_{MAX.} = 25 MHz MIN. at cascade connection)
- ★ • High withstand output voltage: 120 V, +15/-25 mA MAX.
- 5-V CMOS input interface
- High withstand voltage CMOS structure

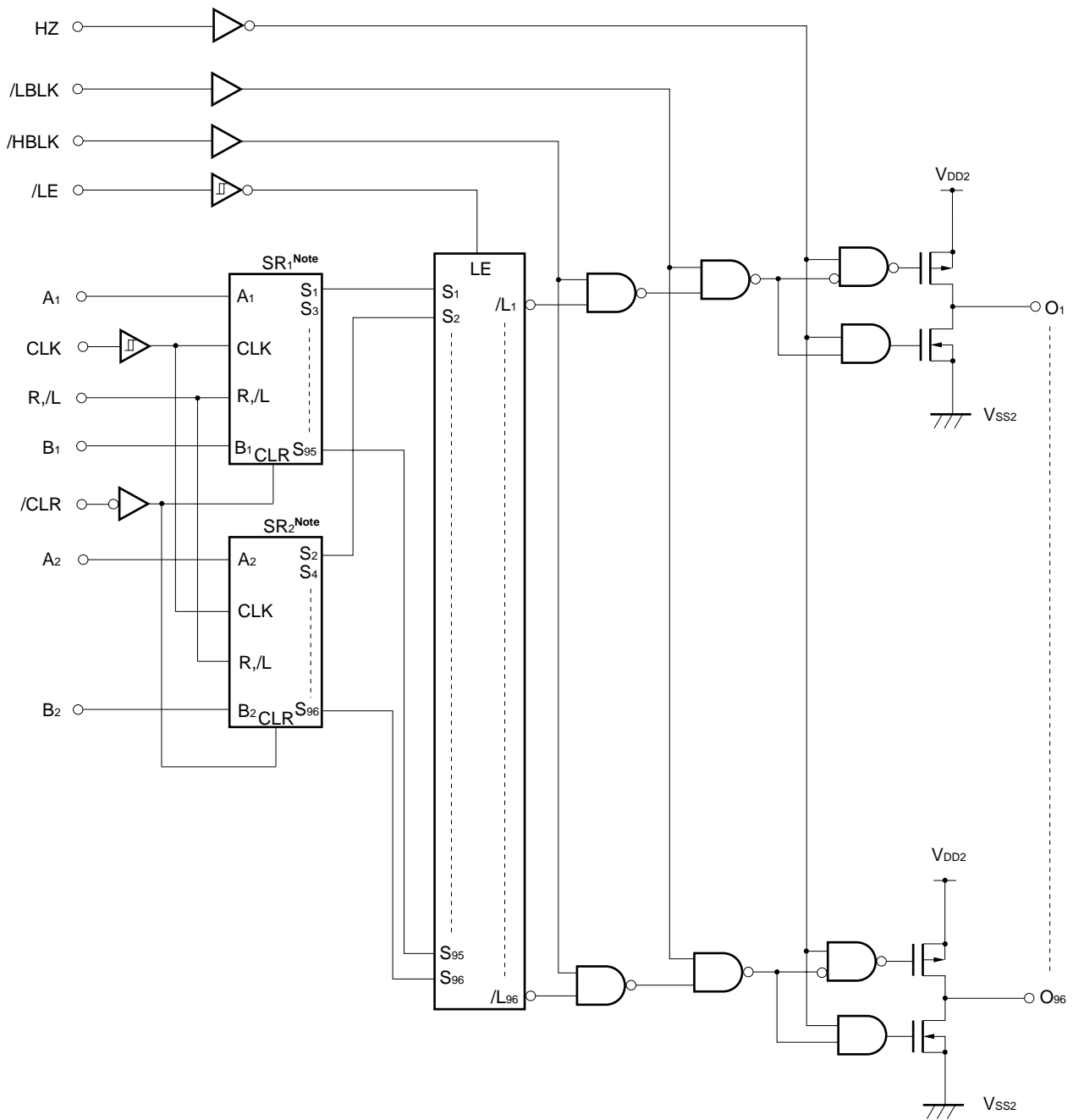
★ ORDERING INFORMATION

Part Number	Package
μ PD16341	Module

Remark Consult an NEC sales representative regarding the module. Since the module characteristics is based on the module specifications, there may be differences between the contents written in this document and real characteristics.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

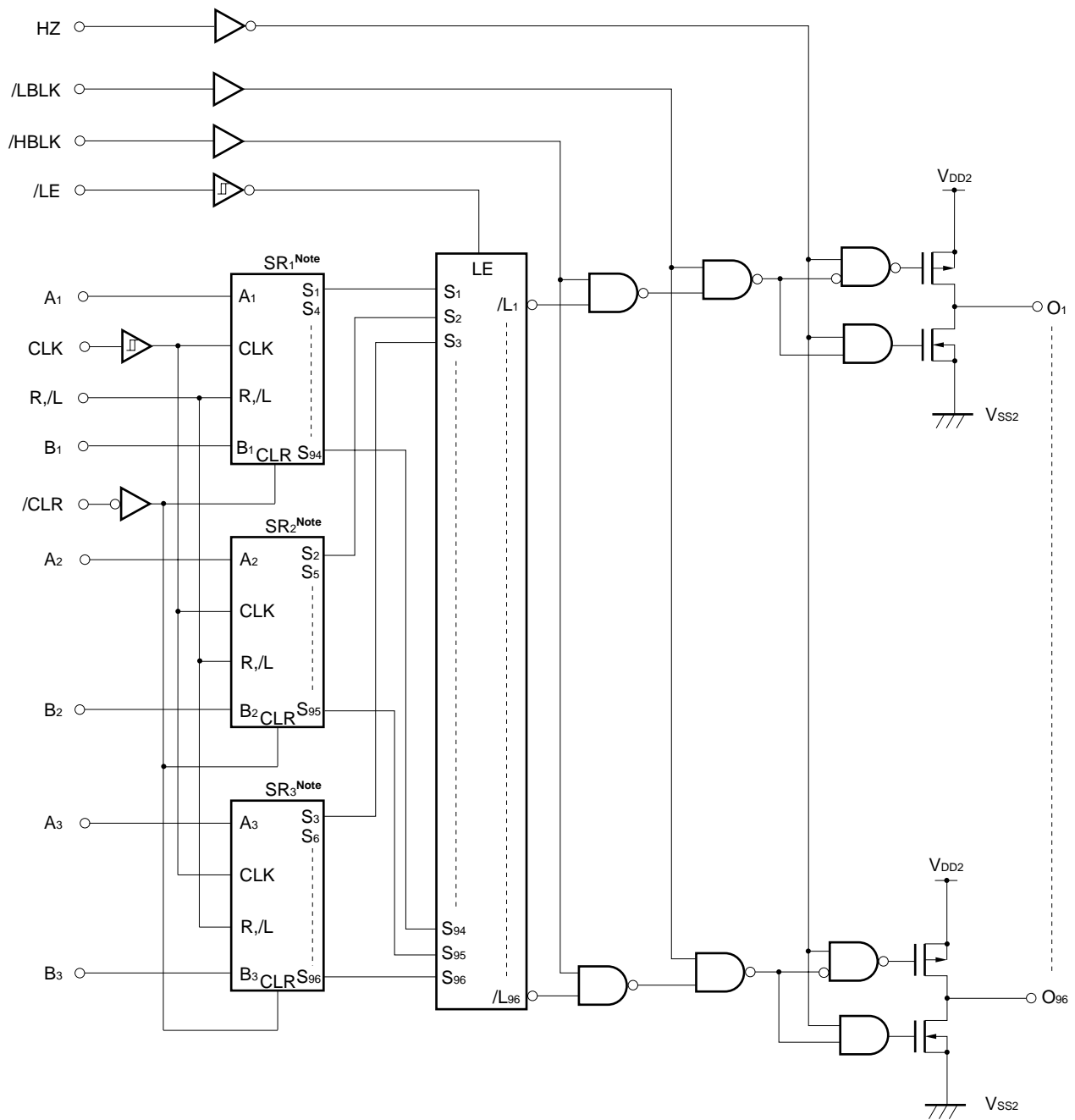
1. BLOCK DIAGRAM (1) (IBS1 = H, IBS2 = H, 2-BIT INPUT, 48-BIT LENGTH SHIFT REGISTER)



Note SRn: 48-bit shift register

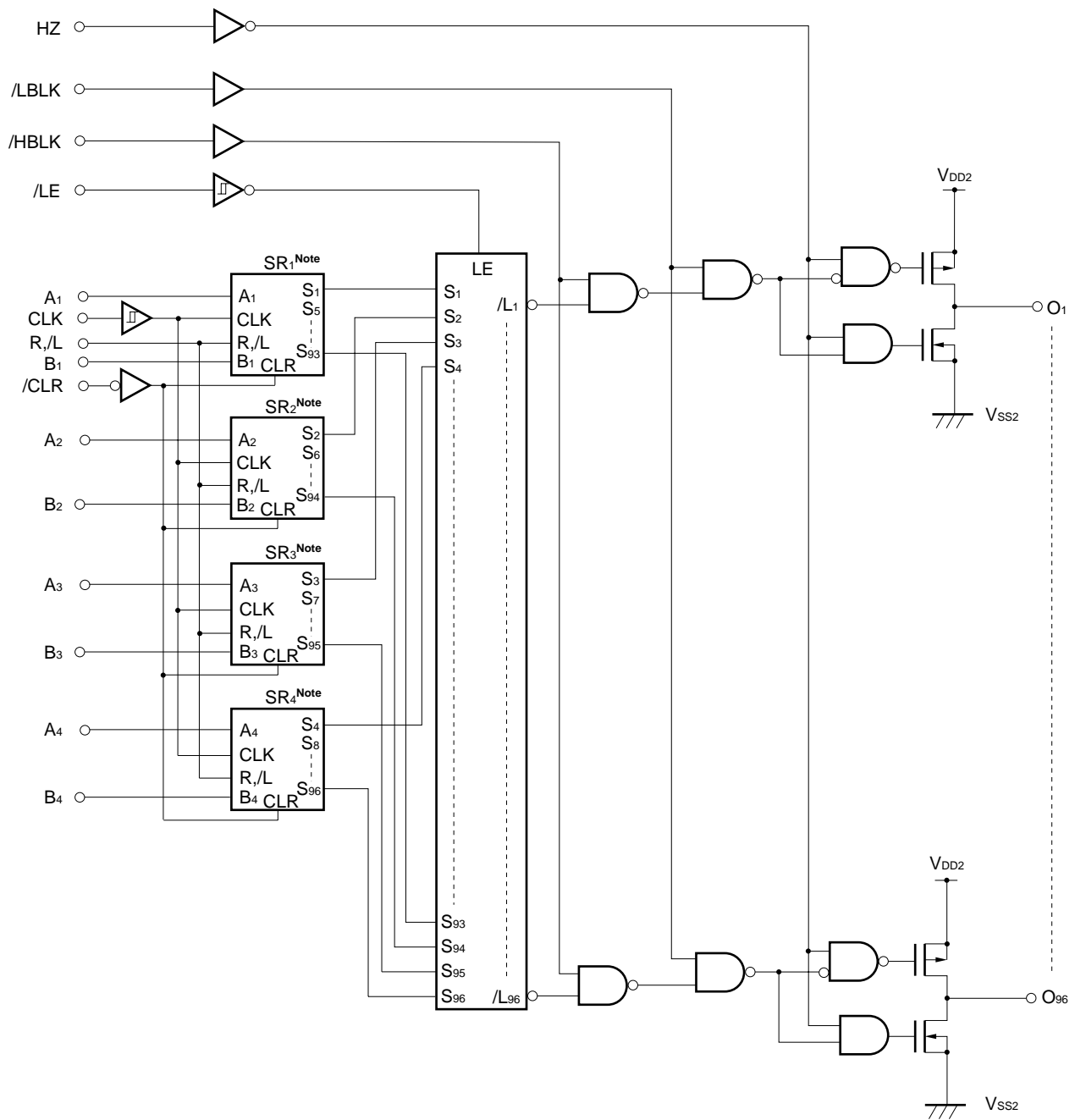
Remark /xxx indicates active low signal.

1. BLOCK DIAGRAM (2) (IBS1 = H, IBS2 = L, 3-BIT INPUT, 32-BIT LENGTH SHIFT REGISTER)



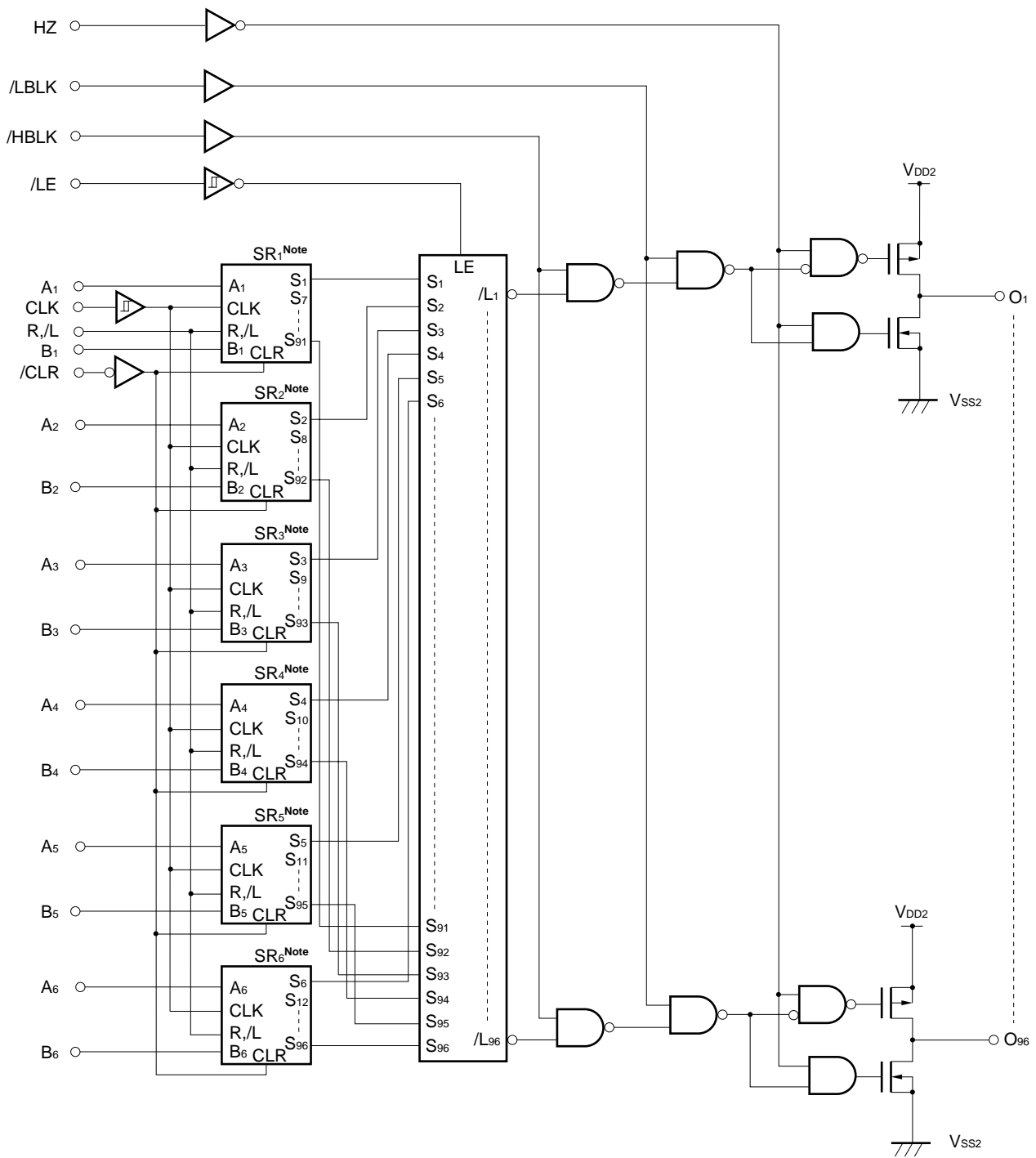
Note SR_n: 32-bit shift register

1. BLOCK DIAGRAM (3) (IBS1 = L, IBS2 = H, 4-BIT INPUT, 24-BIT LENGTH SHIFT REGISTER)



Note SR_n: 24-bit shift register

1. BLOCK DIAGRAM (4) (IBS1 = L, IBS2 = L, 6-BIT INPUT, 16-BIT LENGTH SHIFT REGISTER)



Note SR_n: 16-bit shift register

2. PIN FUNCTIONS

Symbol	Pin Name	Description
/LCLK	Low blanking input	/LCLK = L : All output = L
/HCLK	High blanking input	/HCLK = L : All output = H
/LE	Latch enable input	Latch executed on fall
HZ	Output high impedance	Make all output high impedance by input H
/CLR	Register clear input	Inputting the low level of this signal clears the entire contents of the shift register to low level.
A _n	RIGHT data input/output ^{Note}	When R _n /L = H, A _n : input B _n : output
B _n	LEFT data input/output ^{Note}	When R _n /L = L, A _n : output B _n : input
CLK	Clock input	Shift executed on rise
R _n /L	Shift control input	Right shift mode when R _n /L = H (In the case of 3-ch input) SR ₁ : A ₁ → S ₁S ₉₄ → B ₁ (Same direction for SR ₂ and SR ₃) Left shift mode when R _n /L = L (In the case of 3-ch input) SR ₁ : B ₁ → S ₉₄S ₁ → A ₁ (Same direction for SR ₂ and SR ₃) The shift direction is the same in the case of 2-/4-/6-ch input.
IBS1,IBS2	Input mode switch	IBS1 IBS2 Input mode
		H L 3-bit input, 32-bit length shift register
		L L 6-bit input, 16-bit length shift register
		H H 2-bit input, 48-bit length shift register
		L H 4-bit input, 24-bit length shift register
O ₁ to O ₉₆	High withstand voltage output	120 V
V _{DD1}	Logic power supply	5 V ± 10 %
V _{DD2}	Driver power supply	20 to 110 V
V _{SS1}	Logic ground	Connect to system ground
V _{SS2}	Driver ground	Connect to system ground

Note When input mode is 2-/3-/4-bit, set unused input and output pins “L” level.
To use for module, the back side of IC chip must be held at the V_{ss} (GND) level.

3. TRUTH TABLE

Shift Register Block

Input		Output		Shift Register
R _n /L	CLK	A	B	
H	↑	Input	Output ^{Note1}	Right shift execution
H	H or L		Output	Hold
L	↑	Output ^{Note2}	Input	Left shift execution
L	H or L	Output		Hold

- Notes**
1. The data of S₉₁ to S₉₃ (in the case of 3-ch input) is shifted to S₉₄ to S₉₆ at the rising of the clock and then output from B₁ to B₃, respectively. This “shift → output” operation is the same in the case of 2-/4-/6-ch input.
 2. The data of S₄ to S₆ (in the case of 3-ch input) is shifted to S₁ to S₃ at the rising of the clock and then output from A₁ to A₃, respectively. This “shift → output” operation is the same in the case of 2-/4-/6-ch input.

Latch Block

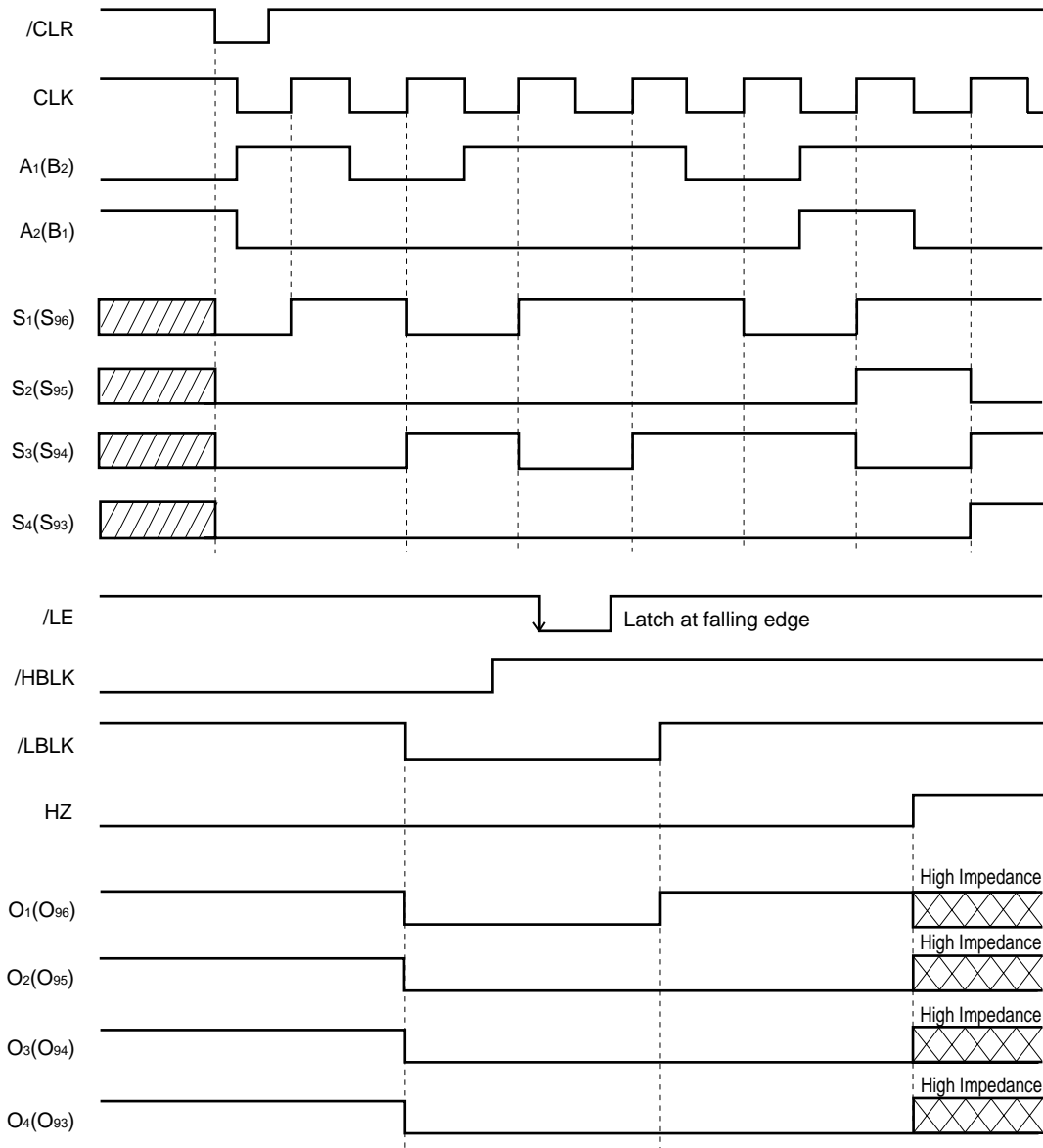
/LE	Output State of Latch Block (/L _n)
↓	Latch S _n data
H or L	Hold latch (output) data

Driver Block

A (B)	/HBLK	/LBLK	HZ	Output State of Driver Block
x	L	H	L	All driver output : H
x	x	L	L	All driver output : L
x	x	x	H	All driver output : High Impedance
L	H	H	L	L
H	H	H	L	H

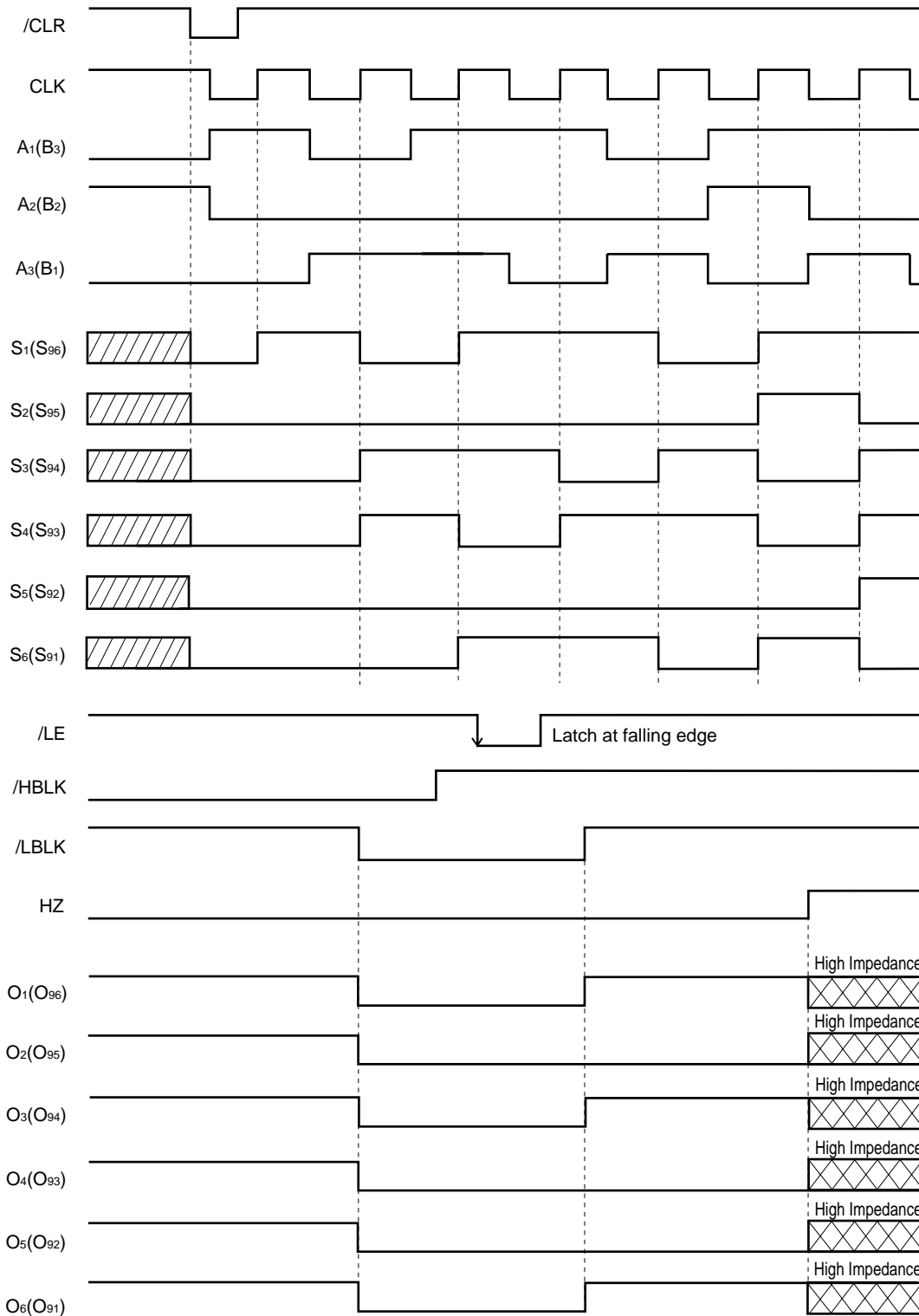
Remark x : H or L, H : High level, L : Low level

4. TIMING CHART (1) (IBS1 = H, IBS2 = H: 2-BIT INPUT, RIGHT SHIFT)



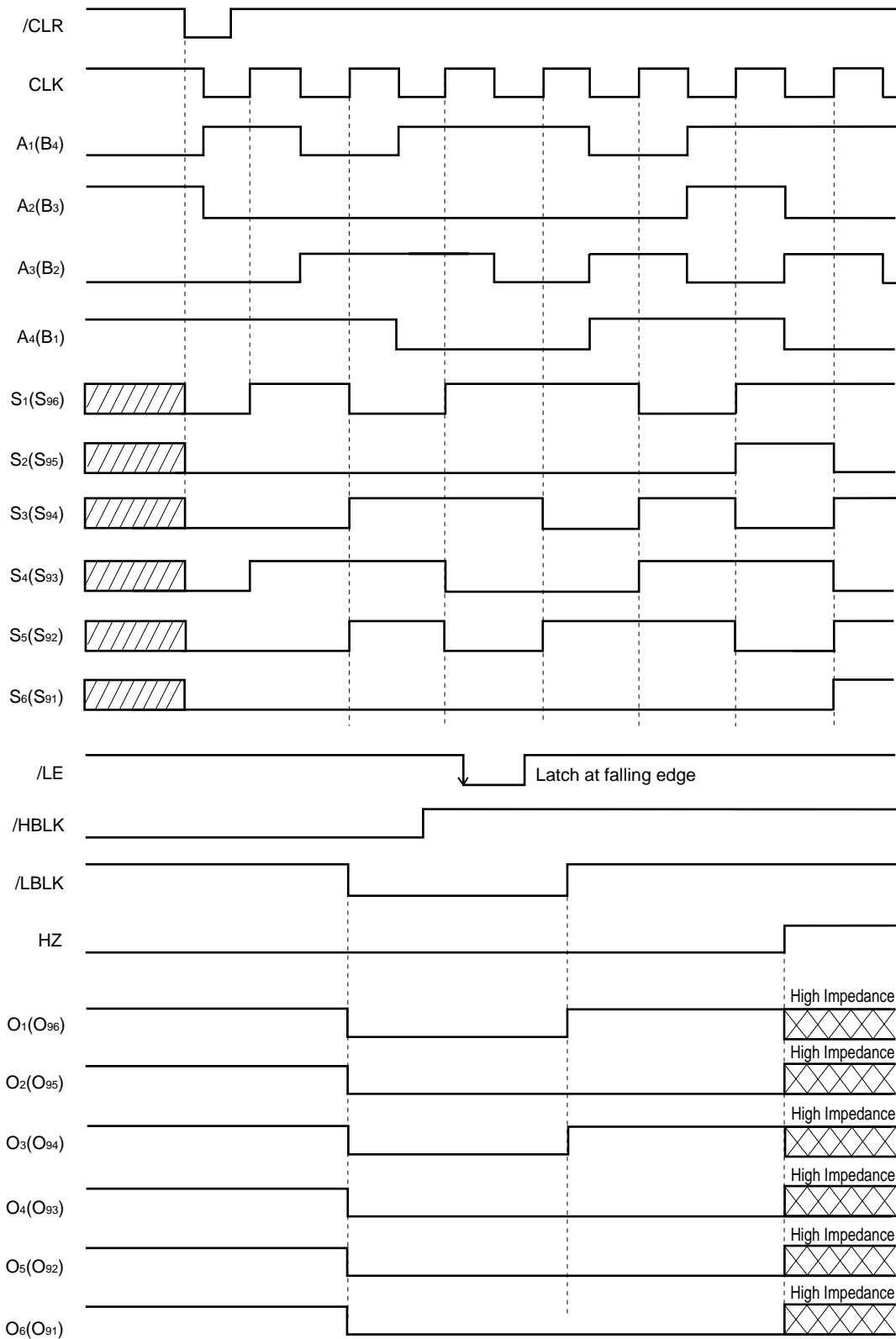
Remark Values in parentheses are when R,/L = L.

4. TIMING CHART (2) (IBS1 = H, IBS2 = L: 3-BIT INPUT, RIGHT SHIFT)



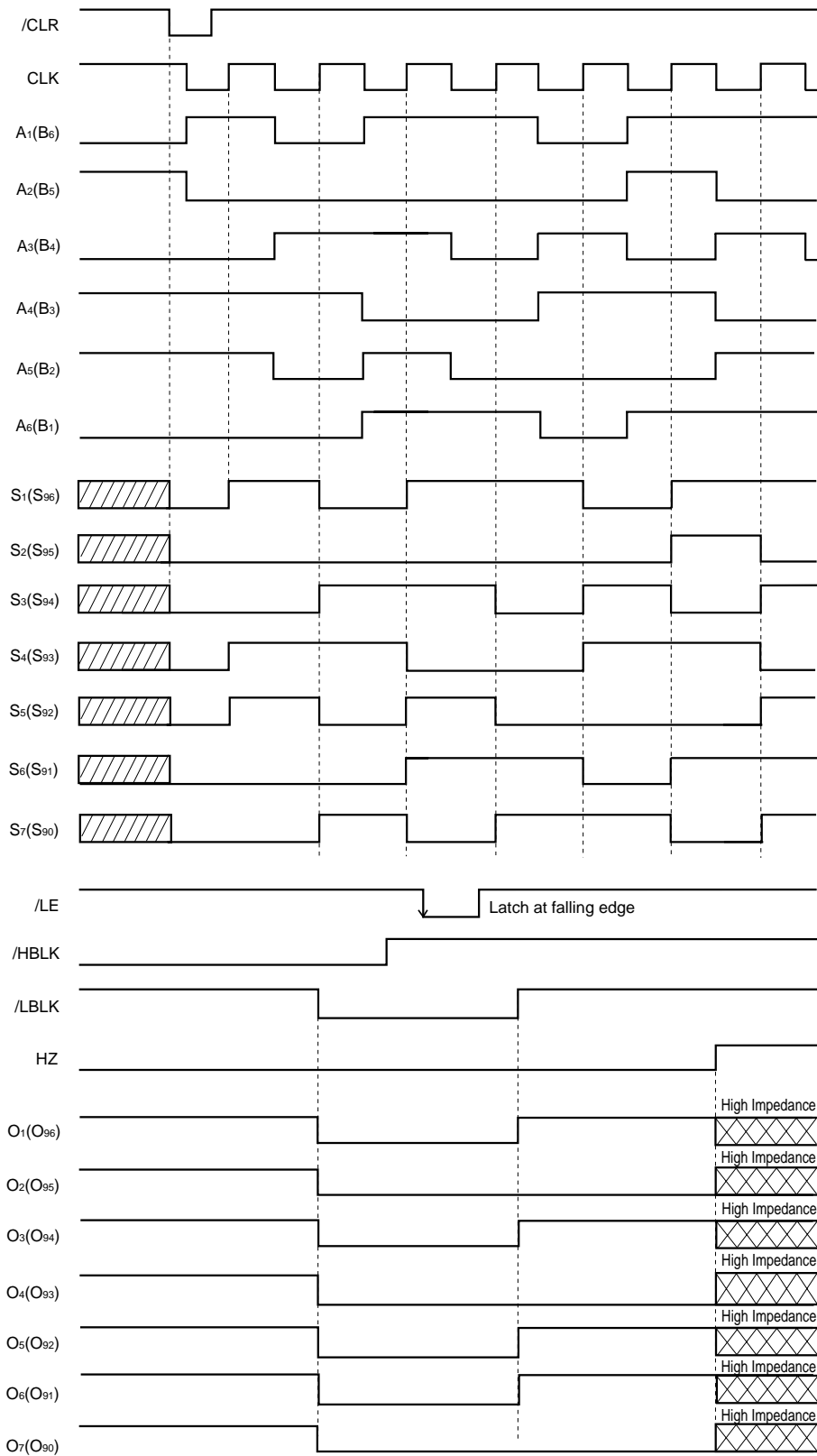
Remark Values in parentheses are when R,/L = L.

4. TIMING CHART (3) (IBS1 = L, IBS2 = H: 4-BIT INPUT, RIGHT SHIFT)



Remark Values in parentheses are when R,/L = L.

4. TIMING CHART (4) (IBS1 = L, IBS2 = L: 6-BIT INPUT, RIGHT SHIFT)



Remark Values in parentheses are when R_i/L_i = L.

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Logic Supply Voltage	V _{DD1}		-0.5 to +6.0	V
Driver Supply Voltage	V _{DD2}		-0.5 to +120	V
Logic Input Voltage	V _I		-0.5 to V _{DD1} + 0.5	V
★ Driver Output Current	I _{O2}		+15 / -25	mA
Operating Junction Temperature	T _J		+125	°C
Storage Temperature	T _{stg}		-65 to +150	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = -40 to +85 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V _{DD1}		4.5	5.0	5.5	V
Driver Supply Voltage	V _{DD2}		20		110	V
High-Level Input Voltage	V _{IH}		0.7 V _{DD1}		V _{DD1}	V
Low-Level Input Voltage	V _{IL}		0		0.2 V _{DD1}	V
★ Driver Output Current	I _{OH2}				-20	mA
	I _{OL2}				13	mA

Electrical Characteristics (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 110 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V _{OH1}	Logic, I _{OH1} = -1.0 mA	0.9 V _{DD1}		V _{DD1}	V
Low-Level Output Voltage	V _{OL1}	Logic, I _{OL1} = 1.0 mA	0		0.1 V _{DD1}	V
★ High-Level Output Voltage	V _{OH21}	O ₁ to O ₉₆ I _{OH2} = -0.4 mA	109			V
	V _{OH22}		I _{OH2} = -4.3 mA	105		V
★ Low-Level Output Voltage	V _{OL21}	I _{OL2} = 1.6 mA			1.0	V
	V _{OL22}		I _{OL2} = 13 mA		10	V
Input Leakage Current	I _{IL}	V _I = V _{DD1} or V _{SS1}			±1.0	μA
High-Level Input Voltage	V _{IH}		0.7 V _{DD1}			V
Low-Level Input Voltage	V _{IL}				0.2 V _{DD1}	V
Static Current Dissipation	I _{DD1}	Logic, T _A = -40 to +85 °C			500	μA
		Logic, T _A = 25 °C			300	μA
	I _{DD2}	Driver, T _A = -40 to +85 °C			1000	μA
		Driver, T _A = 25 °C			100	μA

Switching Characteristics (T_A = +25 °C, V_{DD1} = 5.0 V, V_{DD2} = 110 V, V_{SS1} = V_{SS2} = 0 V, Logic C_L = 15 pF,

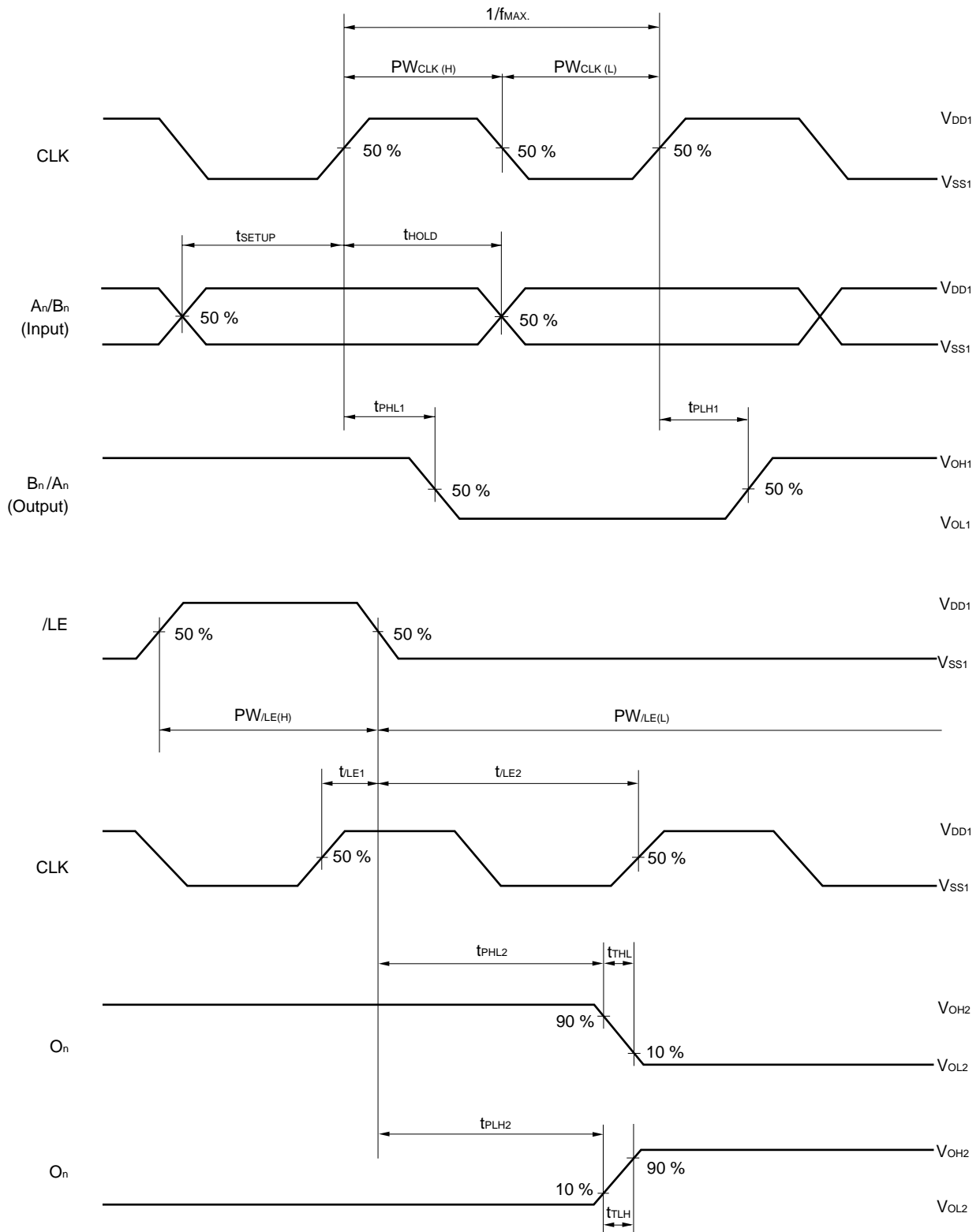
Driver C_L = 50 pF, t_r = t_f = 6.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Propagation Delay Time	t _{PHL1}	CLK ↑ → A/B			34	ns
	t _{PLH1}				34	ns
	t _{PHL2}	/LE ↓ → O ₁ to O ₉₆			180	ns
	t _{PLH2}				180	ns
	t _{PHL3}	/HBLK → O ₁ to O ₉₆			165	ns
	t _{PLH3}				165	ns
	t _{PHL4}	/LBLK → O ₁ to O ₉₆			160	ns
	t _{PLH4}				160	ns
	t _{PHZ}	HZ → O ₁ to O ₉₆			300	ns
	t _{PZH}	R _L = 10 kΩ			180	ns
	t _{PLZ}				300	ns
	t _{PZL}				180	ns
★ Rise Time	t _{TLH}	O ₁ to O ₉₆			360	ns
	t _{TLZ}	O ₁ to O ₉₆			3	μs
	t _{TZH}	R _L = 10 kΩ			360	ns
★ Fall Time	t _{THL}	O ₁ to O ₉₆			450	ns
	t _{THZ}	O ₁ to O ₉₆			3	μs
	t _{TZL}	R _L = 10 kΩ			450	ns
Maximum Clock Frequency	f _{MAX.}	When data is read, duty = 50 %	40			MHz
		Cascade connection : Duty = 50 %	25			MHz
Input Capacitance	C _i				15	pF

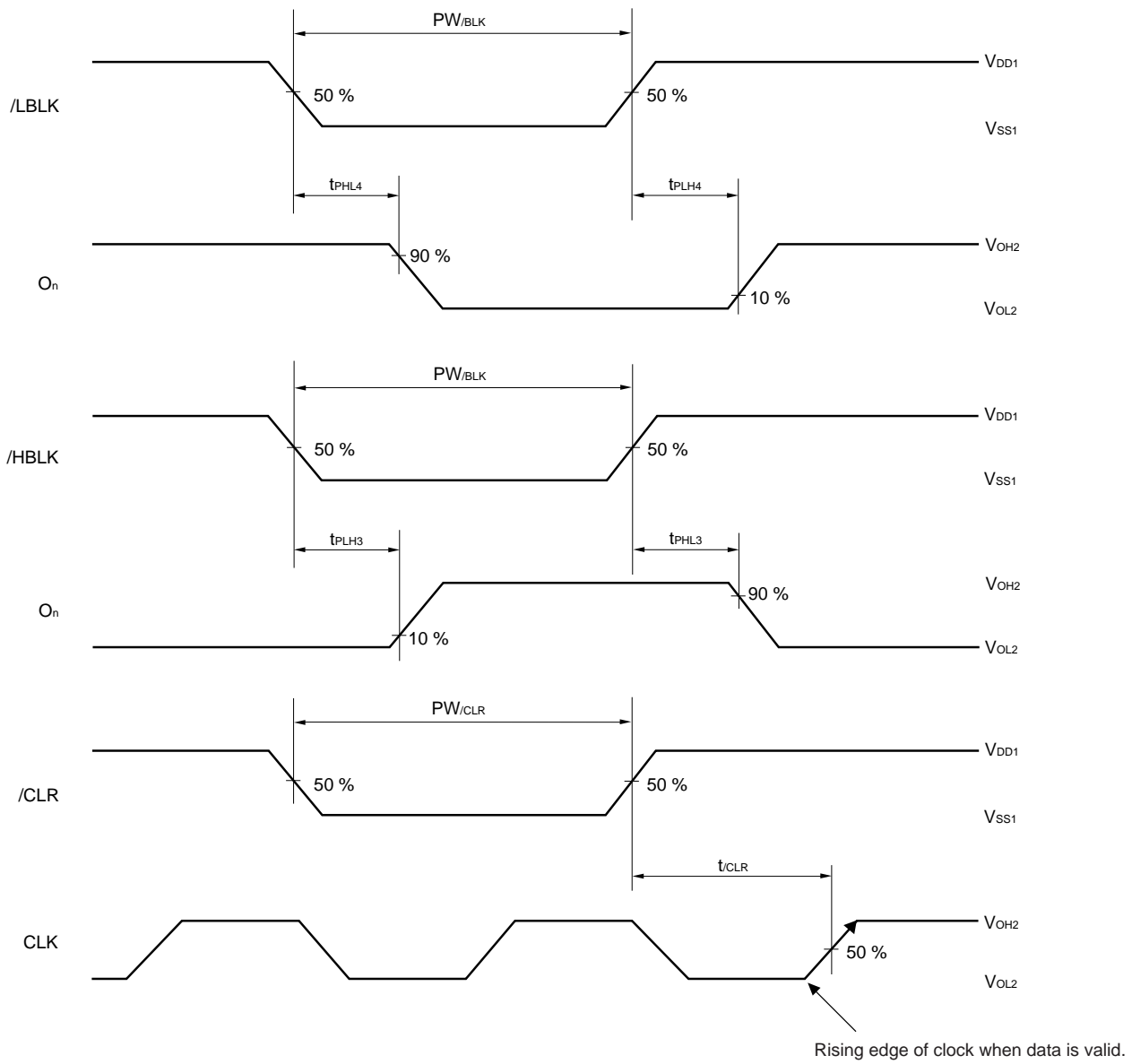
Timing Requirement (T_A = -40 to +85 °C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 6.0 ns)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW _{CLK(H)}		12			ns
	PW _{CLK(L)}					
Latch Enable Pulse Width	PW _{/LE}		12			ns
★ Blank Pulse Width	PW _{/BLK}	/HBLK, /LBLK	600			ns
HZ Pulse Width	PW _{HZ}	R _L = 10 kΩ	3.3			μs
/CLR Pulse Width	PW _{/CLR}		12			ns
Data Setup Time	t _{SETUP}		4			ns
Data Hold Time	t _{HOLD}		6			ns
Latch Enable Time	t _{LE1}		12			ns
	t _{LE2}		12			ns
/CLR Timing	t _{/CLR}		6			ns

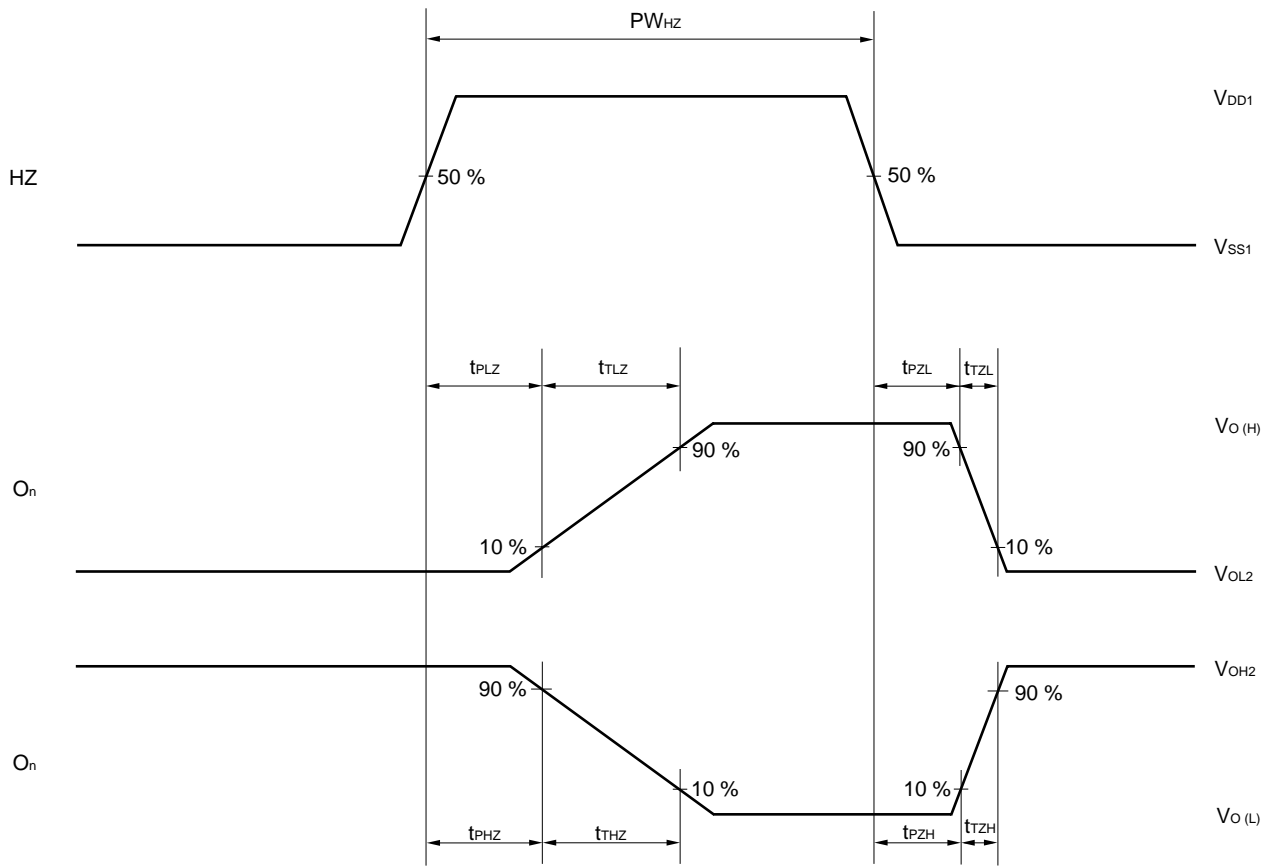
6. Switching Characteristics Waveform (1/3)



6. Switching Characteristics Waveform (2/3)



6. Switching Characteristics Waveform (3/3)



[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents**NEC Semiconductor Device Reliability/Quality Control System(C10983E)****Quality Grades to NEC's Semiconductor Devices(C11531E)**

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 - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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