NEC

MOS INTEGRATED CIRCUIT

μPD45D128442, 45D128842, 45D128164

128 M-bit Synchronous DRAM with Double Data Rate (4-bank, SSTL_2)

Description

The μPD45D128442, 45D128842, 45D128164 are high-speed 134,217,728 bits synchronous dynamic random-access memories, organized as 8,388,608x4x4, 4194,304x8x4, 2,097,152x16x4 (word x bit x bank), respectively.

The synchronous DRAMs use Double Data Rate (DDR) where data bandwidth is twice of regular synchronous DRAM.

The synchronous DRAM is compatible with SSTL_2 (Stub Series terminated Logic for 2.5 V).

The synchronous DRAM is packaged in 66-pin Plastic TSOP (II).

Features

- Fully Synchronous Dynamic RAM with all input signals except DM, DQS and DQ referenced to a positive clock edge
- Double Data Rate interface
  - Differential CLK (/CLK) input
  - Data inputs and DM are synchronized with both edges of DQS
  - Data outputs and DQS are synchronized with a cross point of CLK and /CLK
- Quad internal banks operation
- Possible to assert random column address in every clock cycle
- Programmable Mode register set
  - /CAS latency (2, 2.5)
  - Burst length (2, 4, 8)
  - Wrap sequence (Sequential / Interleave)
- Automatic precharge and controlled precharge
- Auto refresh (CBR refresh) and self refresh
- x4, x8, x16 organization
- Byte write control (x4, x8) by DM
- Byte write control (x16) by LDM and UDM
- ★ 2.5 V ± 0.2 V Power supply for V_{DD}
- ★ 2.5 V ± 0.2 V Power supply for $V_{DD}Q$
- Maximum clock frequency up to 133 MHz
- SSTL_2 compatible with all signals
- 4,096 refresh cycles/64 ms
- 66-pin Plastic TSOP (II) (400 mil)
- Burst termination by Precharge command and Burst stop command

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The mark ★ shows major revised points.

★ **Ordering Information**

Part Number	Organization (word x bit x bank)	Clock frequency MHz (MAX.)	Package
μPD45D128442G5-C75-9LG	8M x 4 x 4	133	66-pin Plastic TSOP (II) (400 mil)
μPD45D128442G5-C80-9LG		125	
μPD45D128842G5-C75-9LG	4M x 8 x 4	133	
μPD45D128842G5-C80-9LG		125	
μPD45D128164G5-C75-9LG	2M x 16 x 4	133	
μPD45D128164G5-C80-9LG		125	

Part Number

[x4, x8]

μPD45D128 842 G5 - C80

- NEC Memory
- Synchrounous DRAM
- Data rate
  - D: Double
- Capacity
  - 128: 128M bits
- Organization
  - 4: x4
  - 8: x8
- Number of Banks
  - 4: 4Bank
- Interface
  - 2: SSTL_2
- Package
  - G5: TSOP (II)
- V_{DD}
  - C: 2.5 V
- ★ Minimum Cycle time
  - 75: 7.5 ns (133MHz)
  - 80: 8 ns (125MHz)

[x16]

164

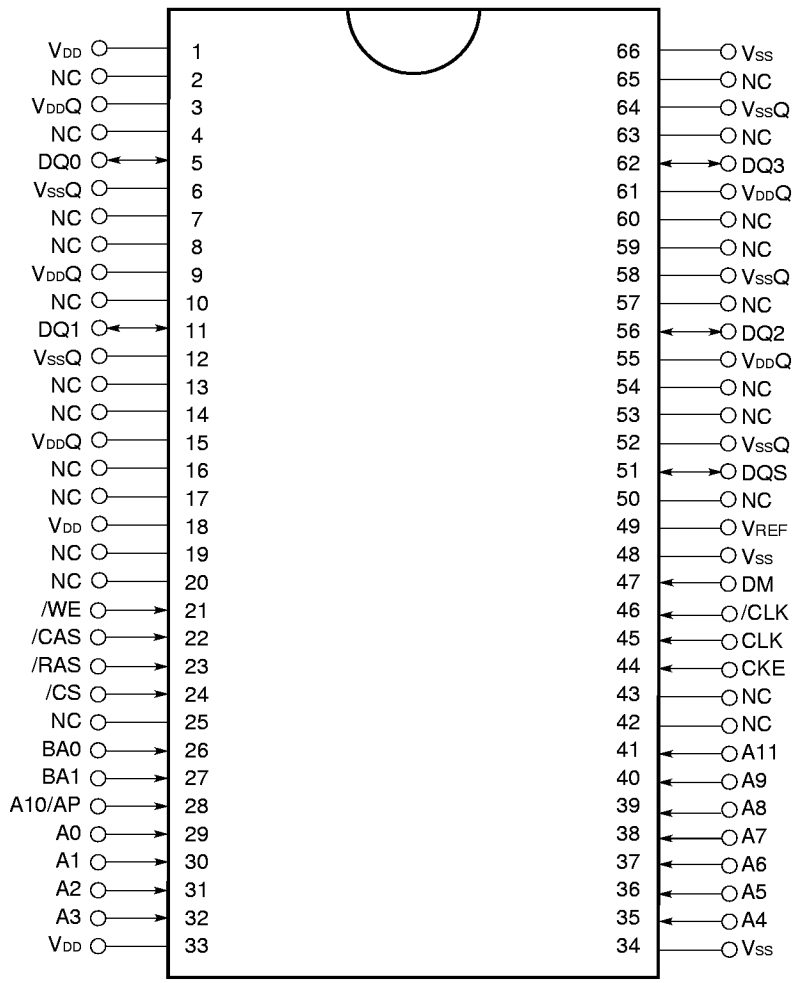
- Organization
  - 16: x16
- Number of Banks and Interface
  - 4: 4Bank, SSTL_2

Pin Configuration

[μPD45D128442]

66-pin Plastic TSOP (II) (400mil)

8M word x 4 bit x 4 bank

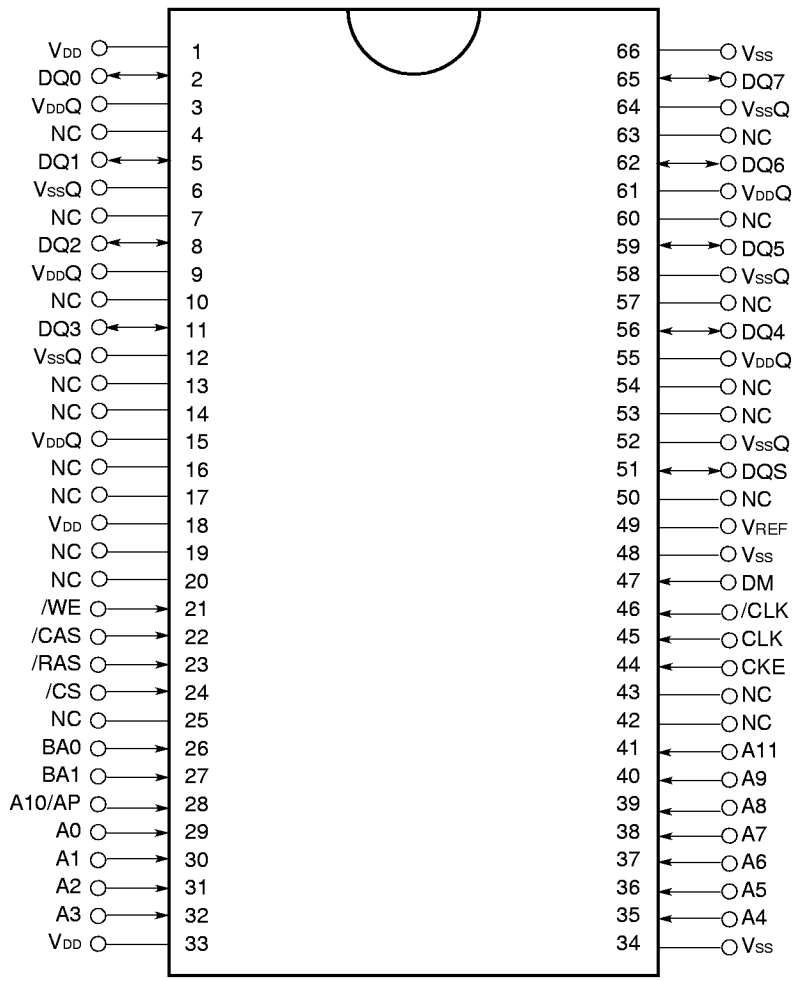


A0 - A11	: Address inputs
A0 - A11	: Row address inputs
A0 - A9, A11	: Column address inputs
BA0, BA1	: Bank select
DQ0 - DQ3	: Data inputs/outputs
DQS	: Data strobe
CLK, /CLK	: System clock input
CKE	: Clock enable
/CS	: Chip select
/RAS	: Row address strobe
/CAS	: Column address strobe
/WE	: Write enable
DM	: DQ write mask enable
V_{DD}	: Supply voltage
V_{SS}	: Ground
$V_{DD}Q$	: Supply voltage for DQ and DQS
$V_{SS}Q$	: Ground for DQ and DQS
V_{REF}	: Input reference
NC	: No connection

[μPD45D128842]

66-pin Plastic TSOP (II) (400mil)

4M word x 8 bit x 4 bank

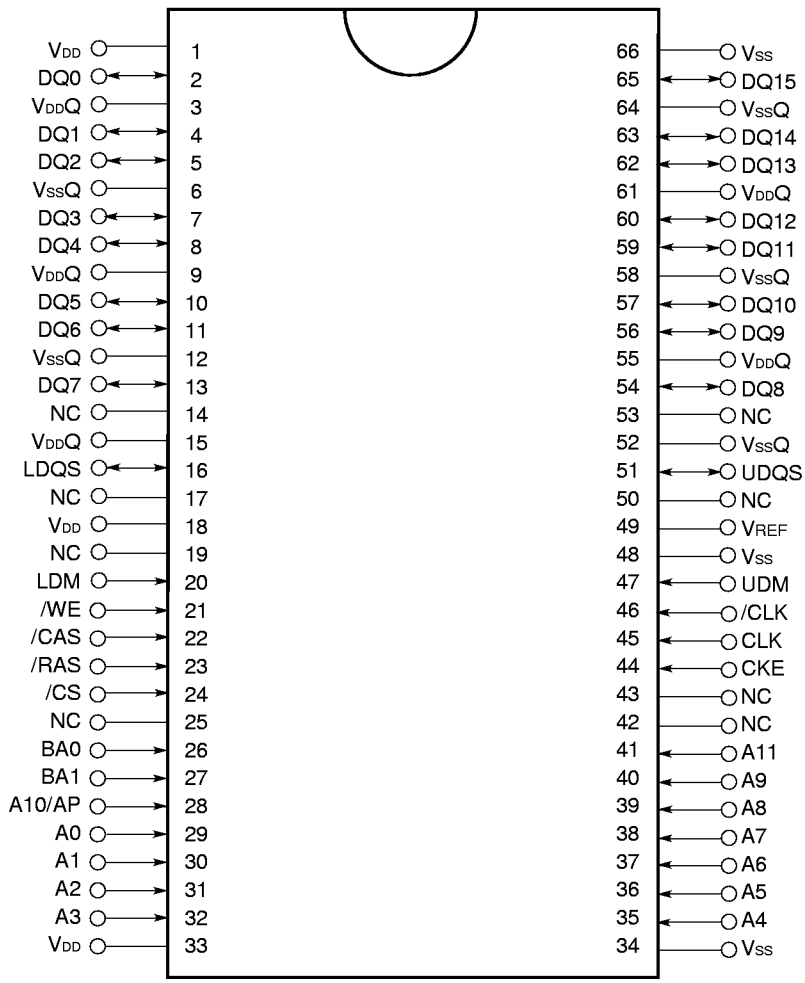


A0 - A11	: Address inputs
A0 - A11	: Row address inputs
A0 - A9	: Column address inputs
BA0, BA1	: Bank select
DQ0 - DQ7	: Data inputs/outputs
DQS	: Data strobe
CLK, /CLK	: System clock input
CKE	: Clock enable
/CS	: Chip select
/RAS	: Row address strobe
/CAS	: Column address strobe
/WE	: Write enable
DM	: DQ write mask enable
V_{DD}	: Supply voltage
V_{SS}	: Ground
$V_{DD}Q$	: Supply voltage for DQ and DQS
$V_{SS}Q$	: Ground for DQ and DQS
V_{REF}	: Input reference
NC	: No connection

[μPD45D128164]

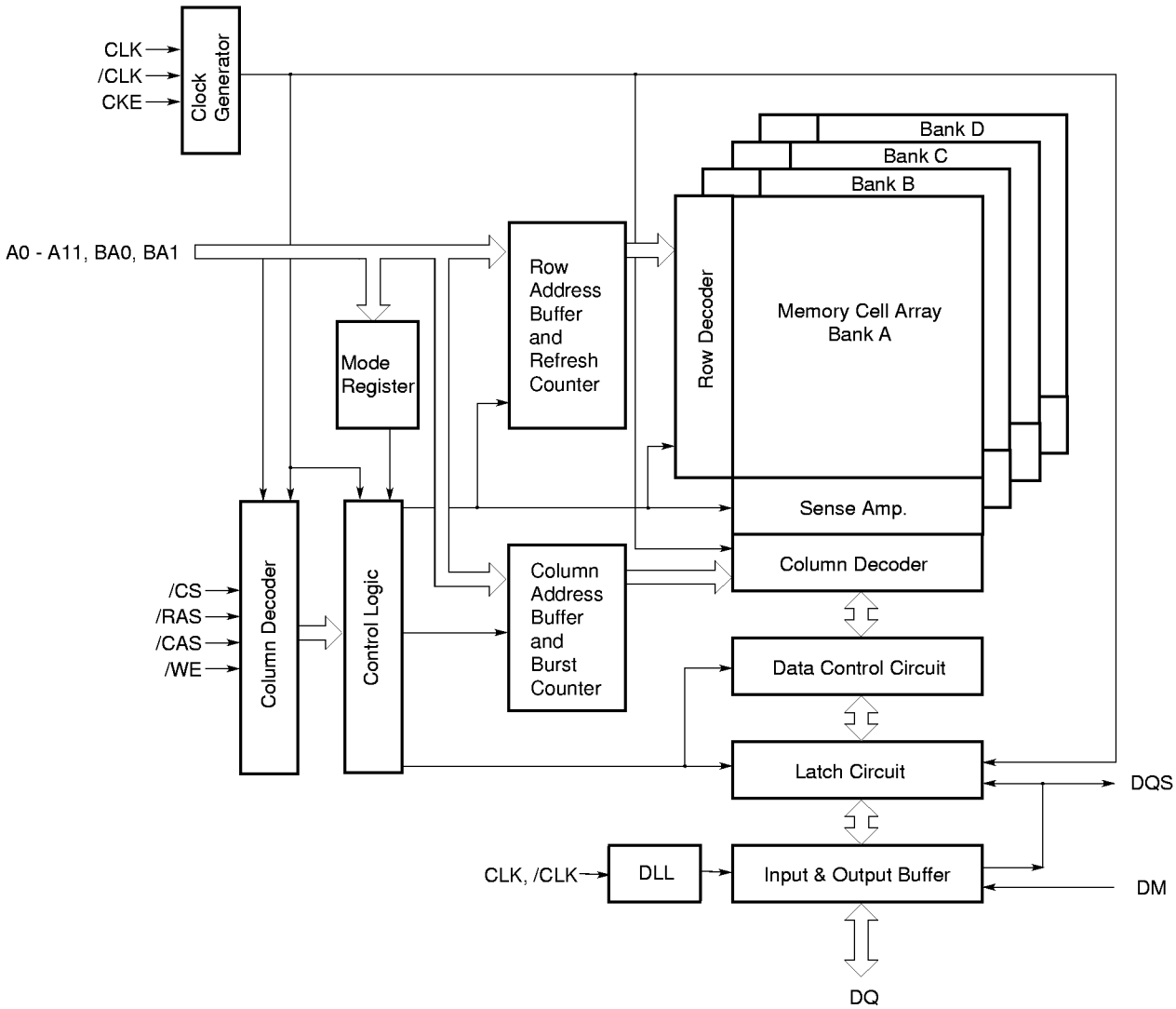
66-pin Plastic TSOP (II) (400mil)

2M word x 16bit x 4 bank



A0 - A11 : Address inputs
A0 - A11 : Row address inputs
A0 - A8 : Column address inputs
BA0, BA1 : Bank select
DQ0 - DQ15 : Data inputs/outputs
LDQS, UDQS : Data strobe
CLK, /CLK : System clock input
CKE : Clock enable
/CS : Chip select
/RAS : Row address strobe
/CAS : Column address strobe
/WE : Write enable
LDM, UDM : DQ write mask enable
VDD : Supply voltage
VSS : Ground
VDDQ : Supply voltage for DQ, LDQS and UDQS
VSSQ : Ground for DQ, LDQS and UDQS
VREF : Input reference
NC : No connection

Block Diagram



CONTENTS

1. Input/Output Pin Function

	Pin name	Input/Output	Function
★	CLK, /CLK	Input	CLK and /CLK are the master clock inputs. The timing reference point for the differential clock is when CLK and /CLK cross. All control and address inputs except for DQ and DM are latched by a rising edge of CLK. By both of rising and falling edges of CLK, output DQ and DQS are validated.
★	CKE	Input	CKE controls power down mode. When the μPD45D128xxx is not in burst mode and CKE is negated, the device enters power down mode and deactivates internal clock signals, input buffers and output drivers. During power down mode, CKE must remain low.
	/CS	Input	/CS low starts a command input cycle. When /CS is high, commands are ignored but the current operations will be continued.
	/RAS, /CAS, /WE	Input	As well as regular SDRAMs, each combination of /RAS, /CAS, and /WE input in conjunction with /CS input at a rising edge of CLK determines SDRAM operation. Refer to the command table.
	A0 – A11	Input	Row address is determined by A0 - A11 at the rising edge of CLK in active command cycle. It does not depend on the bit organization. Column address is determined by A0 - A9, A11 at the rising edge of CLK in read or write command cycle. It depends on the bit organization: A0 - A9, A11 for x4 device, A0 - A9 for x8 device, A0 - A8 for x16 device. A10 defines precharge mode. When A10 is high in precharge command cycle, all banks are precharged; when A10 is low, only the bank selected by BA0 and BA1 is precharged. When A10 is high in read or write command cycle, precharge starts automatically after the burst access.
★	BA0, BA1	Input	BA0, BA1 are bank select signals. In command cycle, BA0 and BA1 low select Bank A, BA0 high and BA1 low select bank B, BA0 low and BA1 high select bank C and then BA0 and BA1 high select bank D.
	DQ0 – DQ15	Input/Output	DQ pins have the same function as I/O pins on conventional DRAMs.
	DQS, LDQS, UDQS	Input/Output	Active on the both edges for data input and output.
	DM, LDM, UDM	Input	DM's are latched by both of rising and falling edges of the DQS. In write mode, DM's control byte mask. Unlike regular SDRAMs, DM's do not control read operation.
	V_{REF}	Input	V_{REF} is reference voltage for SSTL input buffers.
	V_{DD}, $V_{DD}Q$, V_{SS}, $V_{SS}Q$	(Power Supply)	V_{DD} and V_{SS} are power supply pins for internal circuits. $V_{DD}Q$ and $V_{SS}Q$ are power supply pins for the output buffers.

2. Commands

Extended mode register set command

(/CS, /RAS, /CAS, /WE Low)

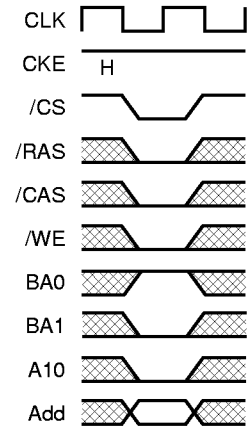
The μPD45D128xxx has an extended mode register that defines enabling or disabling DLL. In this command, A0 through A11, BA0 and BA1 are the data input pins.

After power on, the extended mode register set command must be executed to enabling or disabling DLL.

The extended mode register can be set only when all banks are in idle state.

★ During t_{MRD}, the μPD45D128xxx can not accept any other commands.

Fig.1 Extended mode register set command



Mode register set command

(/CS, /RAS, /CAS, /WE Low)

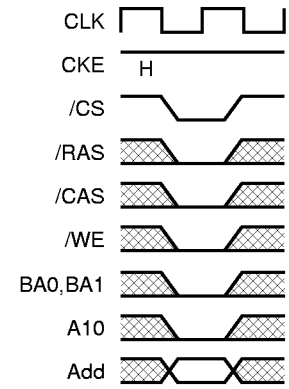
The μPD45D128xxx has a mode register that defines how the device operates. In this command, A0 through A11, BA0 and BA1 are the data input pins.

After power on, the mode register set command must be executed to initialize the device.

The mode register can be set only when all banks are in idle state.

★ During t_{MRD}, the μPD45D128xxx can not accept any other commands.

Fig.2 Mode register set command



Bank activate command

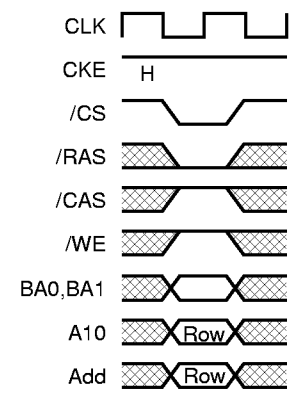
(/CS, /RAS = Low, /CAS, /WE = High)

The μPD45D128xxx has four banks, each with 4,096 rows.

This command activates the bank and the row address selected by BA0 and BA1, and by A0 through A11 respectively.

This command corresponds to a conventional DRAM's /RAS falling.

Fig.3 Bank activate command



Precharge command

(/CS, /RAS, /WE= Low, /CAS = High)

This command begins precharge operation of the bank selected by BA0, BA1 and A10. When A10 is High, all banks are precharged, regardless of BA0 and BA1.

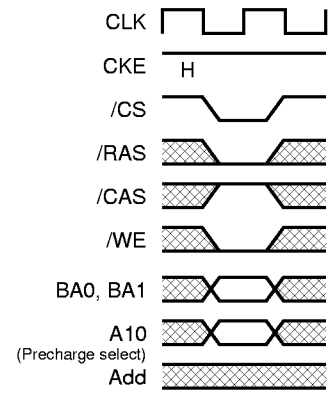
When A10 is Low, only the bank selected by BA0 and BA1 is precharged.

After this command, the μPD45D128xxx can't accept the activate command to the precharging bank during t_{RP} (precharge to activate command period).

This command can terminate the current burst operation.

This command corresponds to a conventional DRAM's /RAS rising.

Fig.4 Precharge command



Read command

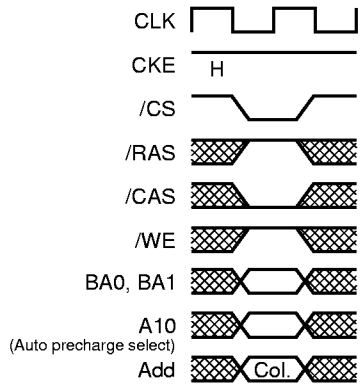
(/CS, /CAS = Low, /RAS, /WE = High)

This command begins the burst read operation. The bank and the burst start column address are selected by BA0 and BA1 and by A0 through A11 respectively.

Read data is available after /CAS latency requirements which have been met.

And it is synchronized with DQS.

Fig.5 Read command



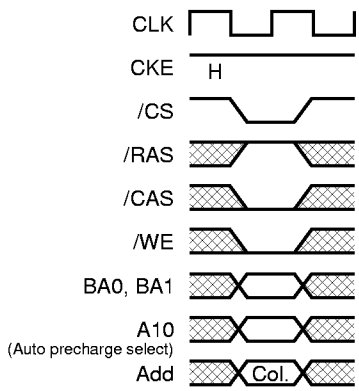
Write command

(/CS, /CAS, /WE = Low, /RAS = High)

This command begins burst write operation. The bank and the burst start column address are selected by BA0 and BA1 and by A0 through A11 respectively.

Write data must be input by DQ0 through DQ15. Byte mask data must be input by DM, LDM, and UDM. Both data must be synchronized with DQS that is inputted after this command.

Fig.6 Write command



CBR (auto) refresh command

(/CS, /RAS, /CAS = Low, /WE, CKE = High)

This command is a request to begin the CBR (auto) refresh operation.

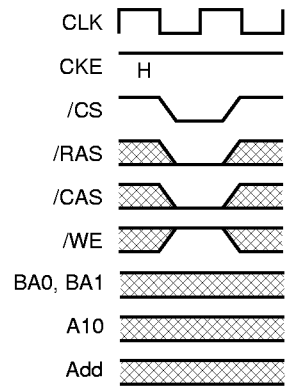
The refresh address is generated internally.

Before executing CBR (auto) refresh, all banks must be precharged.

After this cycle, all banks will be in the idle (precharged) state and ready for a bank activate command.

★ During t_{RFC} (refresh command to refresh or activate command period), the μPD45D128xxx cannot accept any other command.

Fig.7 CBR (auto) refresh command



Self refresh entry command

(/CS, /RAS, /CAS, CKE = Low, /WE = High)

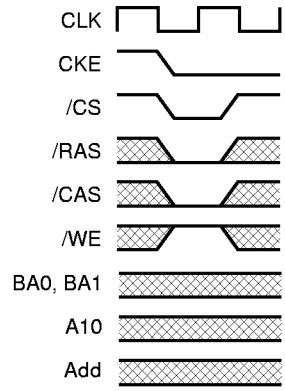
After the command execution, self refresh operation continues while CKE remains low.

When CKE goes high, the μPD45D128xxx will exit the self refresh mode.

During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.

Before executing self refresh, all banks must be precharged.

Fig.8 Self refresh entry command

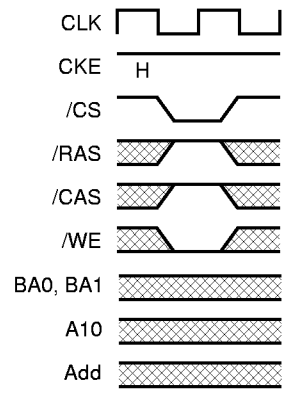


Burst stop command

(/CS, /WE = Low, /RAS, /CAS = High)

This command can stop the current read burst operation.

Fig.9 Burst stop command

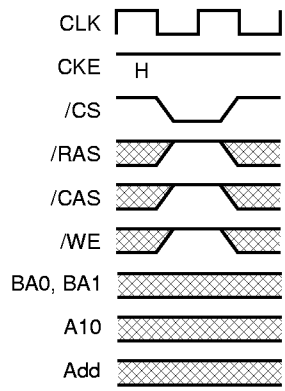


No operation

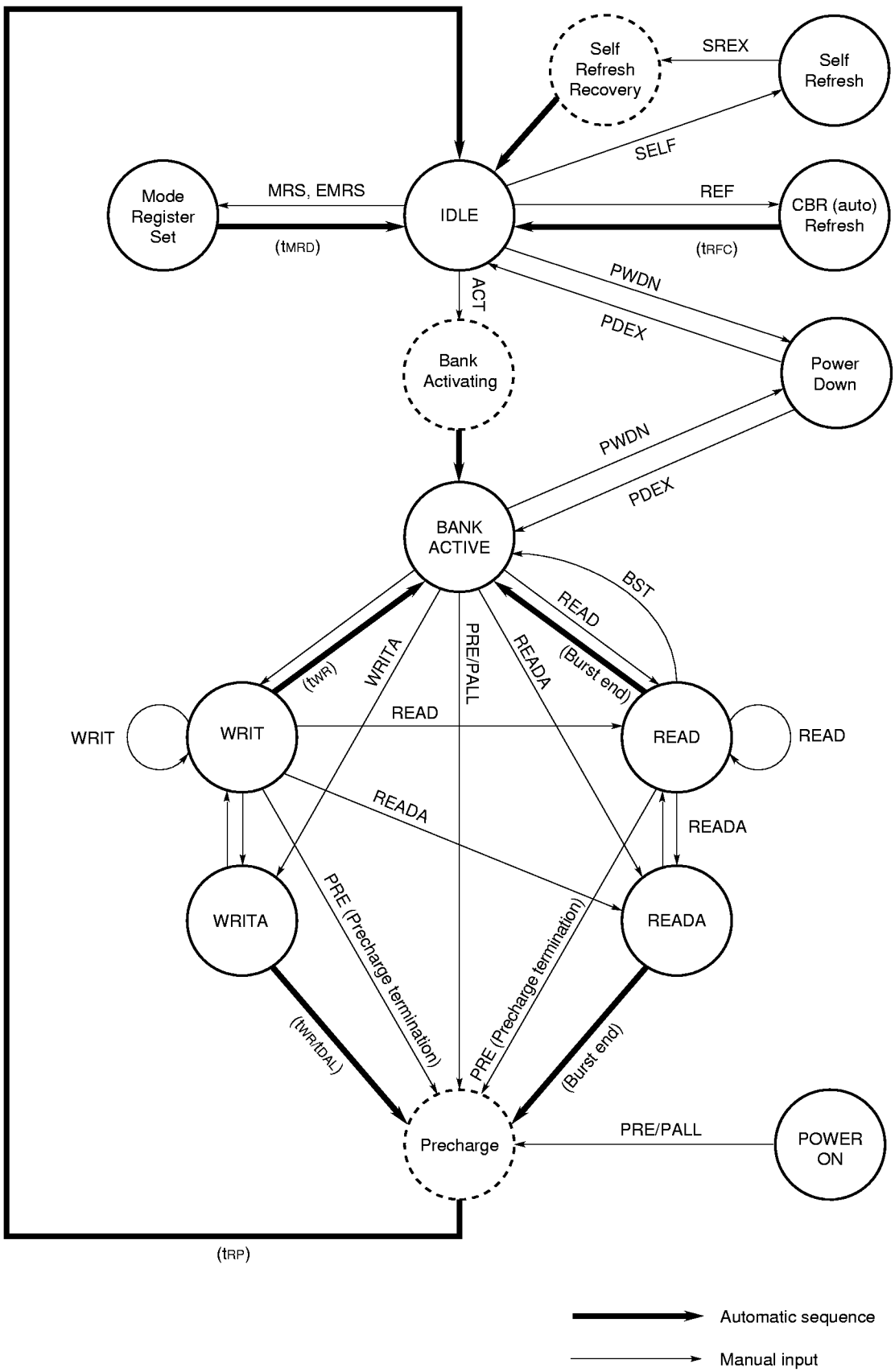
(/CS = Low, /RAS, /CAS, /WE = High)

This command is not an execution command.
This command doesn't begin or terminate any operation.

Fig.10 No operation



★ 3. Simplified State Diagram



4. Truth Table

4.1 Command Truth Table

★

Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	Address			
		n-1	n					BA0	BA1	A10	A0-9,A11
Device deselect	DESL	H	x	H	x	x	x	x		x	x
No operation	NOP	H	x	L	H	H	H	x		x	x
Burst stop	BST	H	x	L	H	H	L	x		x	x
Read	READ	H	x	L	H	L	H	V		L	V
Read with auto precharge	READA									H	
Write	WRIT	H	x	L	H	L	L	V		L	V
Write with auto precharge	WRITA									H	
Bank active	ACT	H	x	L	L	H	H	V			
Prechrage select bank	PRE	H	x	L	L	H	L	V		L	x
Precharge all banks	PALL							x		H	x
Mode register set	MRS	H	x	L	L	L	L	L	L	L	V
Extended mode register set	EMRS							H	L	L	V

4.2 DM Truth Table

Function	Symbol	CKE		DM	
		n-1	n	U	L
Data write enable	ENB	H	x	L	
Data mask	MASK	H	x	H	
Upper byte write enable	ENBU	H	x	L	x
Lower byte write enable	ENBL	H	x	x	L
Upper byte write inhibit	MASKU	H	x	H	x
Lower byte write inhibit	MASKL	H	x	x	H

★ 4.3 CKE Truth Table

Current State	Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	Address
			n-1	n					
Idle	CBR (auto) refresh command	REF	H	H	L	L	L	H	x
Idle	Self refresh entry	SELF	H	L					
Self refresh	Self refresh exit	SREX	L	H	H	x	x	x	x
					L	H	H	x	x
Idle	Power down entry	PWDN	H	L	H	x	x	x	x
					L	H	H	x	x
Bank(s) active	Power down entry	PWDN	H	L	H	x	x	x	x
					L	H	H	x	x
Power down	Power down exit	PDEX	L	H	H	x	x	x	x
					L	H	H	x	x

Remark H = High level, L = Low level, V = Valid, x = High or Low level (Don't care)

4.4 Operative Command Table [Note1]

(1/3)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Idle	H	x	x	x	x	DESL	Nop or Power down	
	L	H	H	H	x	NOP	Nop or Power down	
	L	H	H	L	x	BST	ILLEGAL	2
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	Bank activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	3
	L	L	L	H	x	REF/SELF	CBR (auto) refresh or Self refresh	4
	L	L	L	L	Op-Code	MRS	Mode register set	4
	L	L	L	L	Op-Code	EMRS	Extended mode register set	4
Row active	H	x	x	x	x	DESL	Nop	
	L	H	H	H	x	NOP	Nop	
	L	H	H	L	x	BST	ILLEGAL	2
	L	H	L	H	BA, CA, A10	READ/READA	Begin read/read with AP	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write/write with AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Precharge/Precharge all banks	5
★	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	L	L	L	L	Op-Code	EMRS	ILLEGAL	
Read	H	x	x	x	x	DESL	Nop (Row active after burst end)	
	L	H	H	H	x	NOP	Nop (Row active after burst end)	
	L	H	H	L	x	BST	terminate burst, Row active	6
	L	H	L	H	BA, CA, A10	READ/READA	terminate burst, Begin new read/ read with AP	6
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	terminate burst, Precharge/Precharge all banks	6
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	L	L	L	L	Op-Code	EMRS	ILLEGAL	
★ Write	H	x	x	x	x	DESL	Nop (Row active after t_{WR})	
★	L	H	H	H	x	NOP	Nop (Row active after t_{WR})	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	terminate burst, Begin read/read with AP	6
	L	H	L	L	BA, CA, A10	WRIT/WRITA	terminate burst, Begin new write/ write with AP	6
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	terminate burst, Precharge/Precharge all banks	6
★	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	L	L	L	L	Op-Code	EMRS	ILLEGAL	

(2/3)

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Read with auto precharge	H	x	x	x	x	DESL	Nop (Precharge after burst end)	
	L	H	H	H	x	NOP	Nop (Precharge after burst end)	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	L	L	L	L	Op-Code	EMRS	ILLEGAL	
Write with auto precharge	H	x	x	x	x	DESL	Nop (Idle after t_{DAL})	
	L	H	H	H	x	NOP	Nop (Idle after t_{DAL})	
	L	H	H	L	x	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	L	L	L	L	Op-Code	EMRS	ILLEGAL	
Precharge	H	x	x	x	x	DESL	Nop (Idle after t_{RP})	
	L	H	H	H	x	NOP	Nop (Idle after t_{RP})	
	L	H	H	L	x	BST	ILLEGAL	2
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Nop (Idle after t_{RP})	3
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	L	L	L	L	Op-Code	EMRS	ILLEGAL	
Row activating	H	x	x	x	x	DESL	Nop (Row active after t_{RCD})	
	L	H	H	H	x	NOP	Nop (Row active after t_{RCD})	
	L	H	H	L	x	BST	ILLEGAL	2
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	x	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
	L	L	L	L	Op-Code	EMRS	ILLEGAL	

(3/3)

	Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
★	Write recovering	H	x	x	x	x	DESL	Nop (Row active after t_{WR})	
★		L	H	H	H	x	NOP	Nop (Row active after t_{WR})	
★		L	H	H	L	x	BST	Nop (Row active after t_{WR})	
		L	H	L	H	BA, CA, A10	READ/READA	Begin read/read with AP	
		L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin new write/write with AP	
		L	L	H	H	BA, RA	ACT	ILLEGAL	2
		L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
		L	L	L	H	x	REF/SELF	ILLEGAL	
		L	L	L	L	Op-Code	MRS	ILLEGAL	
		L	L	L	L	Op-Code	EMRS	ILLEGAL	
	Write recovering with auto precharge	H	x	x	x	x	DESL	Nop (Idle after t_{DAL})	
		L	H	H	H	x	NOP	Nop (Idle after t_{DAL})	
		L	H	H	L	x	BST	ILLEGAL	
		L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
		L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
		L	L	H	H	BA, RA	ACT	ILLEGAL	2
		L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
		L	L	L	H	x	REF/SELF	ILLEGAL	
		L	L	L	L	Op-Code	MRS	ILLEGAL	
		L	L	L	L	Op-Code	EMRS	ILLEGAL	
★	Refresh	H	x	x	x	x	DESL	Nop (Idle after t_{RFC})	
★		L	H	H	H	x	NOP	Nop (Idle after t_{RFC})	
★		L	H	H	L	x	BST	Nop (Idle after t_{RFC})	2
		L	H	L	x	x	READ/WRIT	ILLEGAL	2
		L	L	H	x	x	ACT/PRE/PALL	ILLEGAL	3
		L	L	L	x	x	REF/SELF/MRS/EMRS	ILLEGAL	
★	Mode register accessing	H	x	x	x	x	DESL	Nop (Idle after t_{MRD})	
★		L	H	H	H	x	NOP	Nop (Idle after t_{MRD})	
		L	H	H	L	x	BST	ILLEGAL	2
		L	H	x	x	x	READ/WRIT	ILLEGAL	2
		L	L	x	x	x	ACT/PRE/PALL/REF/SELF/MRS/EMRS	ILLEGAL	2

Remark H = High level, L = Low level, x = High or Low level (Don't care),
BA = Bank address, RA = Row address, CA = Column address, A10 = Precharge control address,
Op-Code = Operand code, Nop = No operation, AP = Auto precharge,
ILLEGAL = Device operation and/or data-integrity are not guaranteed

Notes 1. All entries assume that CKE was active (High level) during the preceding clock cycle and the current clock cycle.

2. ILLEGAL to bank in specified states; function may be legal in the bank indicated by BA0, BA1 depending on the state of that bank.

3. Nop to bank precharging or in idle state. May precharge bank indicated by BA0, BA1.

4. ILLEGAL if any bank is not idle.

5. ILLEGAL if t_{RAS} is not satisfied.

6. Must satisfy command interval and/or burst terminate condition.

4.5 Command Truth Table for CKE

	Current State	CKE		/CS	/RAS	/CAS	/WE	Add	Command	Action	Notes
		n-1	n								
	Self refresh	H	x	x	x	x	x	x		ILLEGAL(Impossible)	
★		L	H	H	x	x	x	x	SREX	Exit S.R, self refresh recovery	2
				L	H	H	x	x			
		L	L	x	x	x	x	x		Maintain self refresh	
	Self refresh recovery	H	H	H	x	x	x	x	DESL	Nop (Idle after t_{RC})	
		H	H	L	H	H	H	x	NOP	Nop (Idle after t_{RC})	
		H	L	x	x	x	x	x		ILLEGAL	
		L	x	x	x	x	x	x		ILLEGAL (Impossible)	
	Power down	H	x	x	x	x	x	x		ILLEGAL (Impossible)	
★		L	H	H	x	x	x	x	PDEX	Exit power down, Idle	
				L	H	H	x	x			
		L	L	x	x	x	x	x		Maintain power down	
	All banks idle	H	H	V	V	V	V	x		Refer to operative command table	
		H	L	H	x	x	x	x	PWDN	Power down entry	1
		H	L	L	H	H	H	x	PWDN	Power down entry	1
		H	L	L	x	x	L	x		ILLEGAL	
		H	L	L	H	L	x	x		ILLEGAL	
		H	L	L	L	H	x	X		ILLEGAL	
		H	L	L	L	L	H	X	SELF	Self refresh entry	1
★		L	X	x	x	x	x	x		Power down	
	Row active	H	x	x	x	x	x	x		Refer to operative command table	
		L	x	x	x	x	x	x		Power down	1
	Any state except listed above	H	H	V	V	V	V	V		Refer to operative command table	
		H	L	x	x	x	x	x		ILLEGAL	
		L	x	x	x	x	x	x		ILLEGAL (Impossible)	

Remark H = High level, L = Low level, x = High or Low level (Don't care), V = Valid,
Add = Address (A0 - A11, BA0, BA1),
ILLEGAL = Device operation and/or data-integrity are not guaranteed

Notes 1. Self refresh can be entered only from all banks idle state.
Power down can be entered only from all banks idle or row active state.

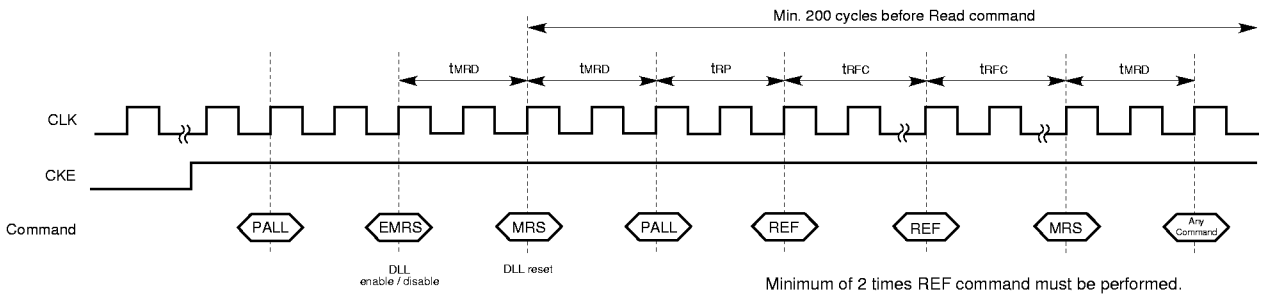
2. CKE low to high transition will re-enable CLK and other inputs asynchronously.
A Minimum setup time must be satisfied before any command other than exit.

★ 5. Initialization

The μPD45D128xxx is initialized in the power-on sequence according to the following.

(1) Power must first be applied to V_{DD}, then $V_{DD}Q$, and finally to V_{REF}. V_{TT} must be applied.
(2) Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS output will be in Hi-Z state.
(3) To stabilize internal circuits, when power is applied a 100 μs or longer pause must precede any signal toggling.
(4) After the pause, all banks must be precharged using precharge command. The precharge all banks command is convenient.
(5) EMRS command must be performed to enable or disable DLL. Then MRS command must be applied to reset DLL. After this MRS command additional 200 cycles are required before read command.
(6) All banks must be precharged using precharge command again. Then two or more CBR refresh command must be performed.
(7) After the refresh the mode register can be programmed by MRS command.

Case 1: MRS after the REF



Remark Two refresh commands may be follow the first MRS command.

6. Programming the Mode Register

The mode register is programmed by the Mode register set command using address bits BA0, BA1, A11 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has five fields;

★ Option : A11 through A9, A7
★ DLL reset : A8
/CAS latency : A6 through A4
Wrap type : A3
Burst length : A2 through A0

★ Following mode register programming, no command can be issued during t_{MRD}.

/CAS Latency

/CAS latency is the mode critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available.
The value is determined by the frequency of the clock and the speed grade of the device.

Burst Length

Burst length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become Hi-Z.
The burst length is programmable as 2, 4 and 8.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either "Sequential" or "Interleave". The method chosen will depend on the type of CPU in the system.
Some microprocessor cache system are optimized for sequential addressing and others for interleaved addressing. **7.1 Burst Length and Sequence** shows the addressing sequence for each burst length using them. Both sequences support bursts of 2, 4 and 8.

★ The extended mode register has two fields;

Option : A11 through A1
DLL enable : A0

7. Mode Register

★

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
x	x	x	x	x	0	1	V	V	V	V	V	V	V	Vender specific

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	1	0	0	0	0	0	0	0	0	0	0	0	DLL	Extended mode register set

Bit 0	DLL
0	Enable
1	Disable

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	DLL	0	LTMODE			WT	BL			Mode register set

Bit 8	DLL
0	Normal
1	Reset

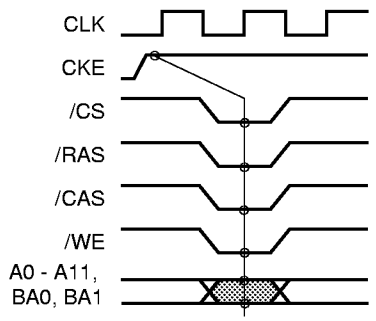
	Bit 2 - Bit 0	WT = 0	WT = 1
Burst Length	000	R	R
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	R	R

	Bit 3	Mode
Wrap Type	0	Sequential
	1	Interleave

	Bit 6 - Bit 4	/CAS Latency
Latency Mode	000	R
	001	R
	010	2
	011	R
	100	R
	101	R
	110	2.5
	111	R

Remark V = Valid, x = Don't care

Remark R: Reserved



Mode register set timming

7.1 Burst Length and Sequence

[Burst Length = Two]

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst Length = Four]

Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst Length = Eight]

Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

8. Address Bits of Bank-Select and Precharge

[Activate Command]

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
														Row Address

BA1	BA0	Result
0	0	Select Bank A, "Activate" command
0	1	Select Bank B, "Activate" command
1	0	Select Bank C, "Activate" command
1	1	Select Bank D, "Activate" command

[Precharge Command]

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
														Row Address

BA1	BA0	A10	Result
0	0	0	Precharge Bank A
0	1	0	Precharge Bank B
1	0	0	Precharge Bank C
1	1	0	Precharge Bank D
x	x	1	Precharge All Banks

Remark x = Don't care

[Read/Write Command]

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
														Column Address

A10	Result
0	Disables Auto-Precharge
1	Enables Auto-Precharge

BA1	BA0	Result
0	0	Enables Read/Write commands for Bank A
0	1	Enables Read/Write commands for Bank B
1	0	Enables Read/Write commands for Bank C
1	1	Enables Read/Write commands for Bank D

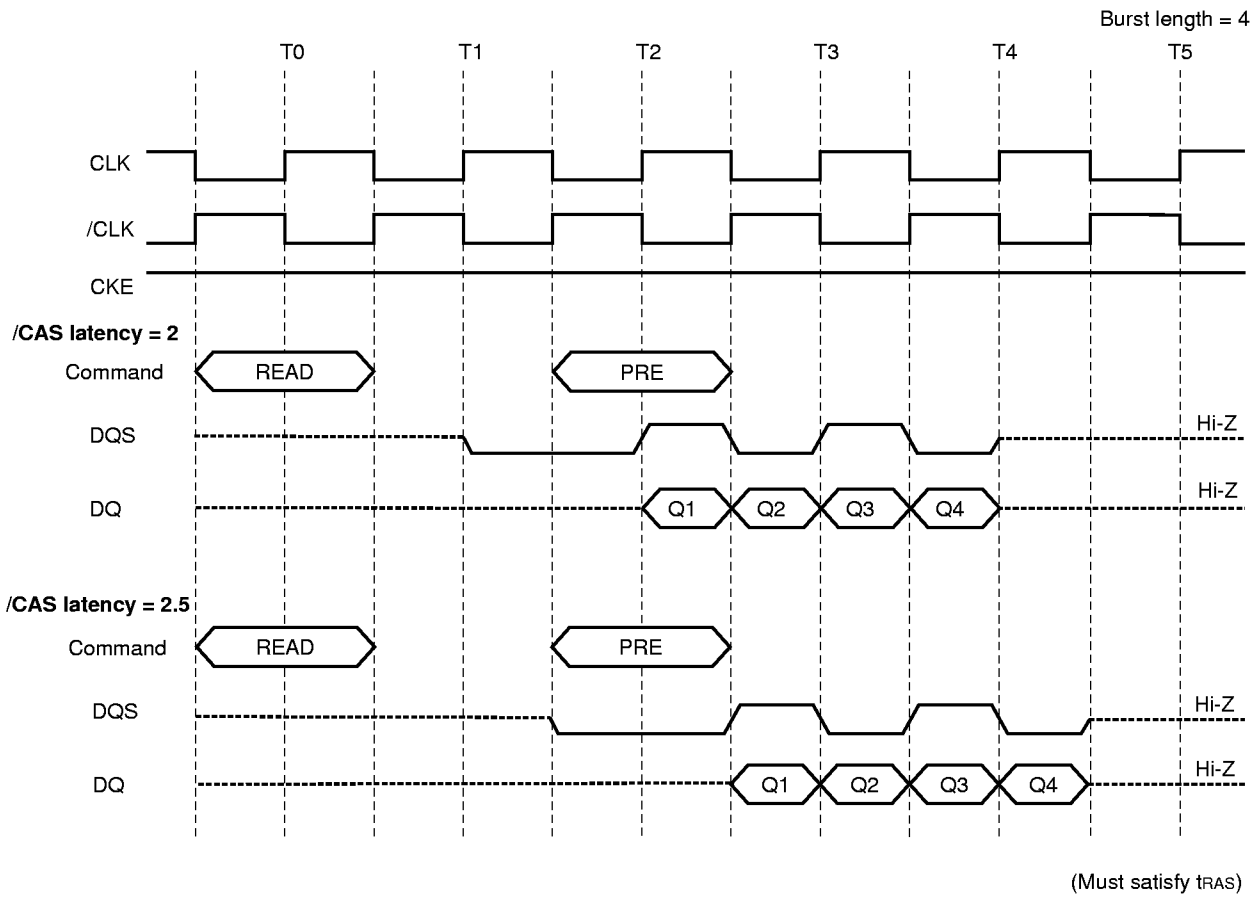
9. Precharge

9.1 Read to Precharge Command Interval

The precharge command can be issued anytime after $t_{RAS\ (MIN.)}$ is satisfied. Soon after the precharge command is issued, precharge operation performed and the DDR SDRAM enters the idle state after t_{RP} is satisfied. The parameter t_{RP} is the time required to perform the precharge.

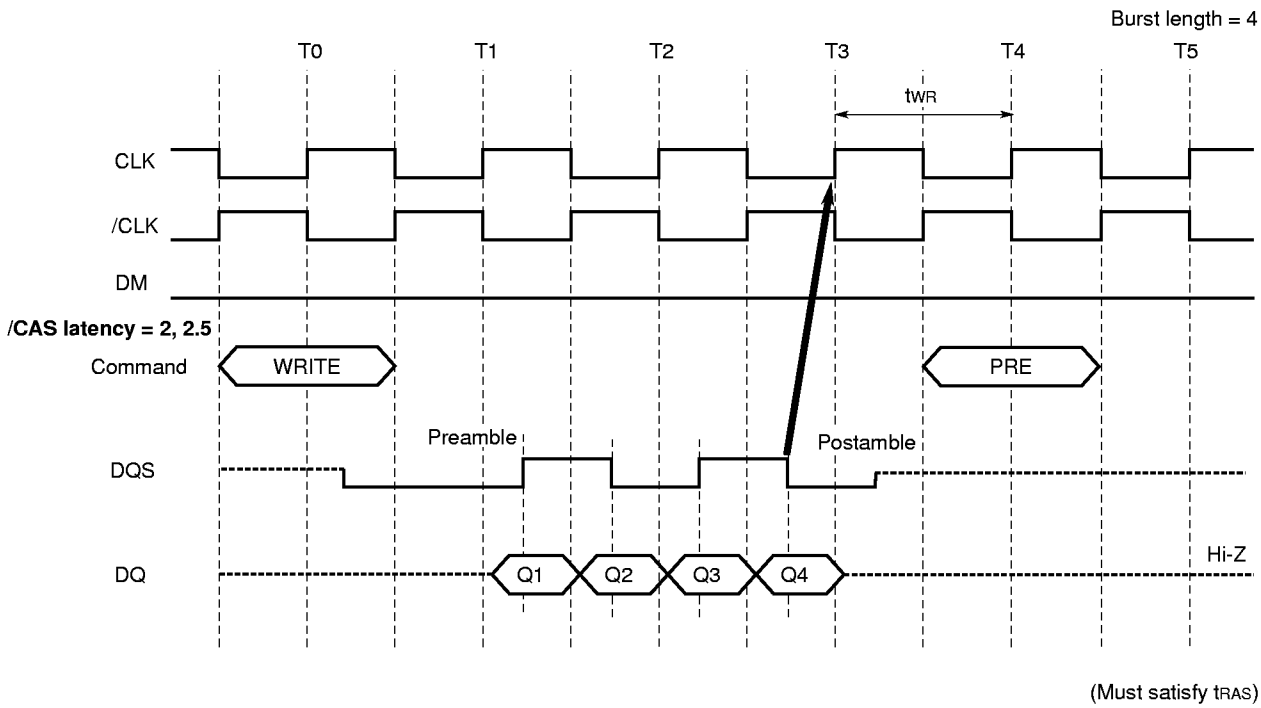
The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is as follows.

/CAS latency = 2 : (burst length/2) clocks after the read command is issued.
/CAS latency = 2.5 : (burst length/2) clocks after the read command is issued.



★ 9.2 Write to Precharge Command Interval

In order to write all burst data to the memory cell correctly, the asynchronous parameter t_{WR} must be satisfied. The t_{DPL} specification defines the earliest time that a precharge command can be issued.



(Must satisfy t_{RAS})

10. Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the read or write command (read with auto precharge command or write with auto precharge command), auto precharge is selected and begin automatically.

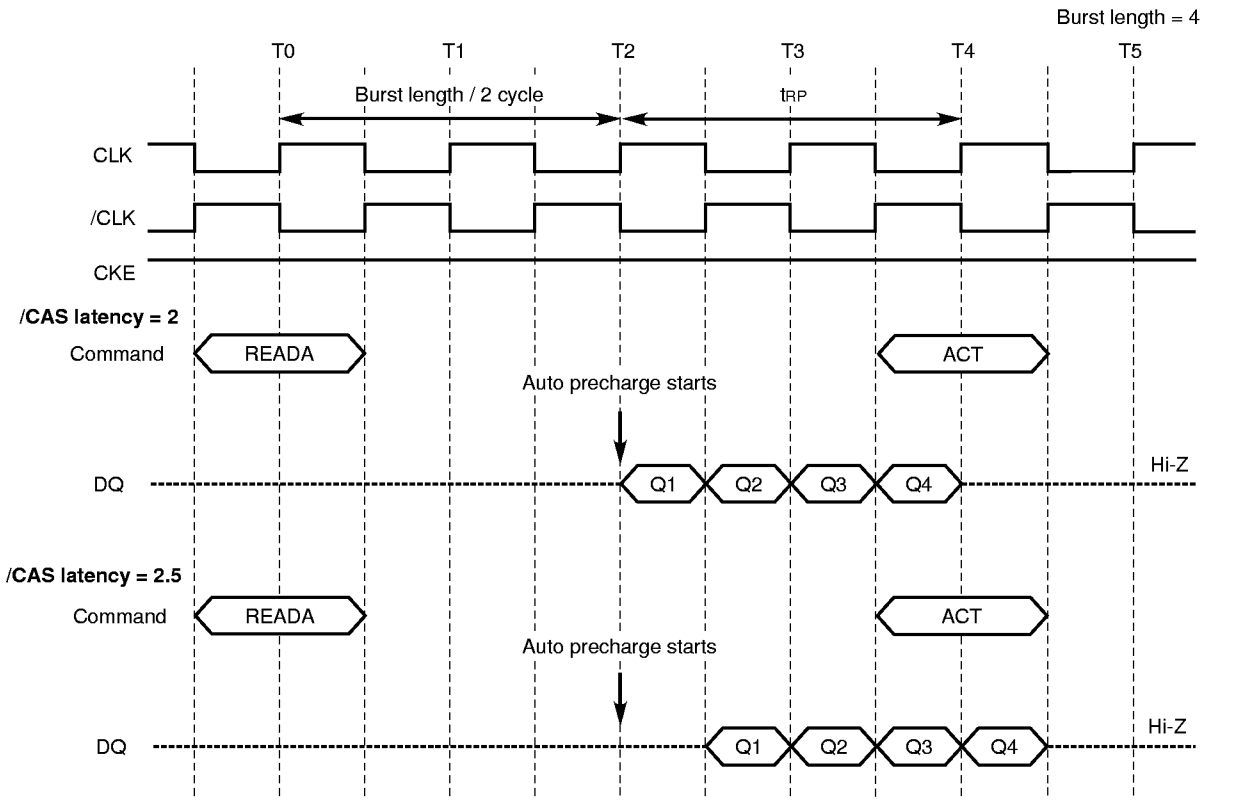
The t_{RAS} must be satisfied with a read with auto precharge or a write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends.

In read cycle, once auto precharge has started, an activate command to the bank can be issued after t_{RP} has been satisfied.

In write cycle, the t_{DAL} must be satisfied to issue the next activate command to the bank being precharged.

10.1 Read with Auto Precharge

When a read with auto precharge command is issued, the auto precharge begins (Burst length / 2) clocks later from a read with auto precharge command.

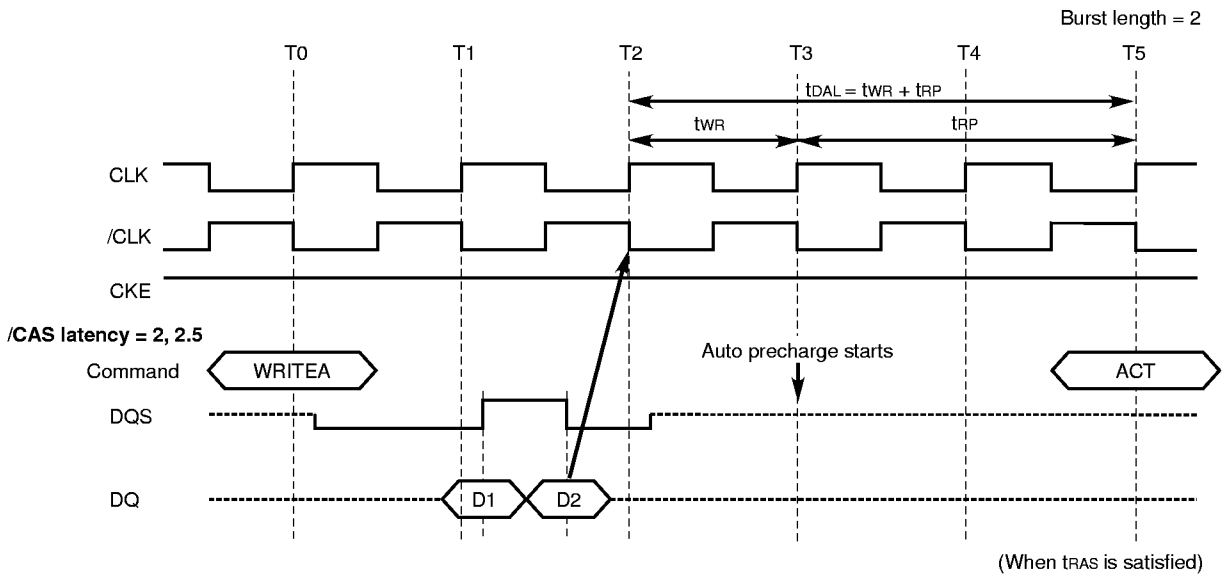


(When t_{RAS} is satisfied)

Remark READA means Read with Auto Precharge command

★ 10.2 Write with Auto Precharge

When a write with auto precharge command is issued, the auto precharge begins after t_{WR} is satisfied.



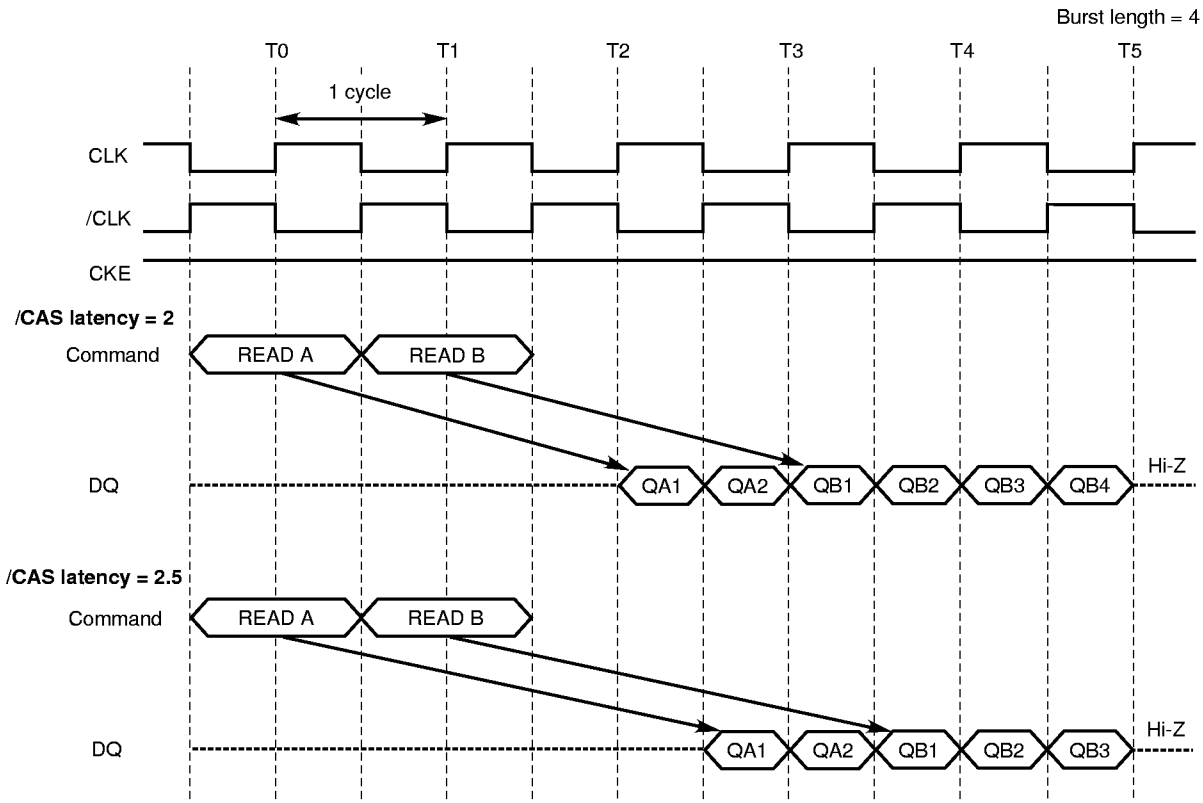
Remark WRITEA means Write with Auto Precharge command

11. Read/Write Command Interval

11.1 Read to Read Command Interval

During a read cycle, when new read command is issued, it will be effective after /CAS latency, even if the previous read operation does not completed. READ will be interrupted by another READ.

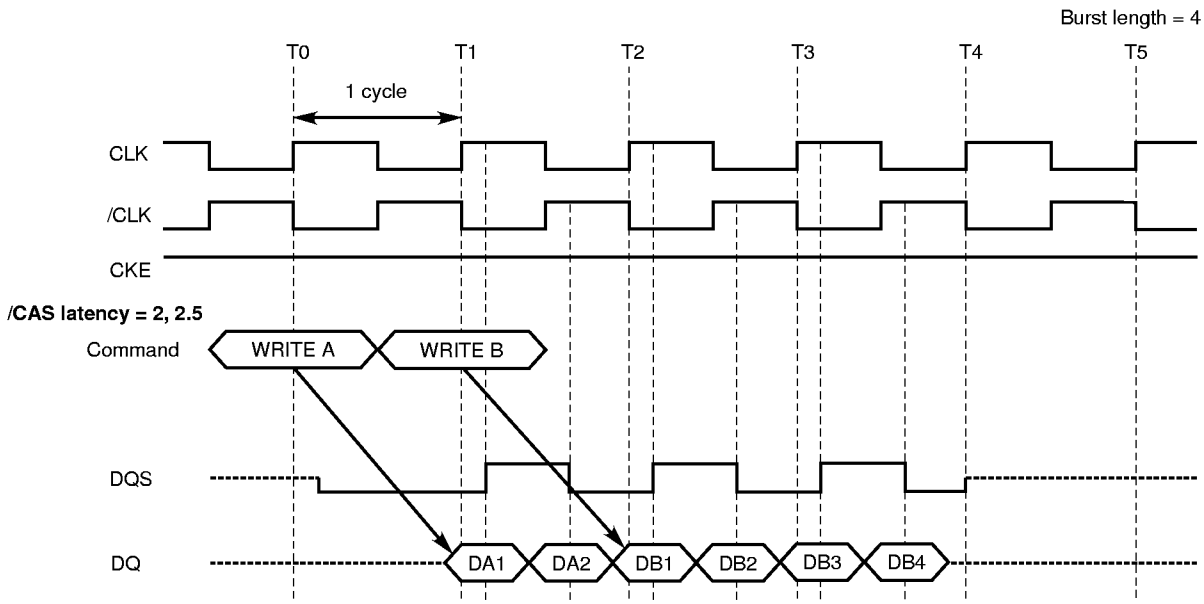
The interval between commands is minimum 1 cycle. Each read command can be issued in every clock without any restriction.



11.2 Write to Write Command Interval

During a write cycle, when new write command is issued, the previous burst will terminate and the new burst will begin with new write command. WRITE will be interrupted by another WRITE.

The interval between commands is minimum 1 cycle. Each write command can be issued in every clock without any restriction.

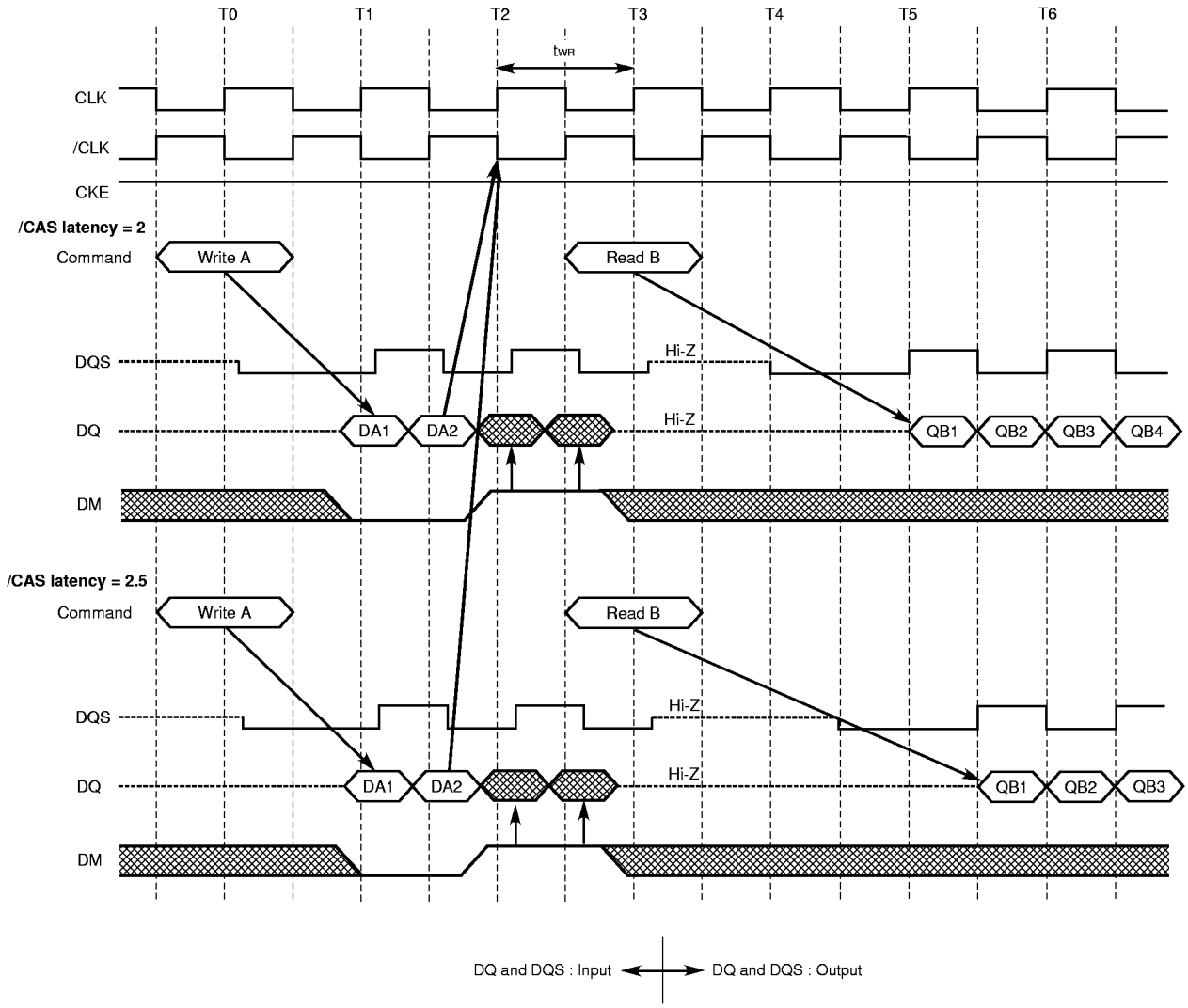


★ 11.3 Write to Read Command Interval

The burst write operation can be interrupted by read command of any bank. The data bus must be high impedance at least 1 cycle prior to the first output data.

The minimum time interval between the rising clock edge after the last input data and the read command is t_{WR}.

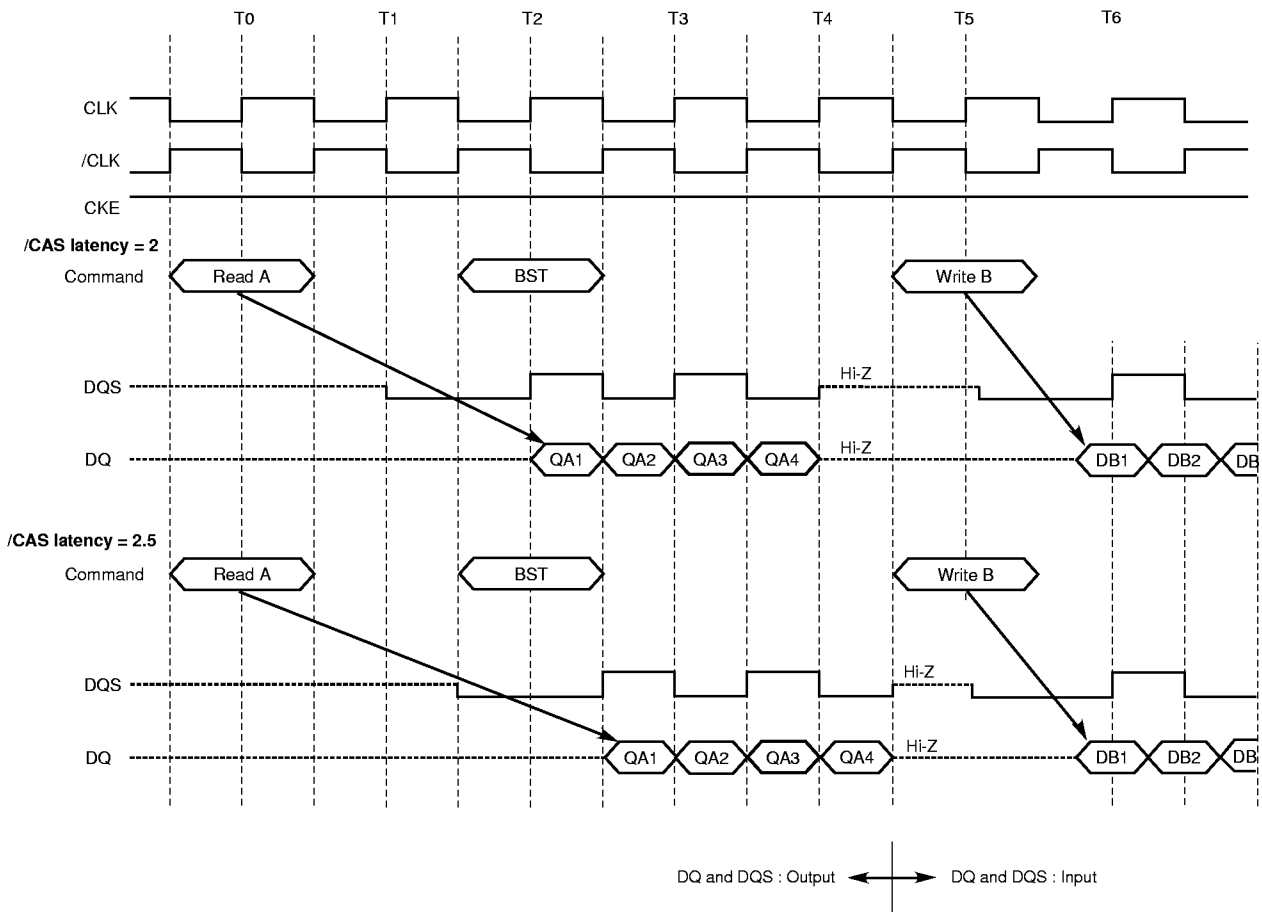
When the read command is issued, the invalid data from the burst write cycle must be masked by DM.



11.4 Read to Write Command Interval

To interrupt the burst read operation using the write command, the burst stop command must be issued to avoid data conflict. The data bus must be high impedance at least 1 cycle before the write command is issued.

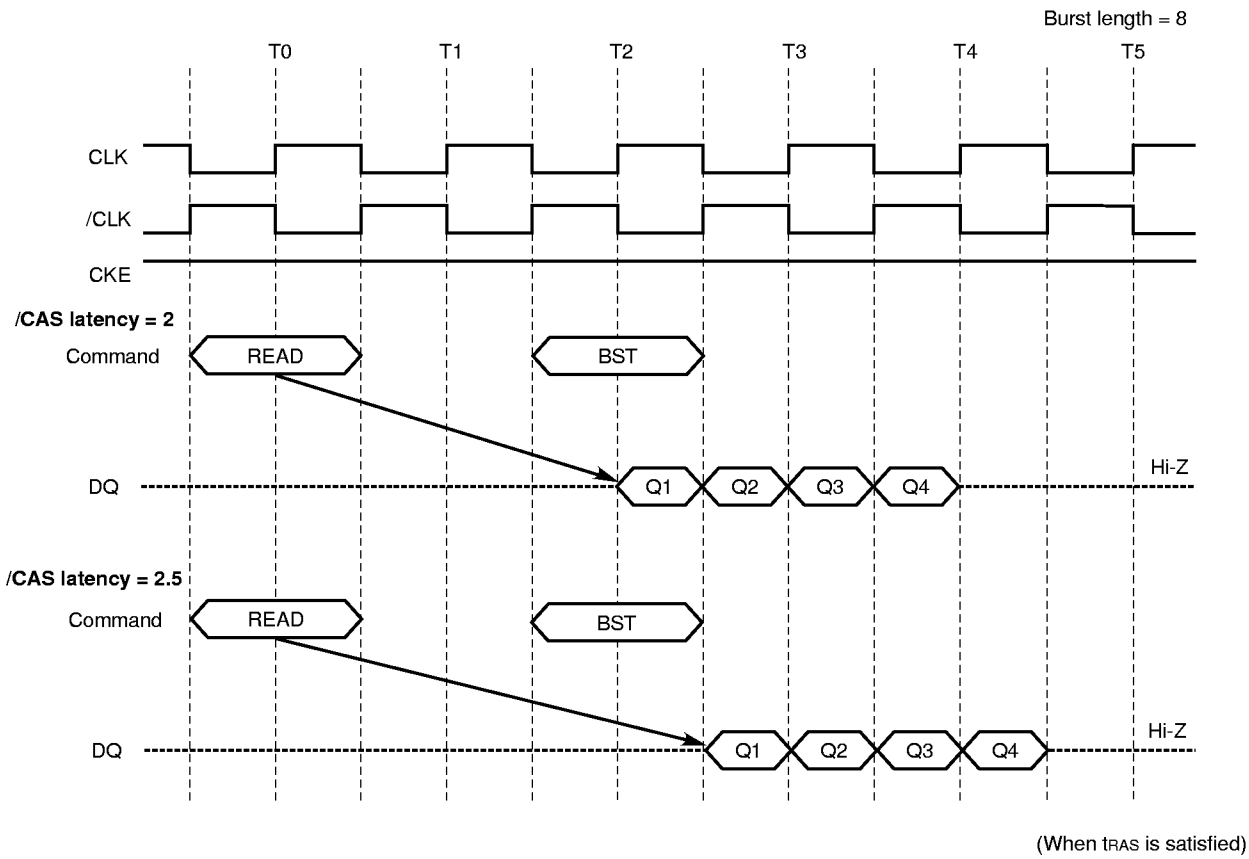
When the write command is issued, any residual data from the burst read cycle must be terminated by the burst stop command. When /CAS latency is 2, 2.5, the burst stop command must be issued at least 3 cycles prior to the write command.



12. Burst Termination

12.1 Burst Stop Command in Read Cycle

During a burst read cycle, when the burst stop command is issued at the rising edge of the clock (CLK), the burst read data are terminated and the data bus goes to high impedance after the /CAS latency from the burst stop command.

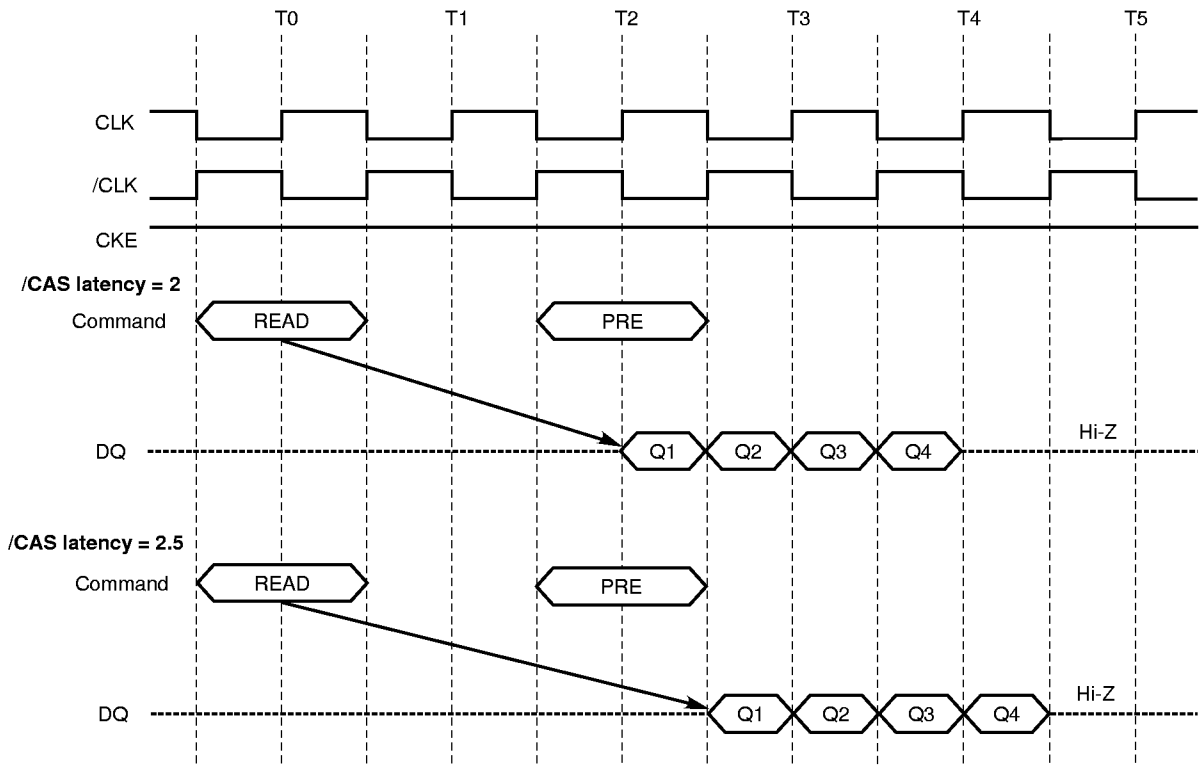


(When t_{RAS} is satisfied)

Remark BST means Burst Stop command

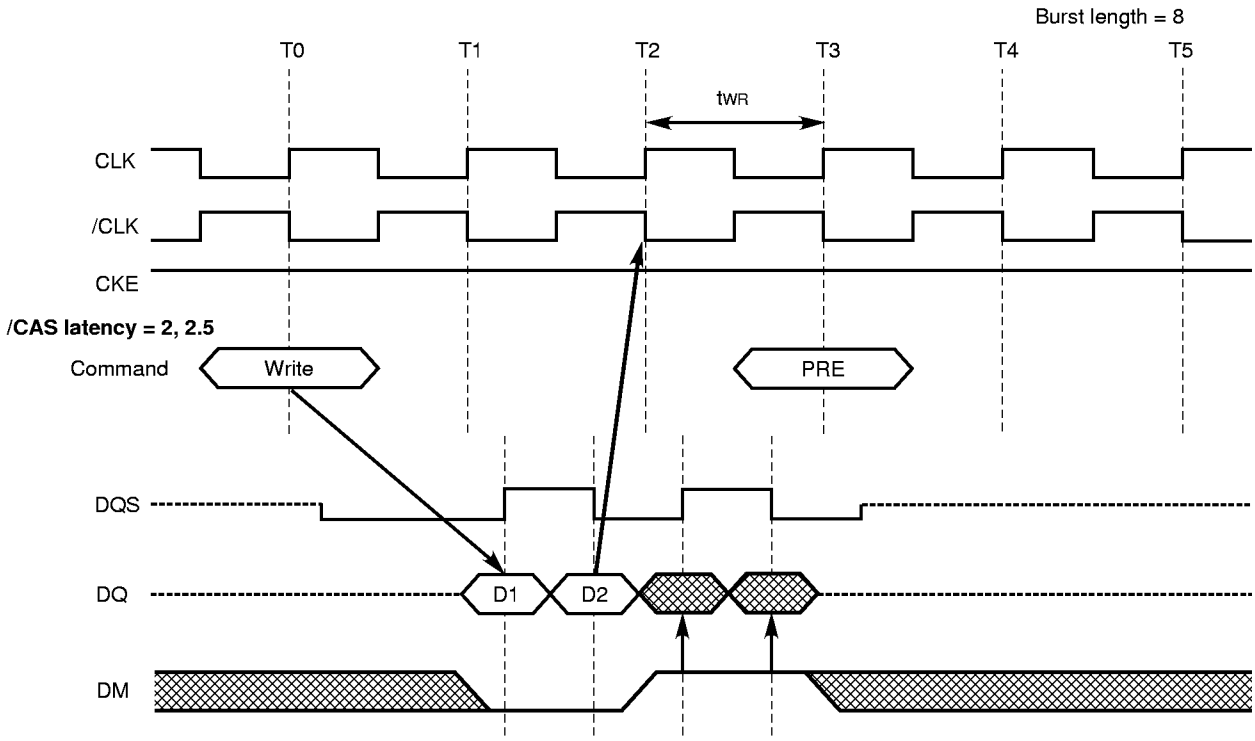
12.2 Precharge Termination in Read Cycle

During a burst read cycle without auto precharge, the burst read operation is terminated by a precharge command of the same banks. When the precharge command is issued at the rising edge of the clock (CLK), the burst read operation is terminated and the data bus goes to high impedance after the /CAS latency from the precharge command. The precharge command can be issued after $t_{RAS\ (MIN.)}$ is satisfied.



★ 12.3 Precharge Termination in Write Cycle

During a burst write cycle without auto precharge, the burst write operation is terminated by a precharge command of the same banks. In order to write the last input data to the memory cell correctly, $t_{DPL\ (MIN.)}$ must be satisfied. When the precharge command is issued at the rising edge of the clock (CLK), the invalid data from the burst write cycle must be masked DM.



13. Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute **Power on sequence and CBR (auto) Refresh** before proper device operation is achieved.

13.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to V_{SS}	V_{DD}, $V_{DD}Q$		–0.5 to +3.6	V
Voltage on any pin relative to V_{SS}	V_T		–0.5 to +3.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		1	W
Storage temperature	T_{stg}		–55 to + 125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

★ 13.2 Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.3	2.5	2.7	V
Supply voltage for DQ, DQS	$V_{DD}Q$		2.3	2.5	2.7	V
Input reference voltage	V_{REF}		1.15	1.25	1.35	V
Termination voltage	V_{TT}		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
High level dc input voltage	V_{IH} (DC)		V_{REF} + 0.18		V_{DD} + 0.3	V
Low level dc input voltage	V_{IL} (DC)		–0.3		V_{REF} – 0.18	V
Input differential voltage (CLK and /CLK)	V_{ID} (DC)		0.36		$V_{DD}Q$ + 0.6	V
Input crossing point voltage (CLK and /CLK)	V_{IX}		0.5 × $V_{DD}Q$–0.2		0.5 × $V_{DD}Q$+0.2	V
Operating ambient temperature	T_A		0		70	°C

★ 13.3 Pin Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, BA0, BA1	2.5		3.5	pF
	C_{I2}	CLK, /CLK, CKE, /CS, /RAS, /CAS, /WE, DM, LDM, UDM	2.5		3.5	pF
Data input/output capacitance	C_{IO1}	DQS, LDQS, UDQS	4		5.5	pF
	C_{IO2}	DQ0 - DQ15	4		5.5	pF

★ 13.4 DC Characteristics 1 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	/CAS latency	Grade	Maximum x4	Maximum x8	Maximum x16	Unit	Notes
Operating current (ACT-PRE)	I_{DD0}	$t_{RC} = t_{RC(MIN.)}$, $t_{CK} = t_{CK(MIN.)}$, One bank, Active-precharge, DQ, DM and DQS inputs changing twice per clock cycle, Address and control inputs changing once per clock cycle		-C75	160			mA	1
				-C80	140				
Operating current (ACT-READ-PRE)	I_{DD1}	$t_{RC} = t_{RC(MIN.)}$, $t_{CK} = t_{CK(MIN.)}$, One bank, Active-read-precharge, I_O = 0 mA, Burst length = 2, Address and control inputs changing once per clock cycle	CL = 2	-C75	165	170	175	mA	
				-C80	150	155	160		
			CL = 2.5	-C75	175	180	185		
				-C80	160	165	170		
Precharge power down standby current	I_{DD2P}	CKE ≤ $V_{IL(MAX.)}$, $t_{CK} = t_{CK(MIN.)}$, All banks idle, Power down mode			10			mA	
Idle standby current	I_{DD2N}	CKE ≥ $V_{IH(MIN.)}$, $t_{CK} = t_{CK(MIN.)}$, /CS ≥ $V_{IH(MIN.)}$, All banks idle			50			mA	
Active power down standby current	I_{DD3P}	CKE ≤ $V_{IL(MAX.)}$, $t_{CK} = t_{CK(MIN.)}$, All banks idle, Power down mode			50			mA	
Active standby current	I_{DD3N}	CKE ≥ $V_{IH(MIN.)}$, $t_{CK} = t_{CK(MIN.)}$, $t_{RC} = t_{RAS(MAX.)}$, One bank, Active-precharge, DQ, DM and DQS inputs changing twice per clock cycle, Address and control inputs changing once per clock cycle			70			mA	
Operating current (Burst read)	I_{DD4R}	$t_{CK} = t_{CK(MIN.)}$, Continuous burst read, Burst length = 2, I_O = 0mA, Address and control inputs changing once per clock cycle	CL = 2	-C75	170	180	200	mA	2
				-C80	170	180	200		
			CL = 2.5	-C75	230	240	265		
				-C80	215	225	250		
Operating current (Burst write)	I_{DD4W}	$t_{CK} = t_{CK(MIN.)}$, Continuous burst write, Burst length = 2, Address and control inputs changing once per clock cycle	CL = 2	-C75	160	170	190	mA	2
				-C80	160	170	190		
			CL = 2.5	-C75	220	230	255		
				-C80	205	215	240		
CBR (auto) refresh current	I_{DD5}	$t_{RFC} = t_{RFC(MIN.)}$		-C75	270			mA	
				-C80	250				
Self refresh current	I_{DD6}	CKE ≤ 0.2 V			2			mA	

Notes 1. I_{DD1} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{DD4R} and I_{DD4W} depend on output loading and cycle rates. Specified values are obtained with the output open.

★ 13.5 DC Characteristics 2 (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V, all other pins not under test = 0 V	–5	5	μA	
Output leakage current	$I_{O(L)}$	D_{OUT} is disabled, V_O = 0 to $V_{DD}Q$ + 0.3 V	–5	5	μA	
Output high current	I_{OH}	V_{OUT} = $V_{DD}Q$ –0.43 V	–15.2		mA	
Output low current	I_{OL}	V_{OUT} = 0.35 V	15.2		mA	

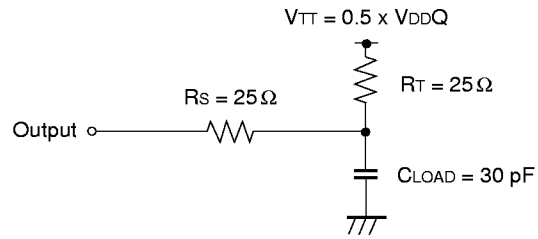
13.6 AC Characteristics (Recommended Operating Conditions unless otherwise noted)

13.6.1 Test Conditions

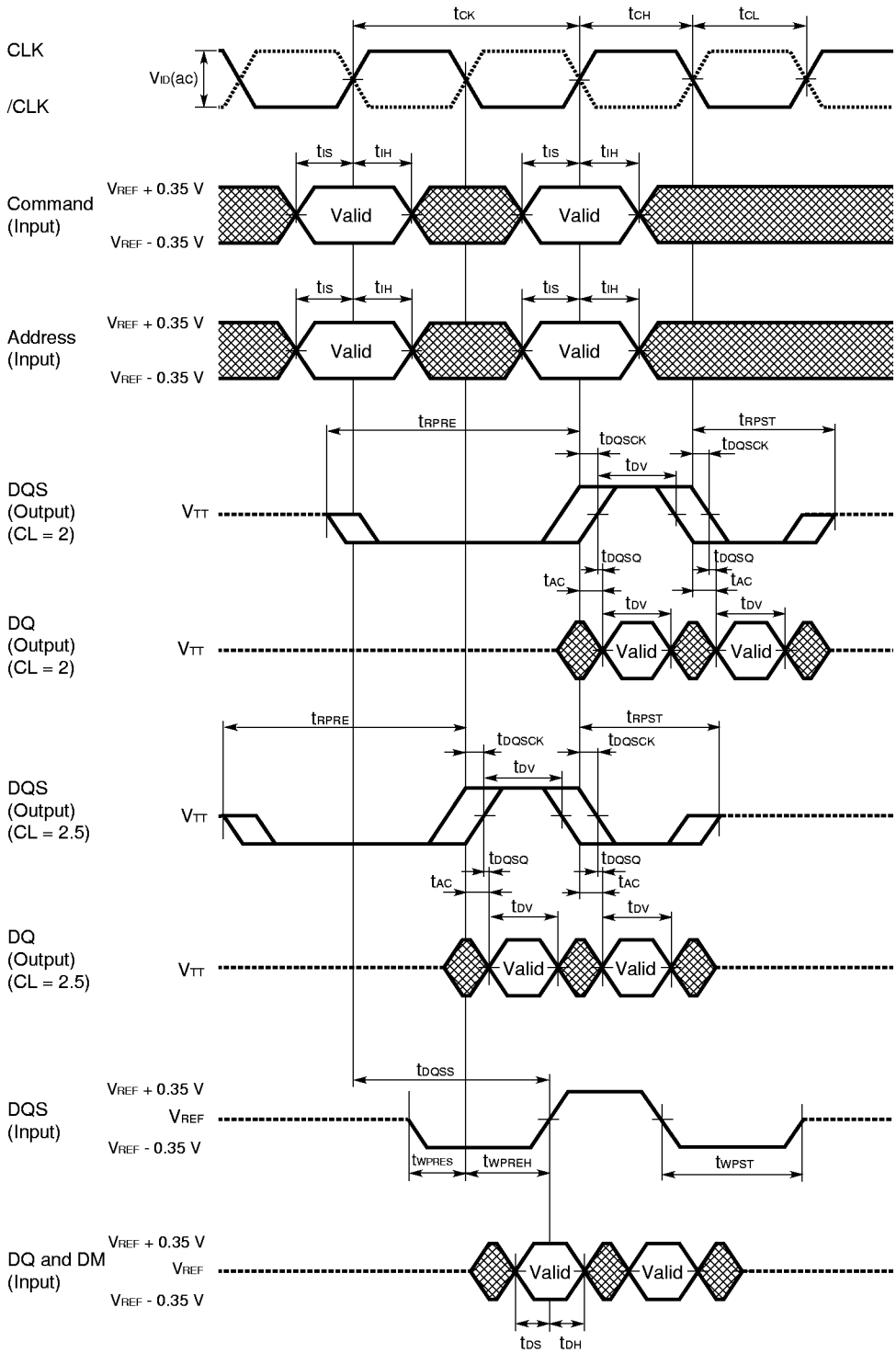
	Parameter	Symbol	Value	Unit	Notes
	Input Reference voltage (Input timing measurement reference level)	V_{REF}	$V_{DD}Q$ x 0.5	V	
	Termination voltage (Output timing measurement reference level)	V_{TT}	V_{REF}	V	1
	High level ac input voltage	V_{IH}(ac)	V_{REF} + 0.35	V	
	Low level ac input voltage	V_{IL}(ac)	V_{REF} – 0.35	V	
★	Input differential voltage (CLK and /CLK)	V_{ID}(ac)	0.7	V	
	Input signal slew rate	SLEW	1	V/ns	2

Notes 1. Output waveform timing is measured where the output signal crosses through the V_{TT} level.

2. Slew rate is to be maintained in the V_{IL} (ac) to V_{IH}(ac) range of the input signal swing. SLEW = (V_{IH}(ac)-V_{IL}(ac))/ Δt



★ 13.6.2 Timing Diagram



★ **13.6.3 Synchronous Characteristics**

Parameter		Symbol	-C75 (PC266B)		-C80 (PC200)		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Clock cycle time	CL = 2.5	t_{CK}	7.5	15	8	15	ns	
	CL = 2		10	15	10	15		
CLK high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
CLK low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
DQ output access time from CLK, /CLK		t_{AC}	–0.75	0.75	–0.8	0.8	ns	
DQS output access time from CLK, /CLK		t_{DQSCK}	–0.75	0.75	–0.8	0.8	ns	
DQS-DQ skew (for DQS and associated DQ signals)		t_{DQSQ}	–0.5	0.5	–0.6	0.6	ns	
DQS-DQ skew (for DQS and all DQ signals)		t_{DQSQA}	–0.5	0.5	–0.6	0.6	ns	
DQ/DQS output valid time		t_{DV}	0.35		0.35		t_{CK}	
Data out low-impedance time from CLK, /CLK		t_{LZ}	–0.75	0.75	–0.8	0.8	ns	
Data out high-impedance time from CLK, /CLK		t_{HZ}	–0.75	0.75	–0.8	0.8	ns	
Read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	
Read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}	
DQ and DM input setup time		t_{DS}	0.5		0.6		ns	
DQ and DM input hold time		t_{DH}	0.5		0.6		ns	
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75		2		ns	
Write preamble setup time		t_{WPRES}	0		0		ns	
DQS hold time from CLK, /CLK		t_{WPREH}	0.25		0.25		t_{CK}	
Write postamble		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}	
Write command to first DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	
DQS input valid time		$t_{DSL,H}$	0.4	0.6	0.4	0.6	t_{CK}	
Address and control input setup time		t_{IS}	1.1		1.2		ns	
Address and control input hold time		t_{IH}	1.1		1.2		ns	
Internal write to read command delay		t_{WTR}	1		1		t_{CK}	
Transition time (CLK, /CLK, DQS, DQ, DM)		t_{TD}	0.5		0.5		ns	
Transition time (CMD, Add)		t_{T}	0.5		0.5		ns	

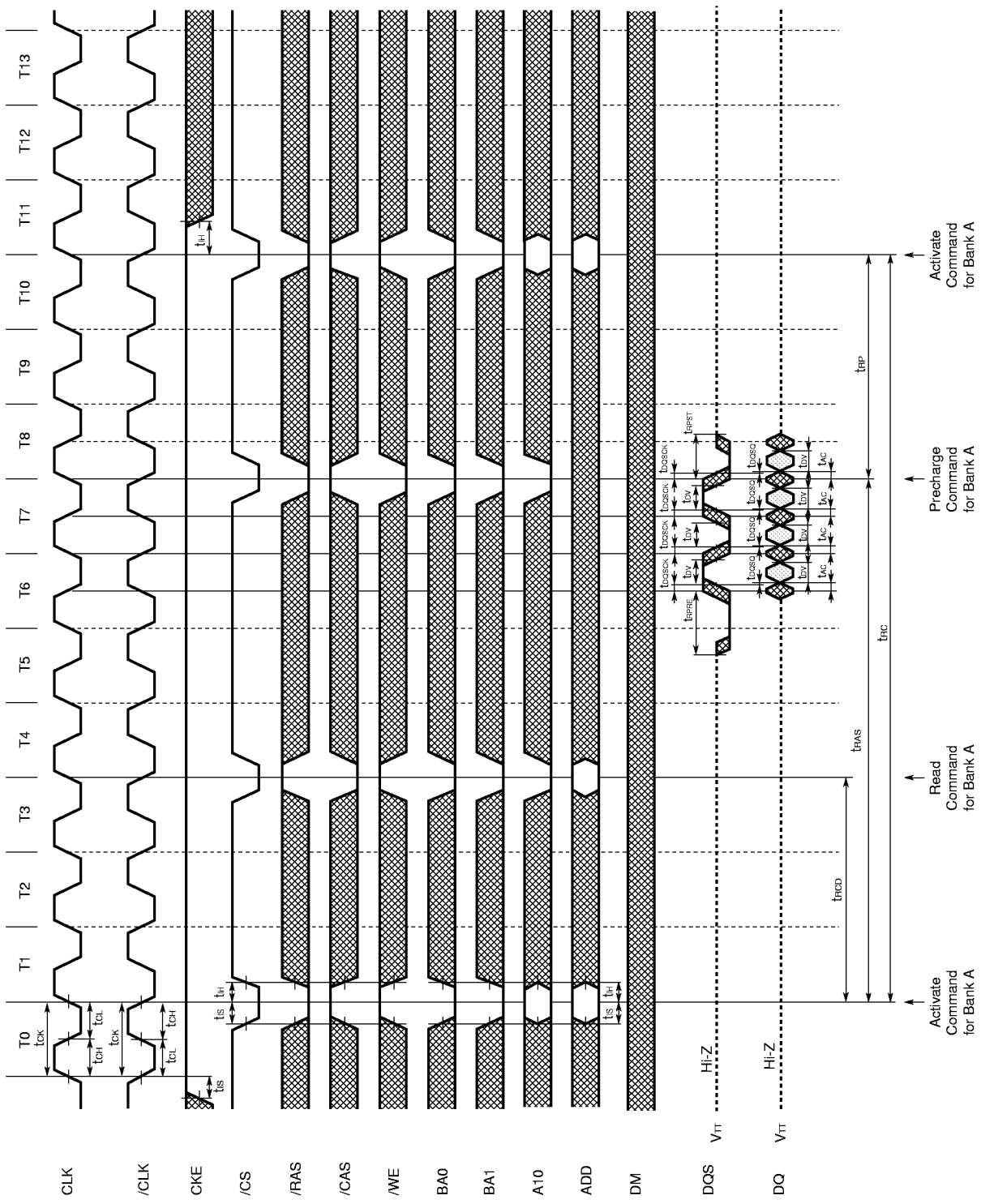
★ **13.6.4 Synchronous Characteristics Example**

Symbol	t_{CK} =7.5 ns		t_{CK} =8 ns		t_{CK} =10 ns		Unit
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{CH}	3.375	4.125	3.6	4.4	4.5	5.5	ns
t_{CL}	3.375	4.125	3.6	4.4	4.5	5.5	ns
t_{DV}	2.625		2.8		3.5		ns
t_{RPRE}	6.75	8.25	7.2	8.8	9	11	ns
t_{RPST}	3	4.5	3.2	4.8	4	6	ns
t_{WPREH}	1.875		2		2.5		ns
t_{WPST}	3	4.5	3.2	4.8	4	6	ns
t_{DQSS}	5.625	9.375	6	10	7.5	12.5	ns
$t_{DSL,H}$	3	4.5	3.2	4.8	4	6	ns
t_{WTR}	7.5		8		10		ns

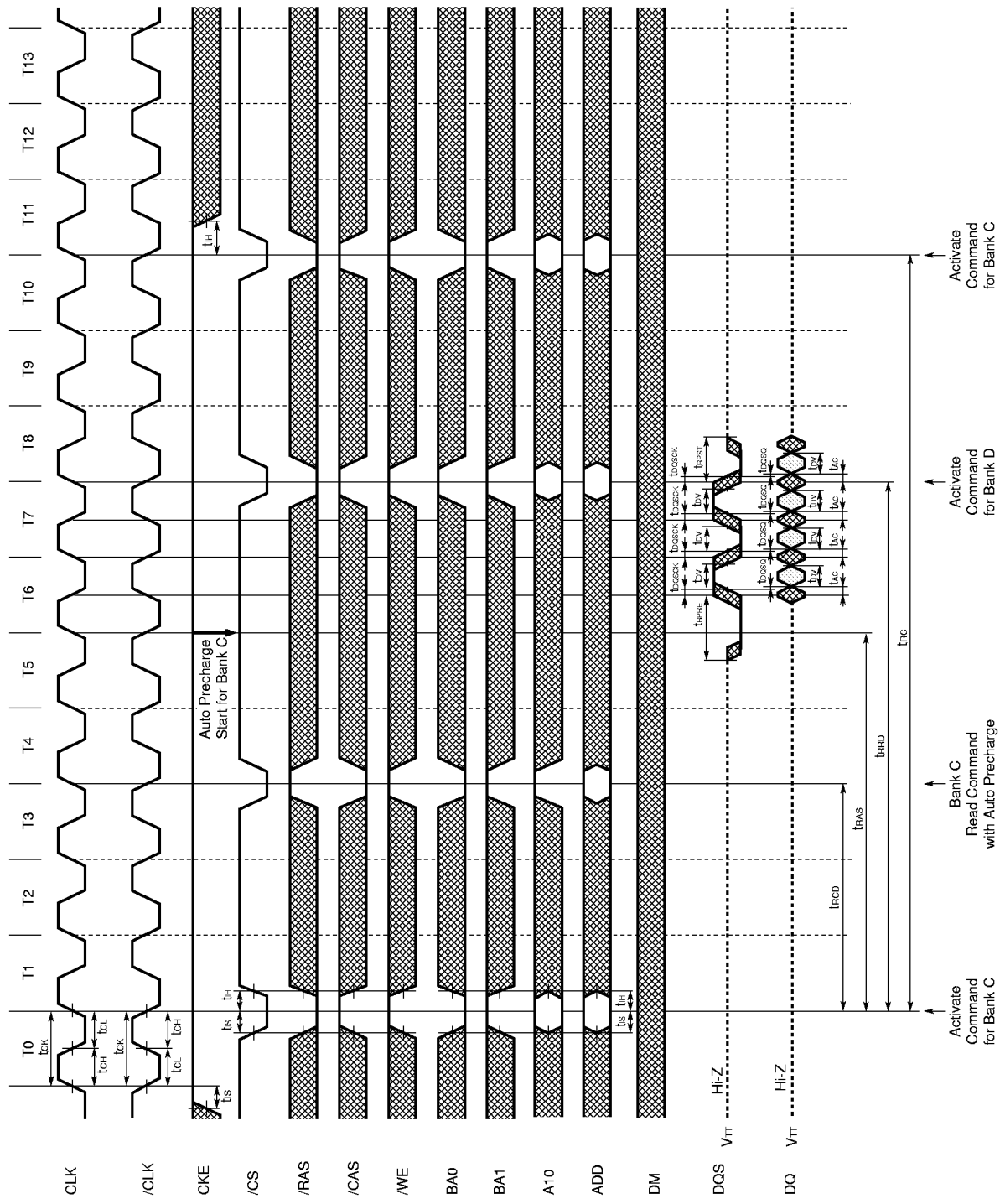
★ **13.6.5 Asynchronous Characteristics**

Parameter	Symbol	-C75(PC266B)		-C80(PC200)		Unit
		MIN.	MAX.	MIN.	MAX.	
ACT to REF/ACT command period (operation)	t_{RC}	65		70		ns
REF to REF/ACT command period (refresh)	t_{RFC}	75		80		ns
ACT to PRE command period	t_{RAS}	45	120,000	50	120,000	ns
PRE to ACT command period	t_{RP}	20		20		ns
ACT to READ/WRITE delay	t_{RCD}	20		20		ns
ACT(one) to ACT(another) command period	t_{RRD}	15		15		ns
Write recovery time	t_{WR}	15		15		ns
Auto precharge write recovery time + precharge time	t_{DAL}	35		35		ns
Mode register set command cycle time	t_{MRD}	15		15		ns
Exit self refresh to command	t_{XSNR}	75		80		ns
Refresh time (4,096 refresh cycles)	t_{REF}		64		64	ms

★ **AC Parameters for Read Timing 1 (Manual Precharge, Burst Length = 4, /CAS Latency = 2.5)**



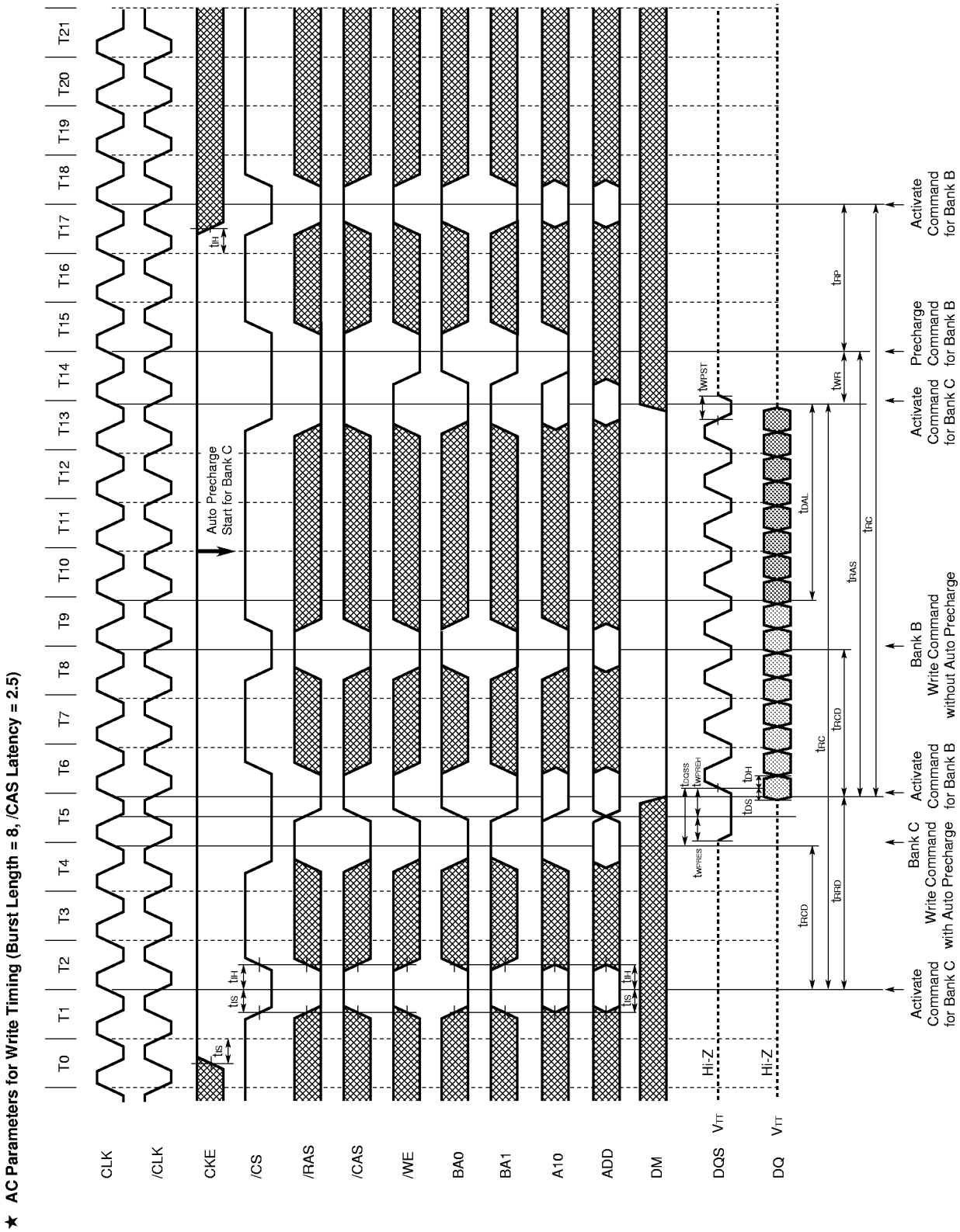
★ **AC Parameters for Read Timing 2 (Auto Precharge, Burst Length = 4, /CAS Latency = 2.5)**



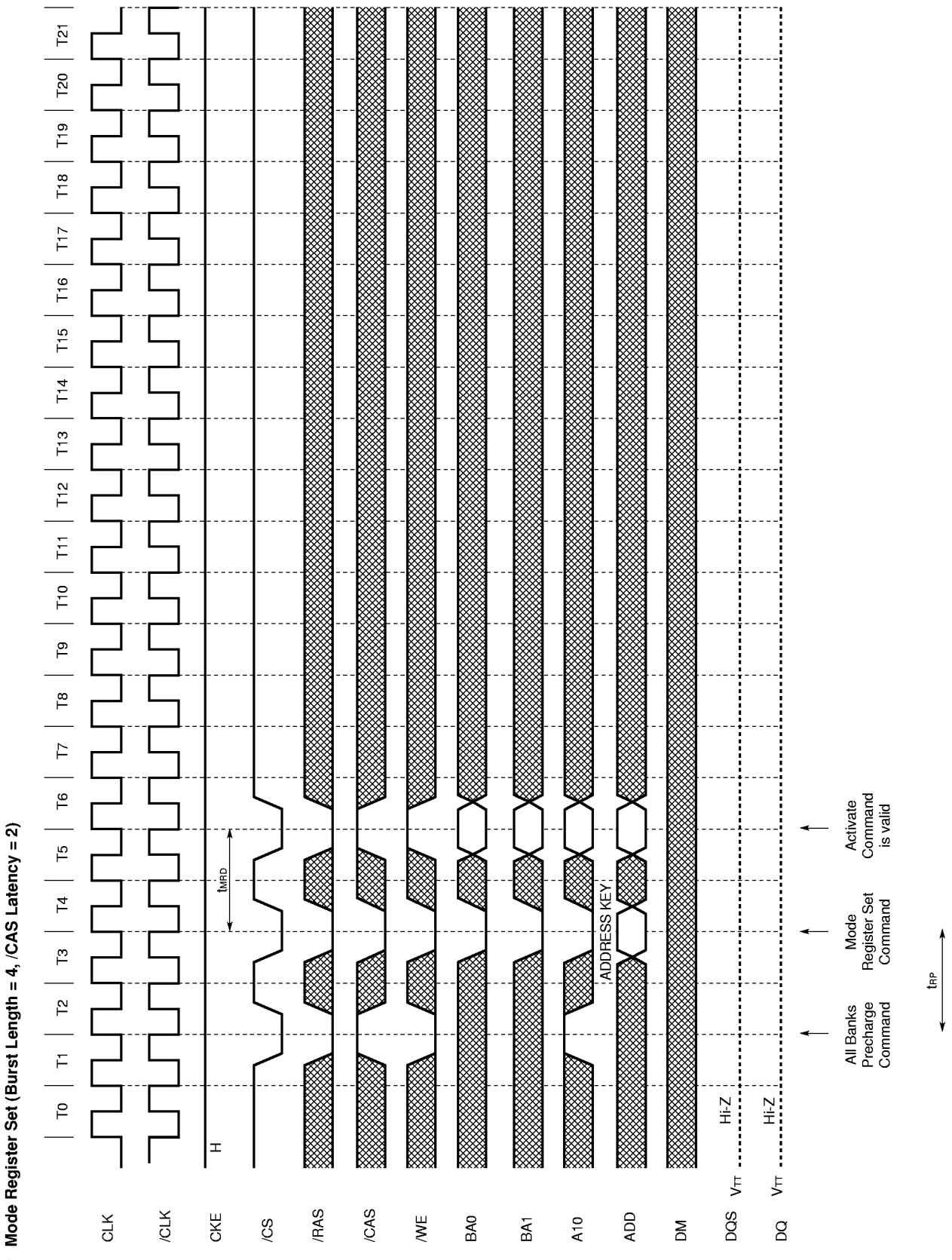
★ **Relationship between Frequency and Latency**

Speed version	-C75		-C80	
Clock cycle time [ns]	7.5	10	8	10
Frequency [MHz]	133	100	125	100
/CAS latency	2.5	2	2.5	2
[t_{RCD}]	3	2	3	2
/RAS latency (/CAS latency + [t_{RCD}])	5.5	4	5.5	4
[t_{RC}]	9	7	9	7
[t_{RFC}]	10	8	10	8
[t_{RAS}]	6	5	7	5
[t_{RRD}]	2	2	2	2
[t_{RP}]	3	2	3	2
[t_{WR}]	2	2	2	2
[t_{DAL}]	5	4	5	4
[t_{MRD}]	2	2	2	2
[t_{XSNR}]	10	8	10	8

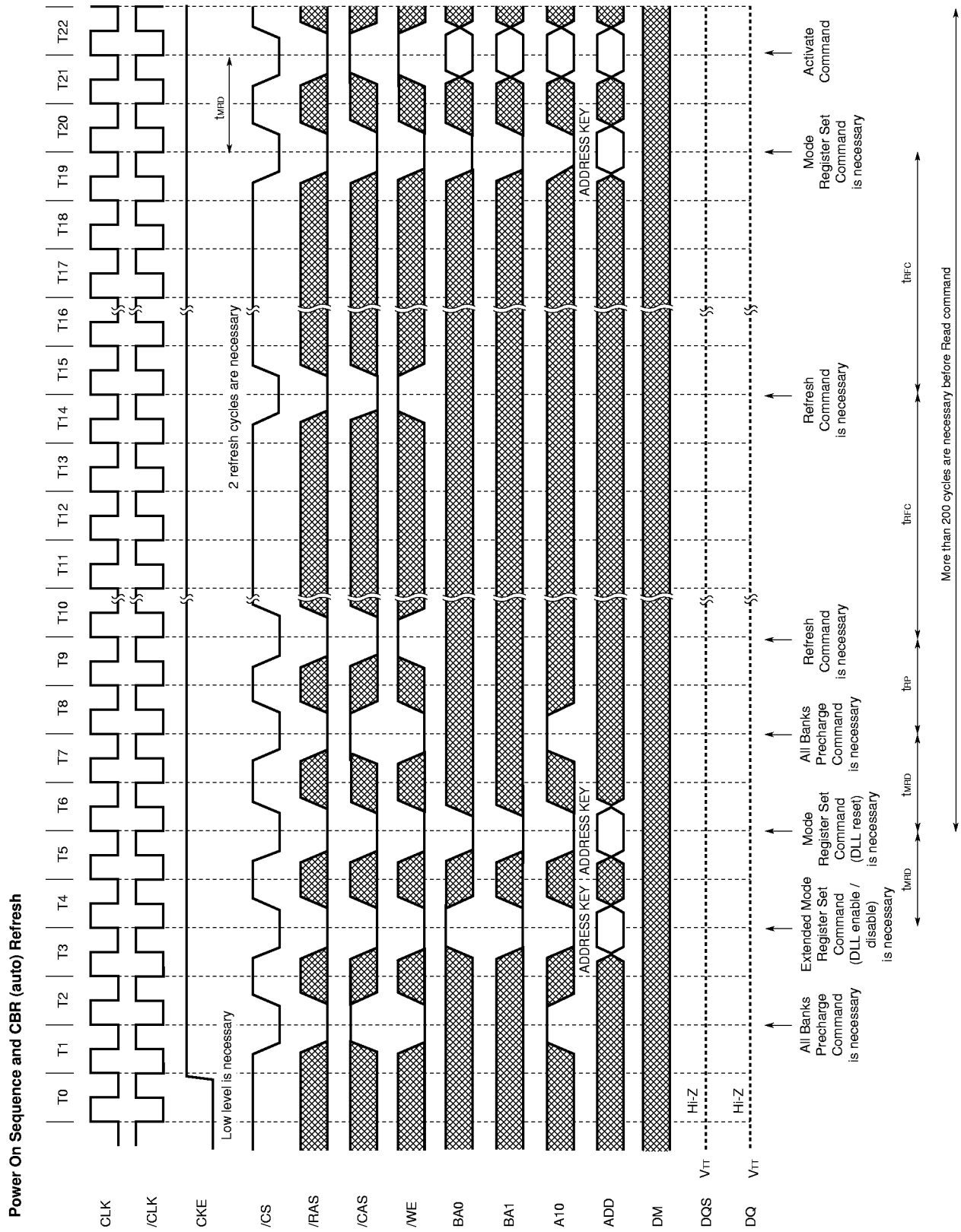
★ AC Parameters for Write Timing (Burst Length = 8, /CAS Latency = 2.5)



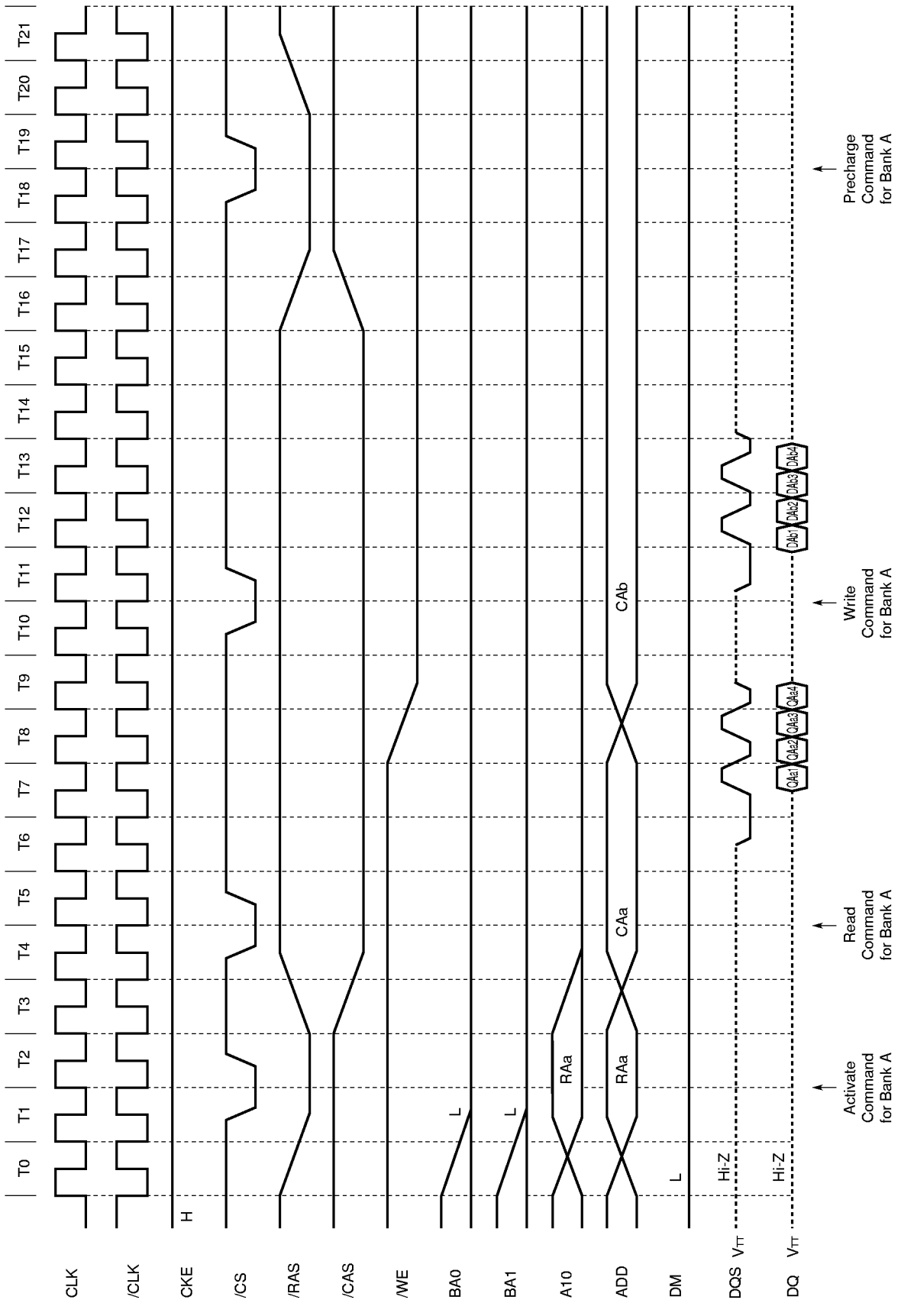
★ **Mode Register Set (Burst Length = 4, /CAS Latency = 2)**



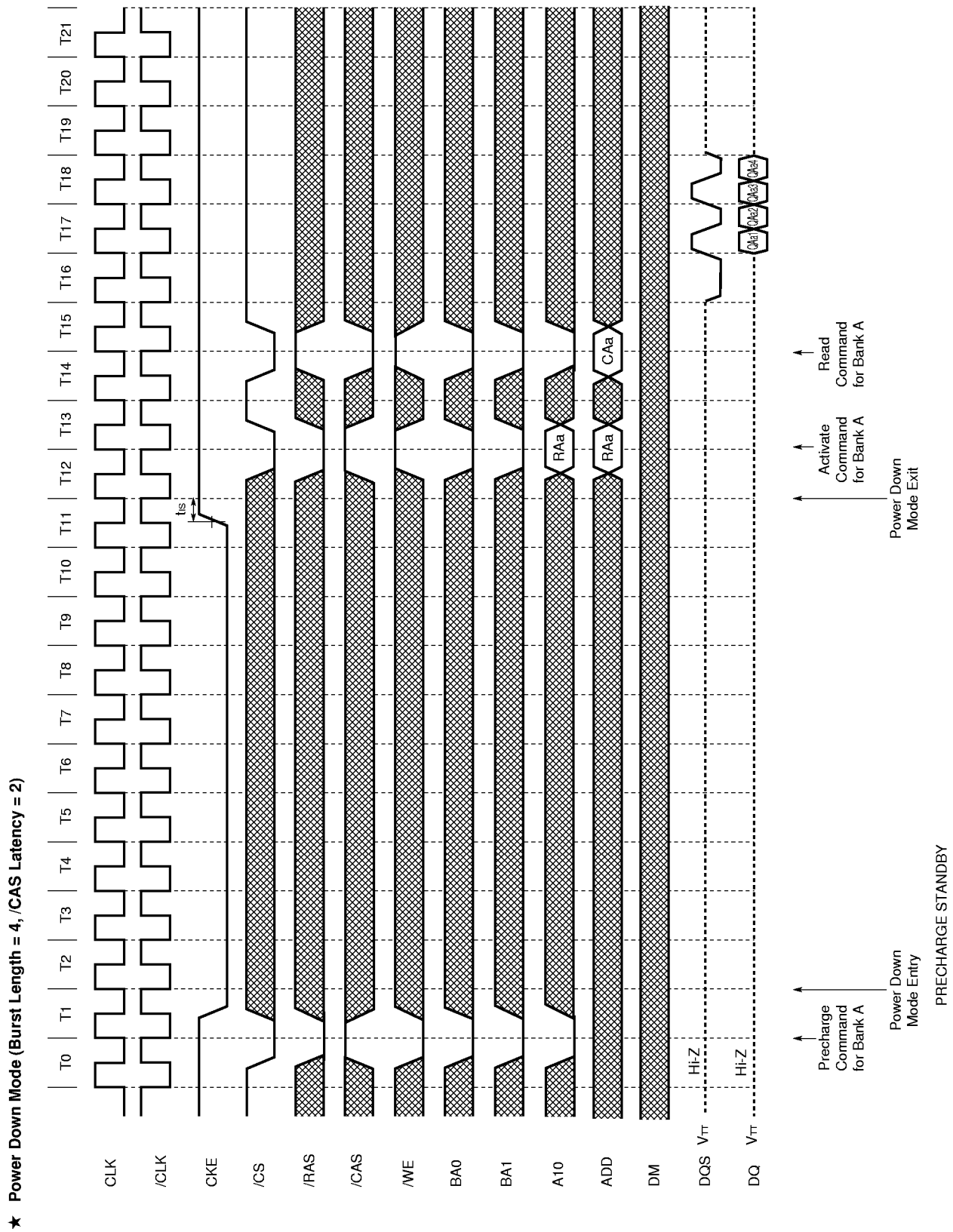
★ **Power On Sequence and CBR (auto) Refresh**



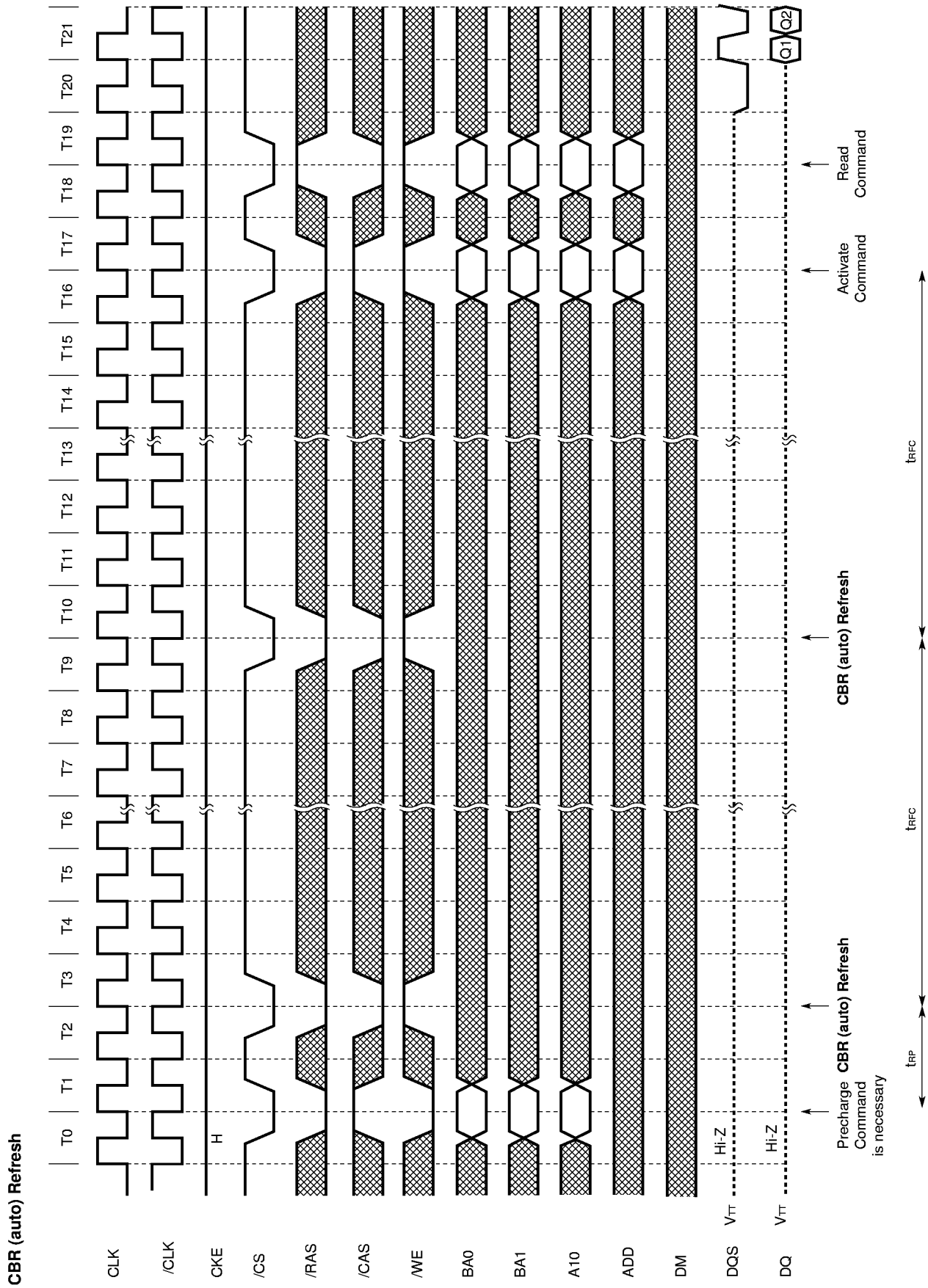
★ **/CS Function (at 100 MHz, Burst Length = 4, /CAS Latency = 2.5)**
Only /CS signal needs to be issued at minimum rate



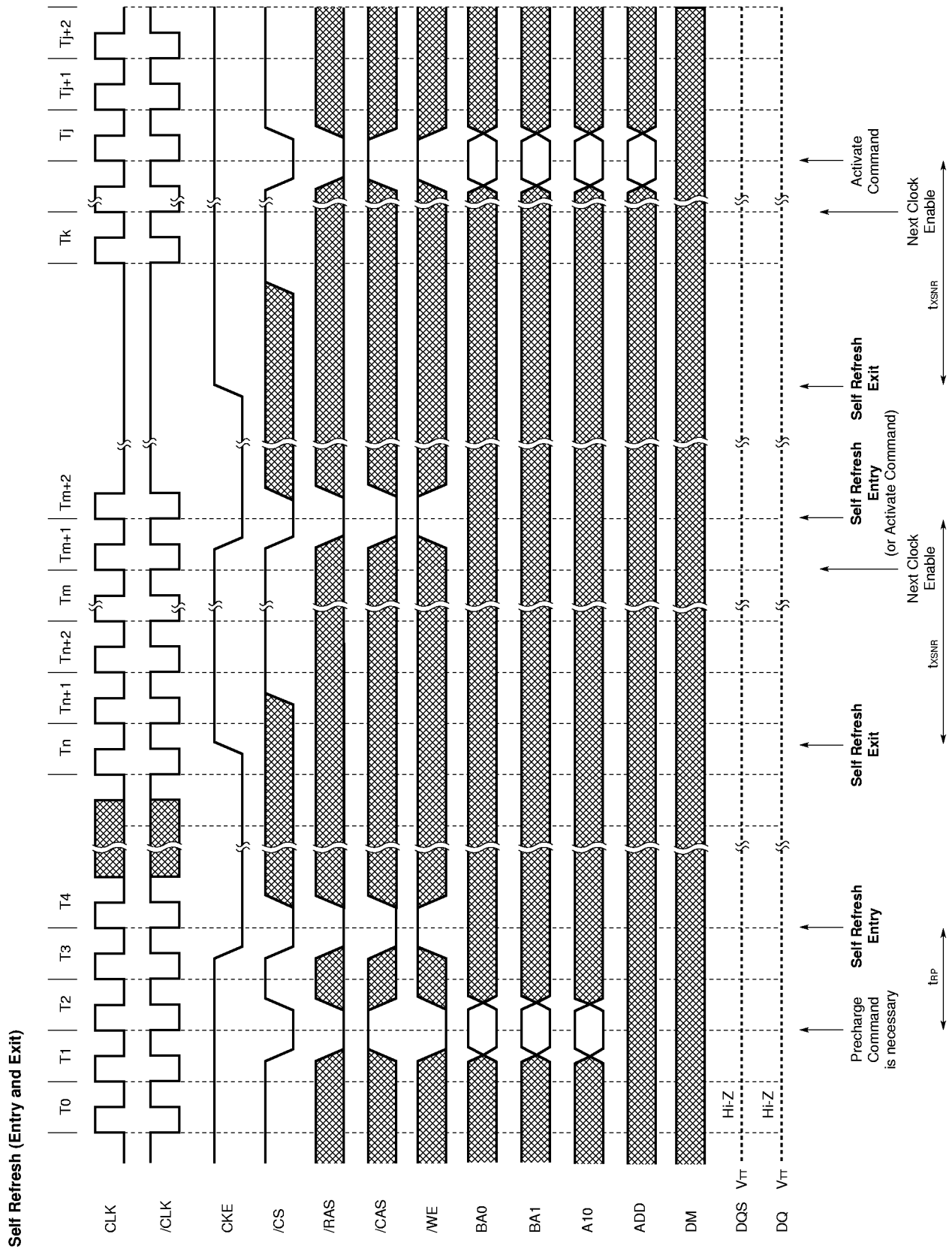
★ **Power Down Mode (Burst Length = 4, /CAS Latency = 2)**



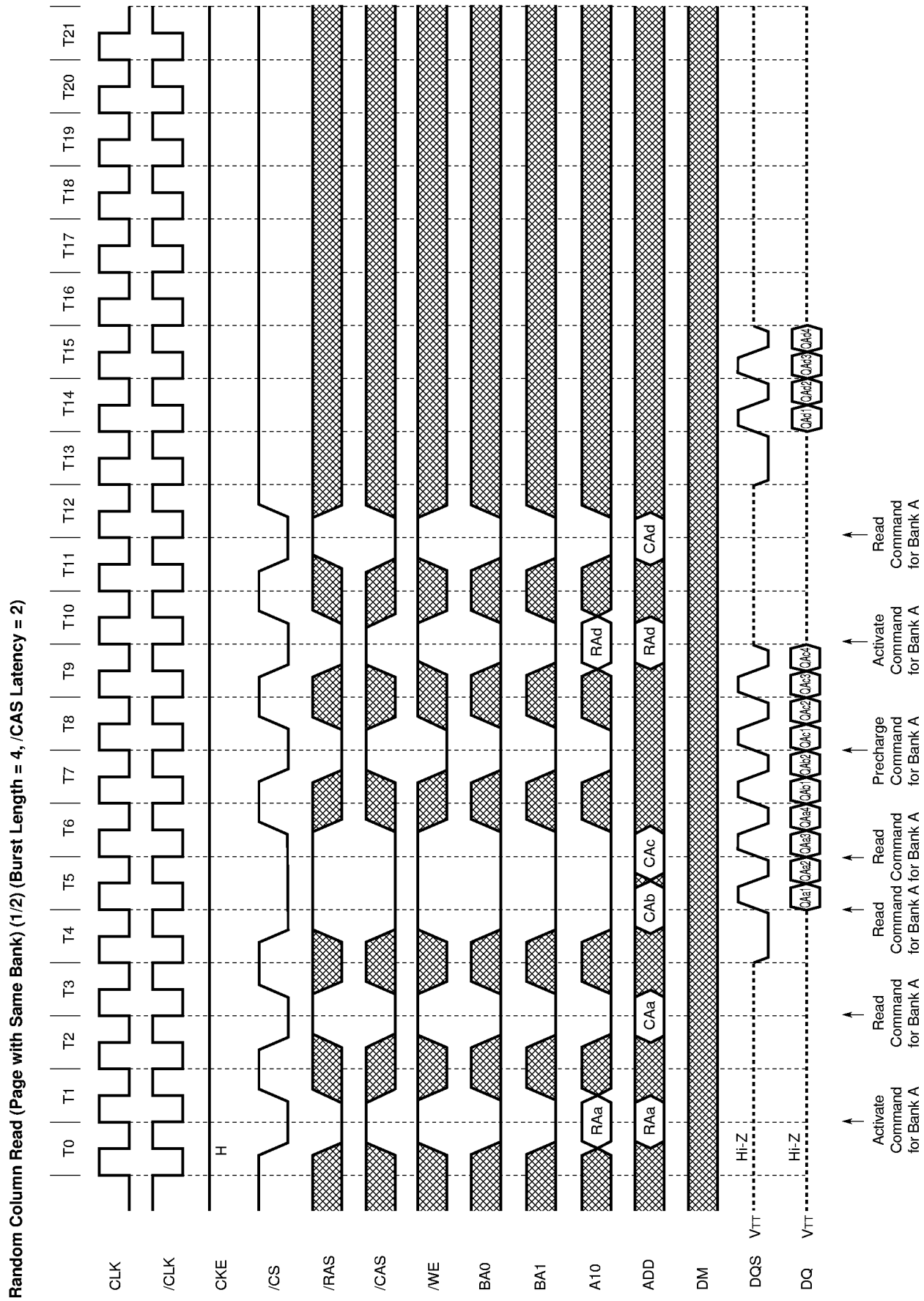
★ CBR (auto) Refresh



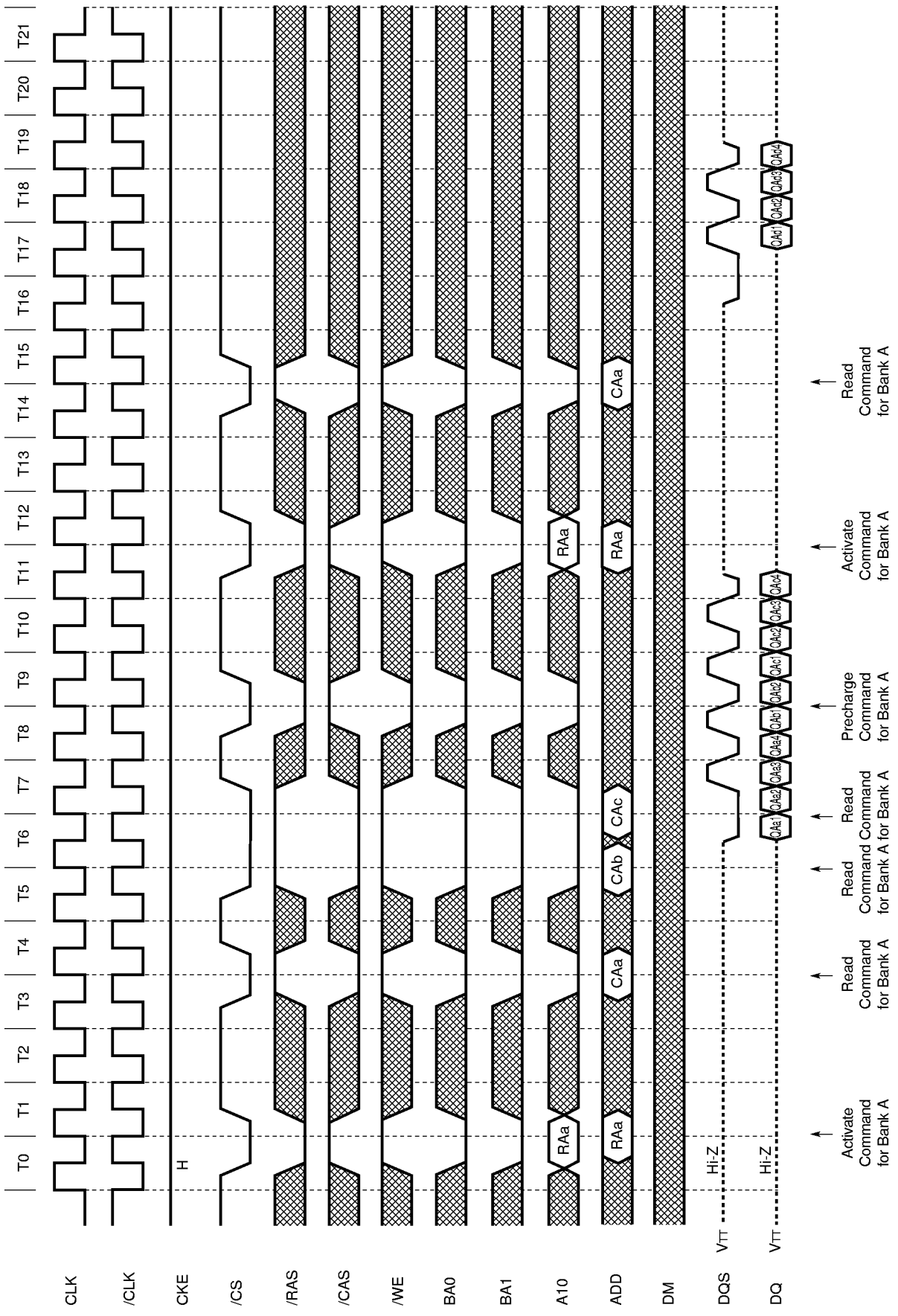
★ Self Refresh (Entry and Exit)



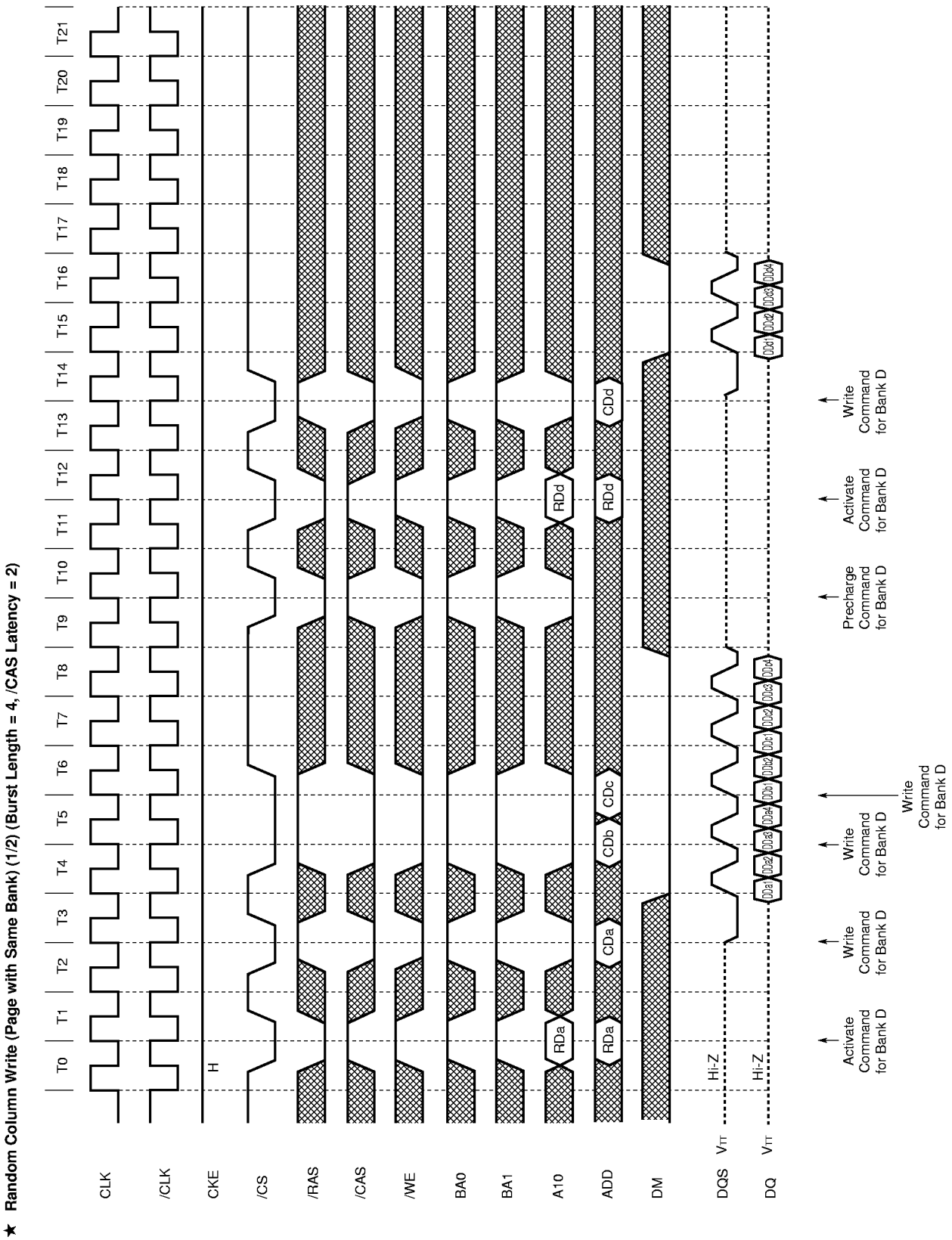
★ **Random Column Read (Page with Same Bank) (1/2) (Burst Length = 4, /CAS Latency = 2)**



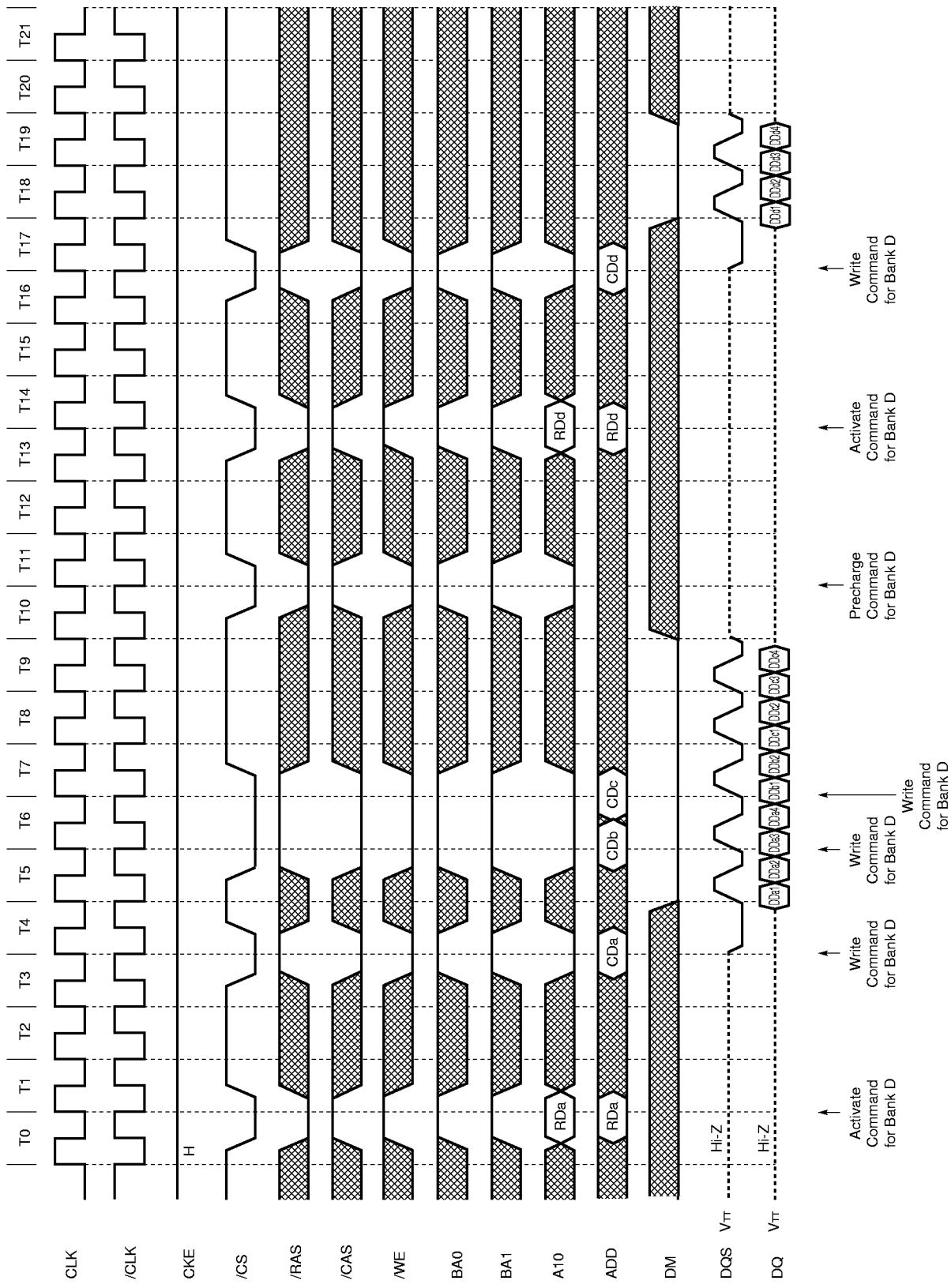
★ **Random Column Read (Page with Same Bank) (2/2) (Burst Length = 4, /CAS Latency = 2.5)**



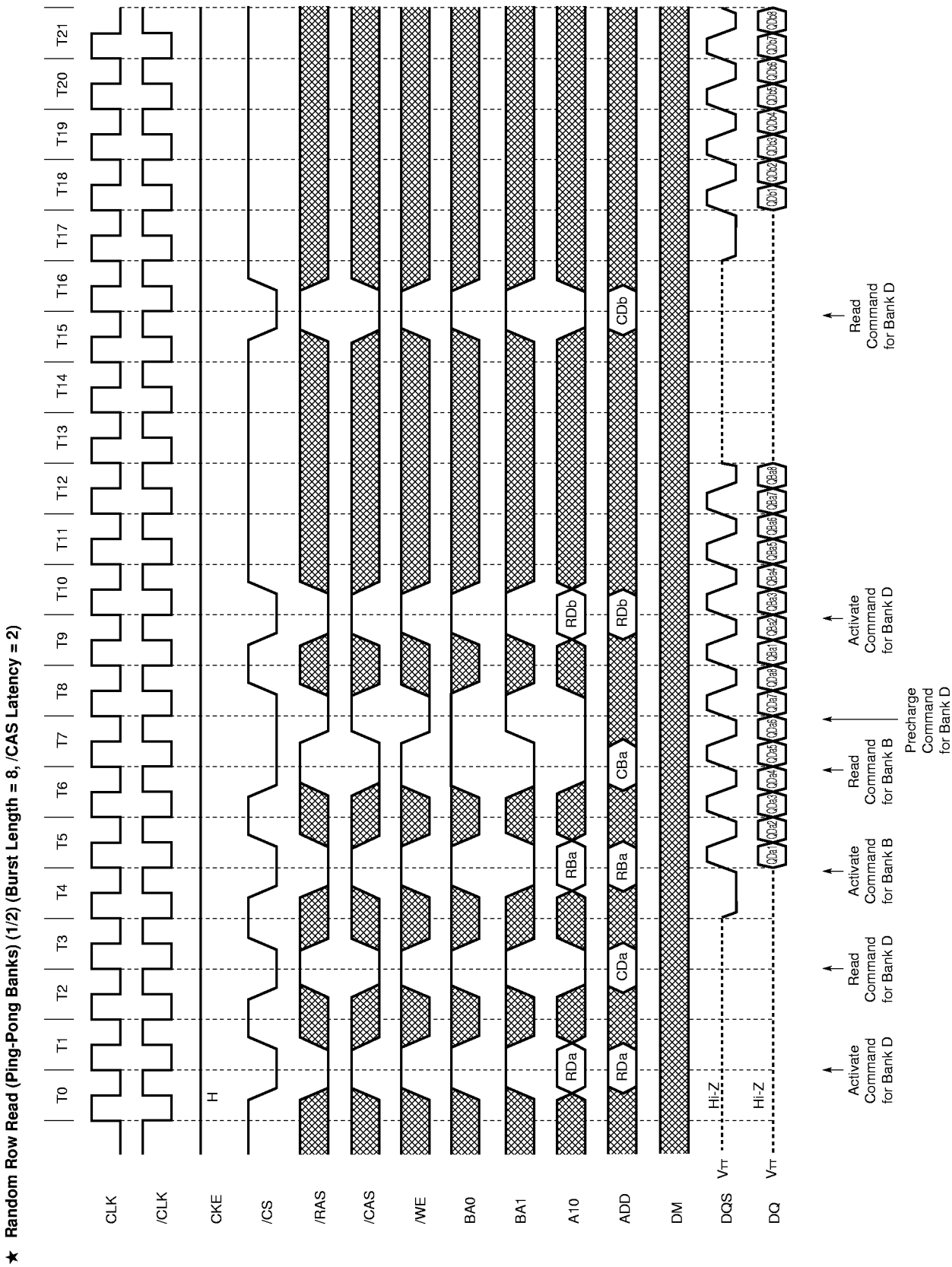
★ Random Column Write (Page with Same Bank) (1/2) (Burst Length = 4, /CAS Latency = 2)



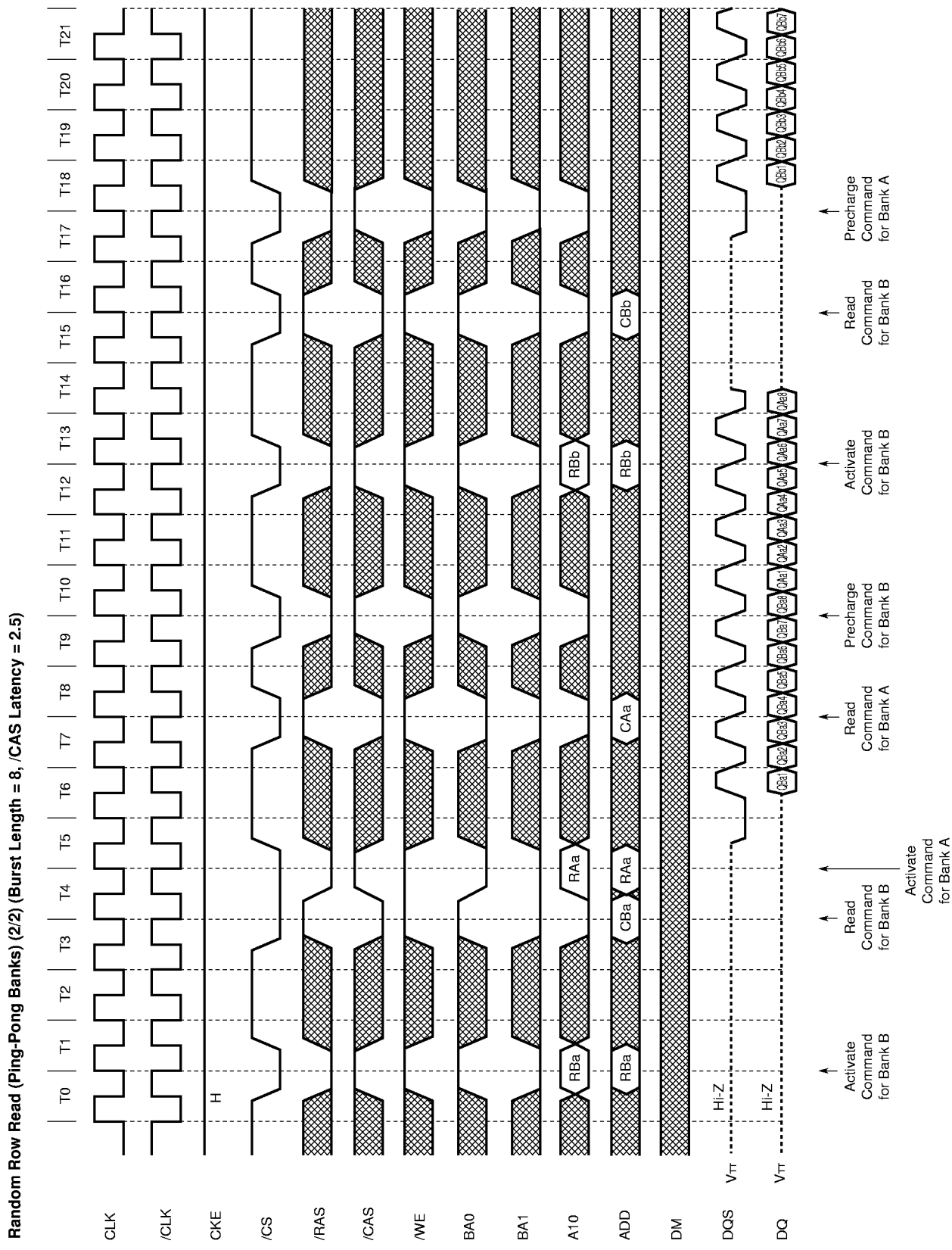
★ **Random Column Write (Page with Same Bank) (2/2) (Burst Length = 4, /CAS Latency = 2.5)**



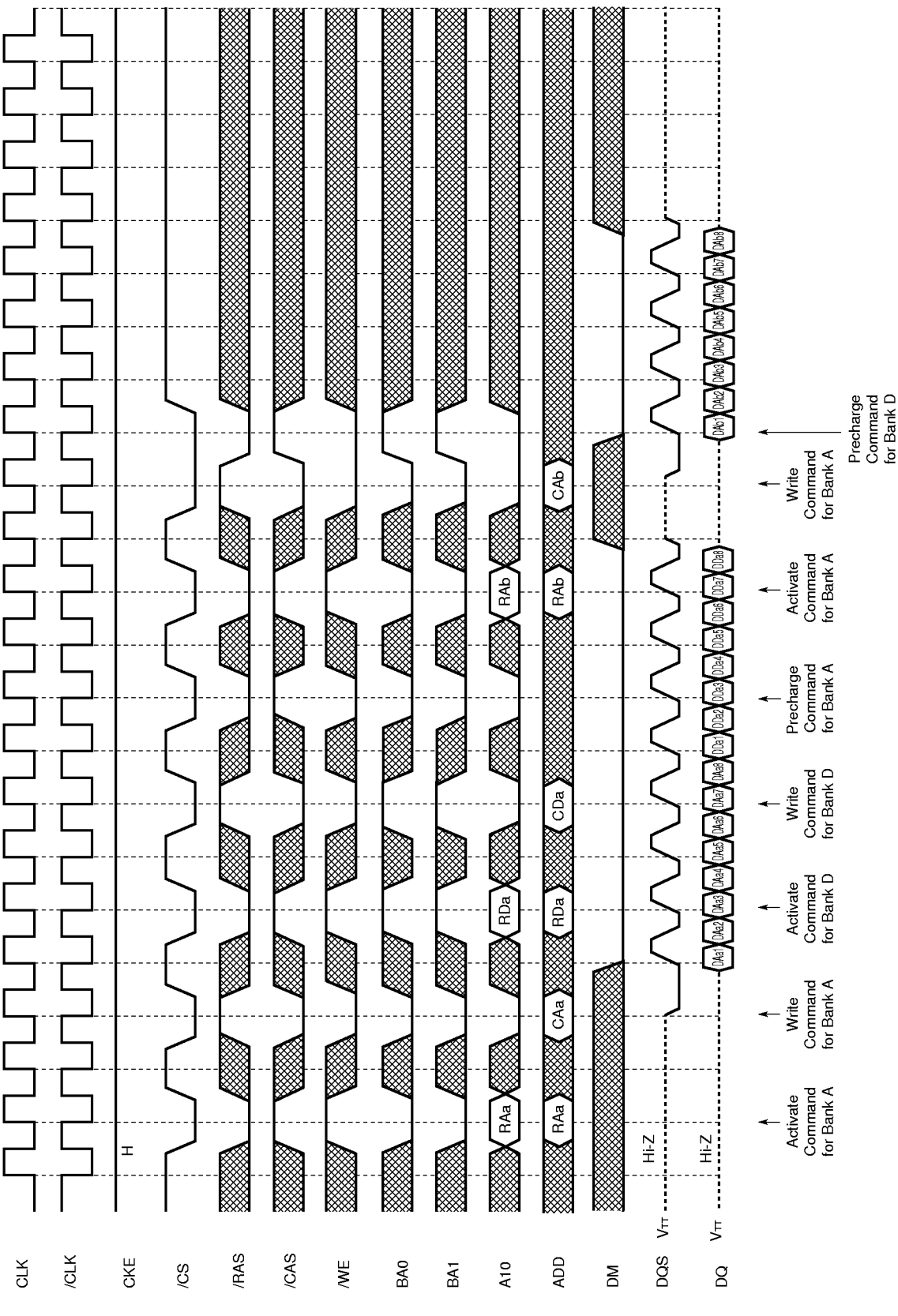
★ **Random Row Read (Ping-Pong Banks) (1/2) (Burst Length = 8, /CAS Latency = 2)**



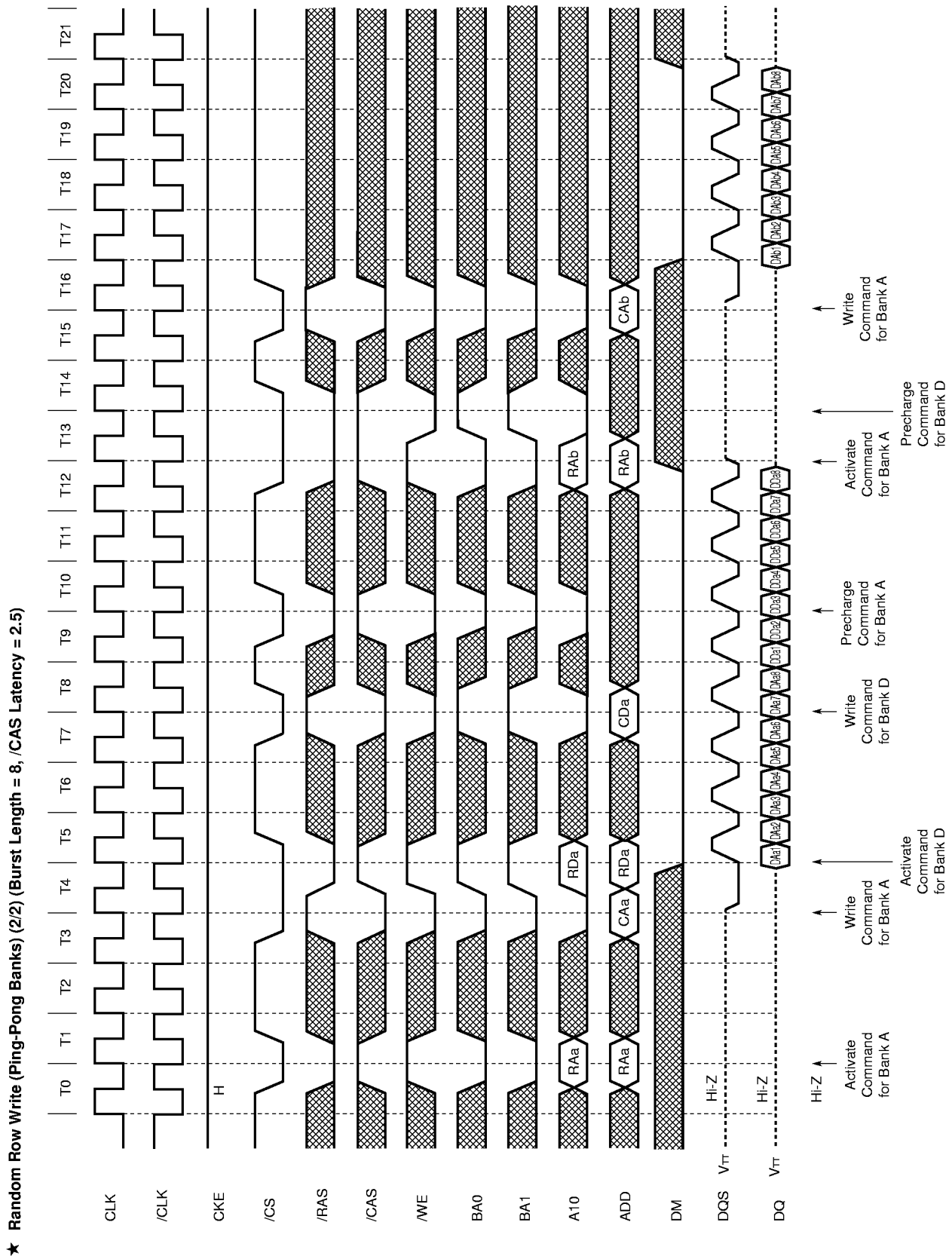
★ **Random Row Read (Ping-Pong Banks) (2/2) (Burst Length = 8, /CAS Latency = 2.5)**



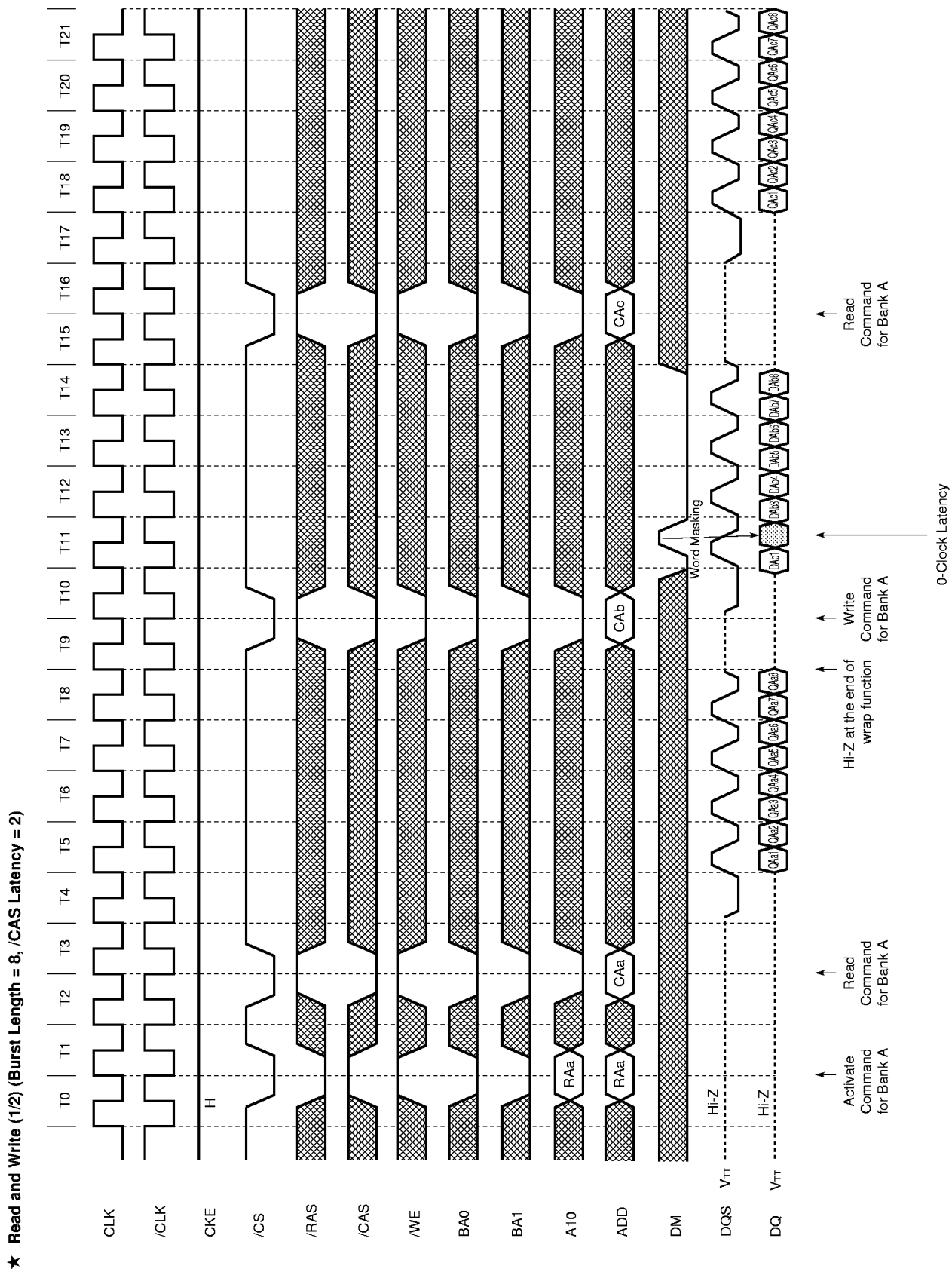
★ **Random Row Write (Ping-Pong Banks) (1/2) (Burst Length = 8, /CAS Latency = 2)**



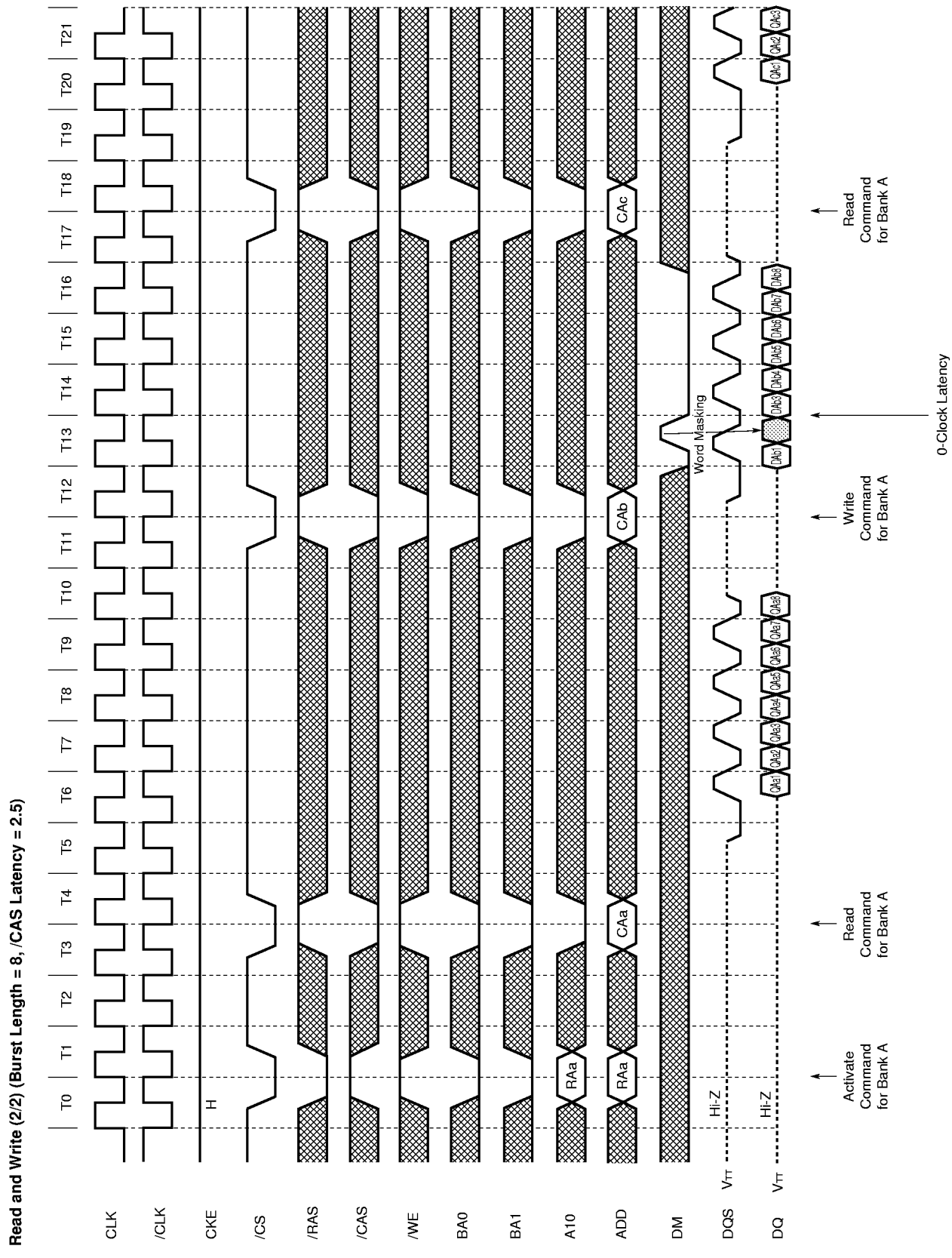
★ **Random Row Write (Ping-Pong Banks) (2/2) (Burst Length = 8, /CAS Latency = 2.5)**



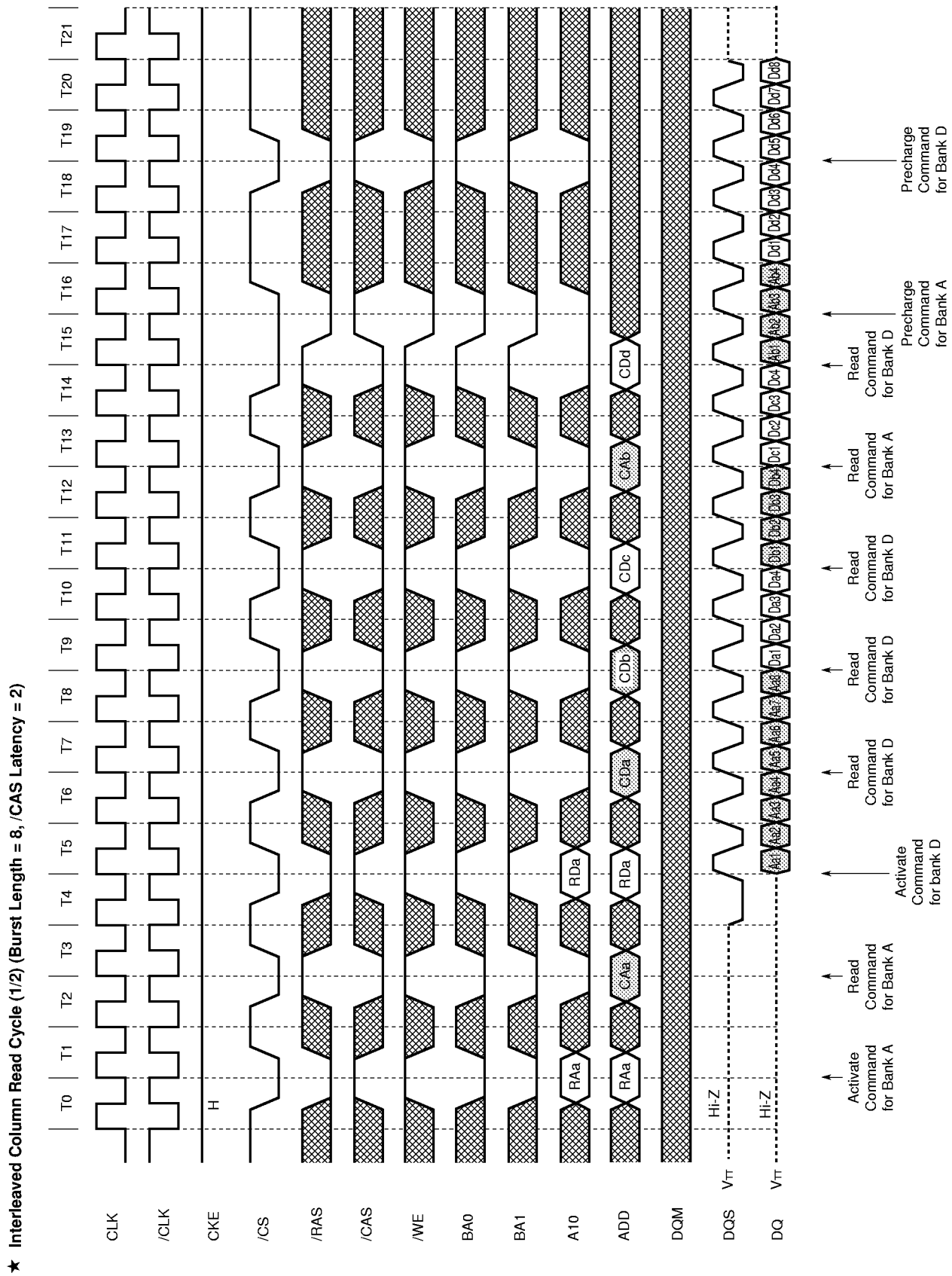
★ **Read and Write (1/2) (Burst Length = 8, /CAS Latency = 2)**



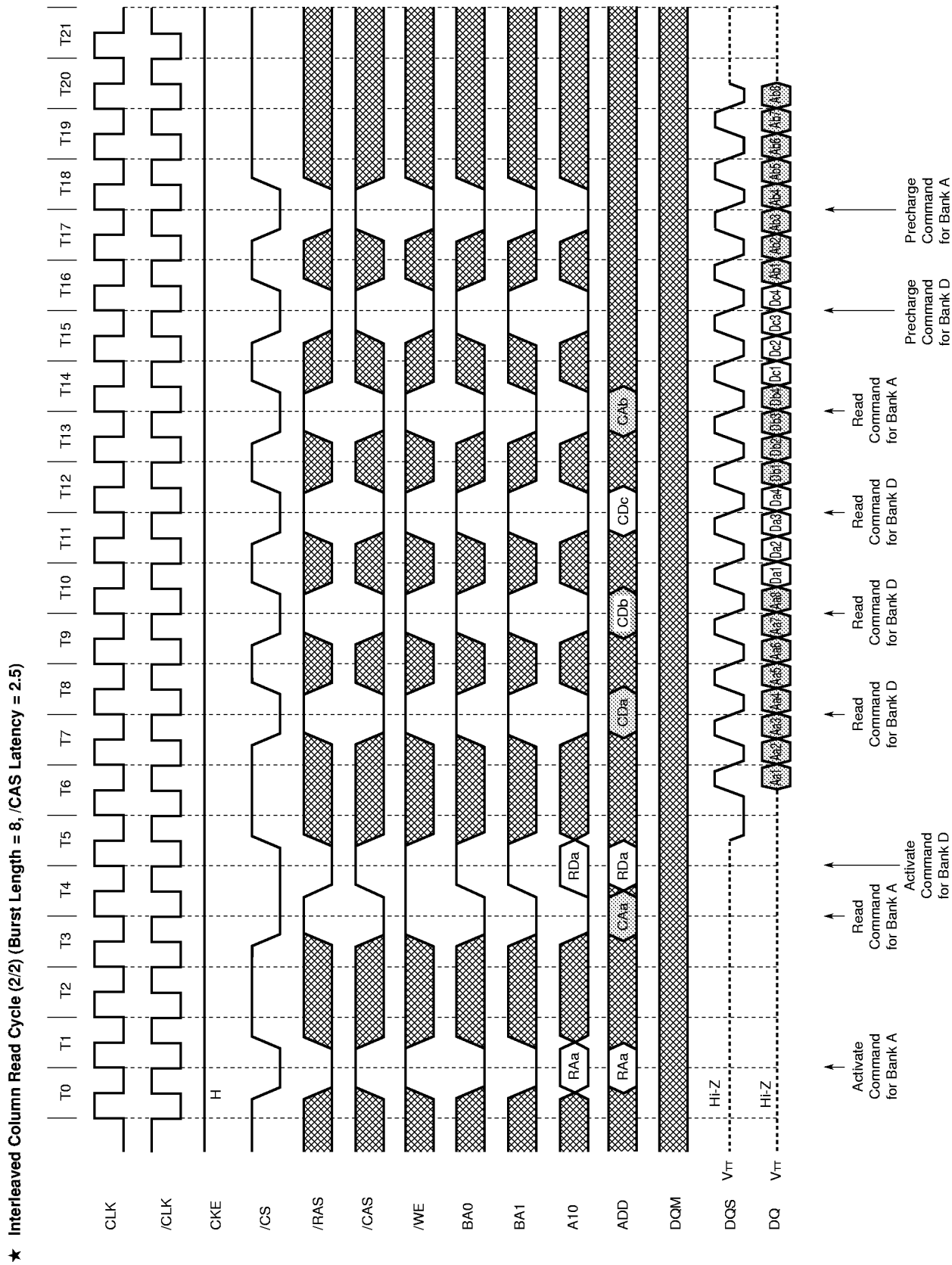
★ **Read and Write (2/2) (Burst Length = 8, /CAS Latency = 2.5)**



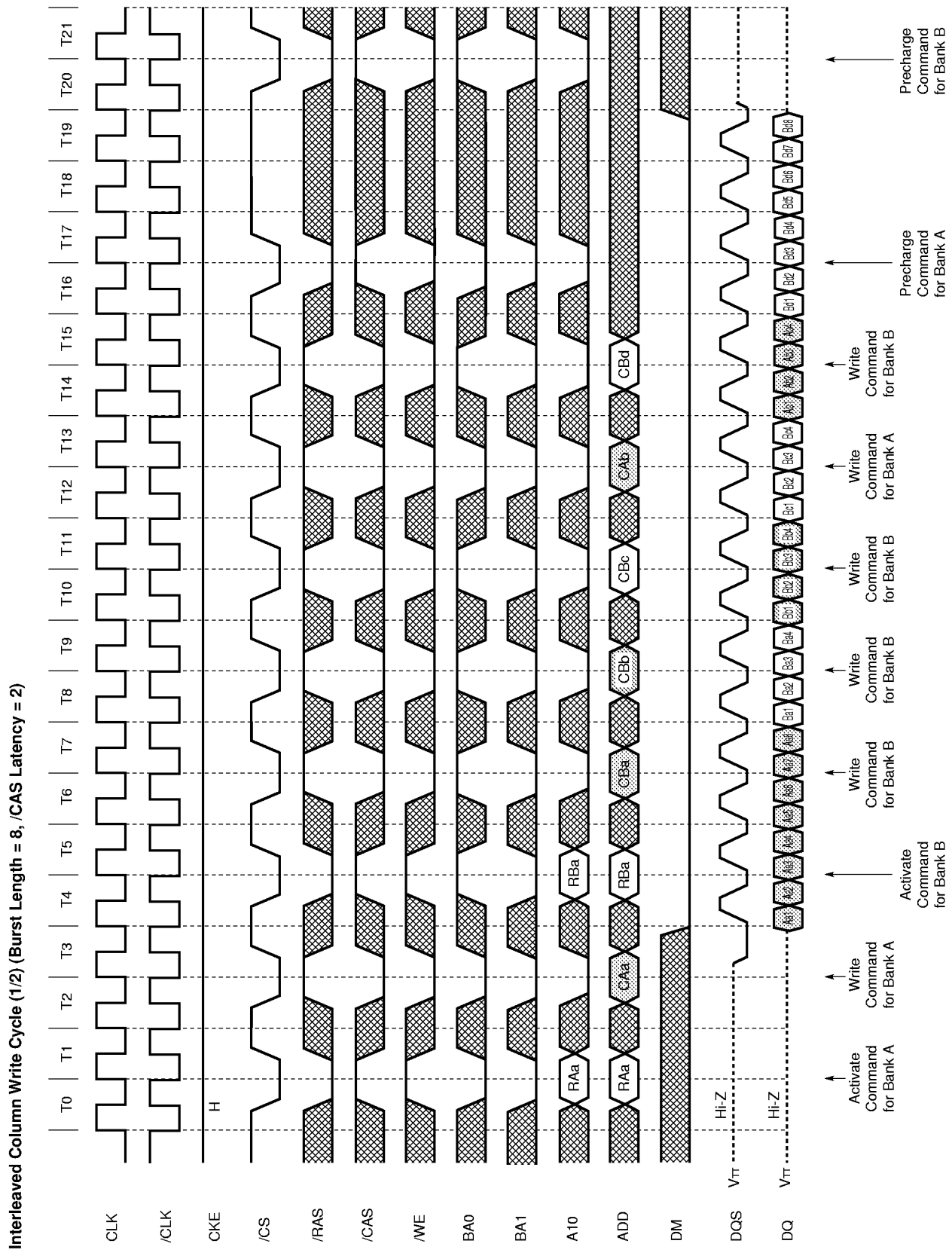
★ **Interleaved Column Read Cycle (1/2) (Burst Length = 8, /CAS Latency = 2)**



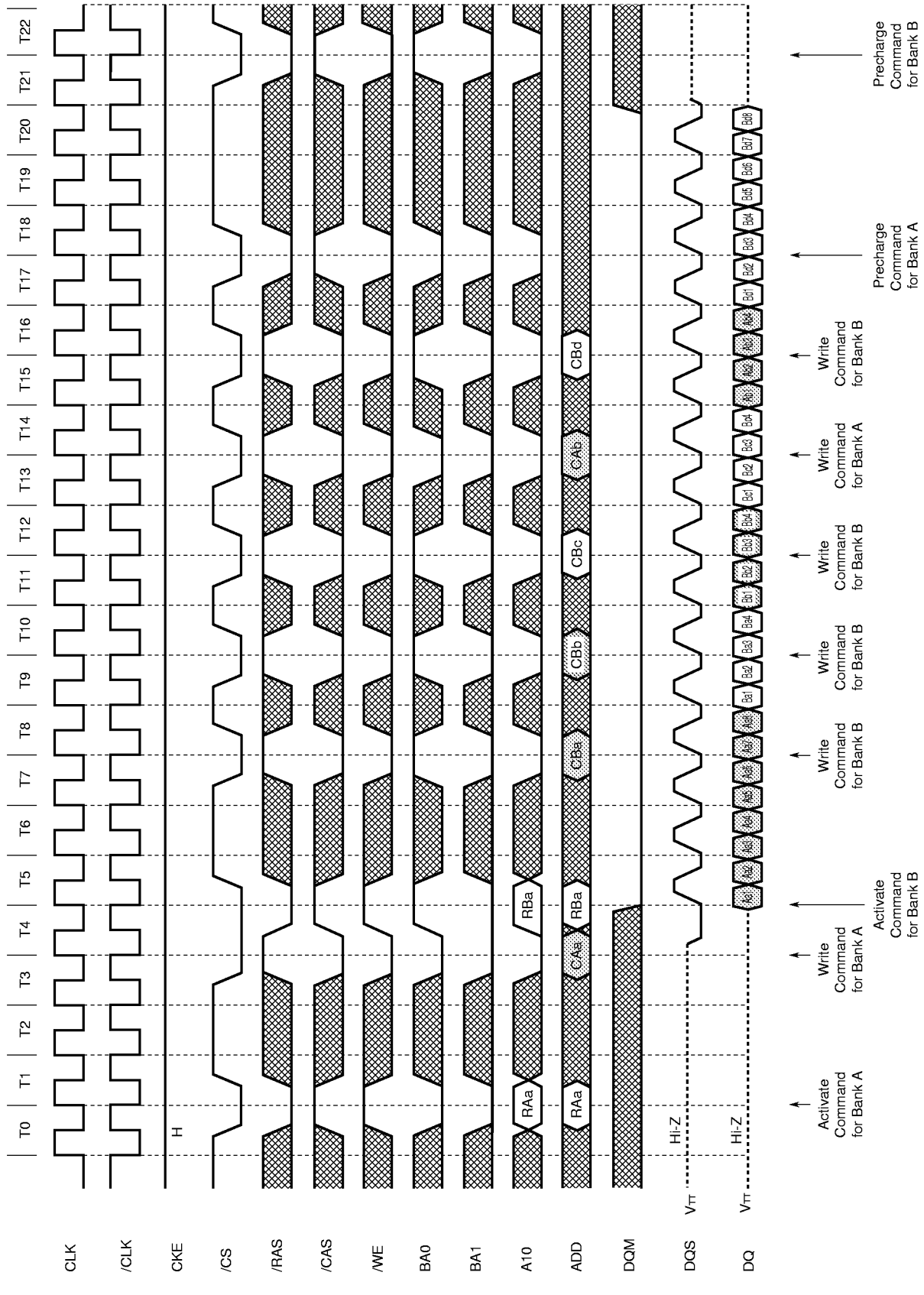
★ **Interleaved Column Read Cycle (2/2) (Burst Length = 8, /CAS Latency = 2.5)**



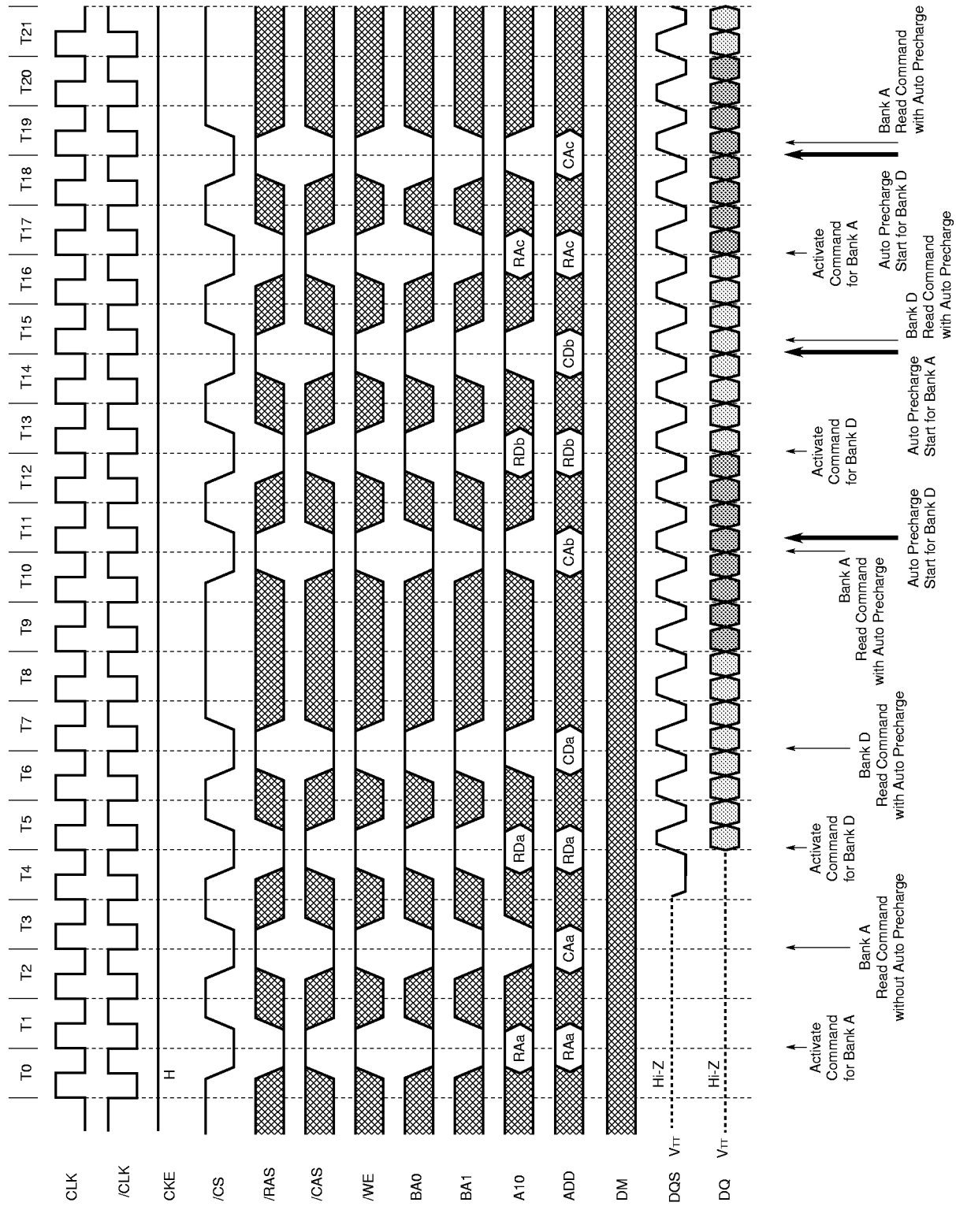
★ **Interleaved Column Write Cycle (1/2) (Burst Length = 8, /CAS Latency = 2)**



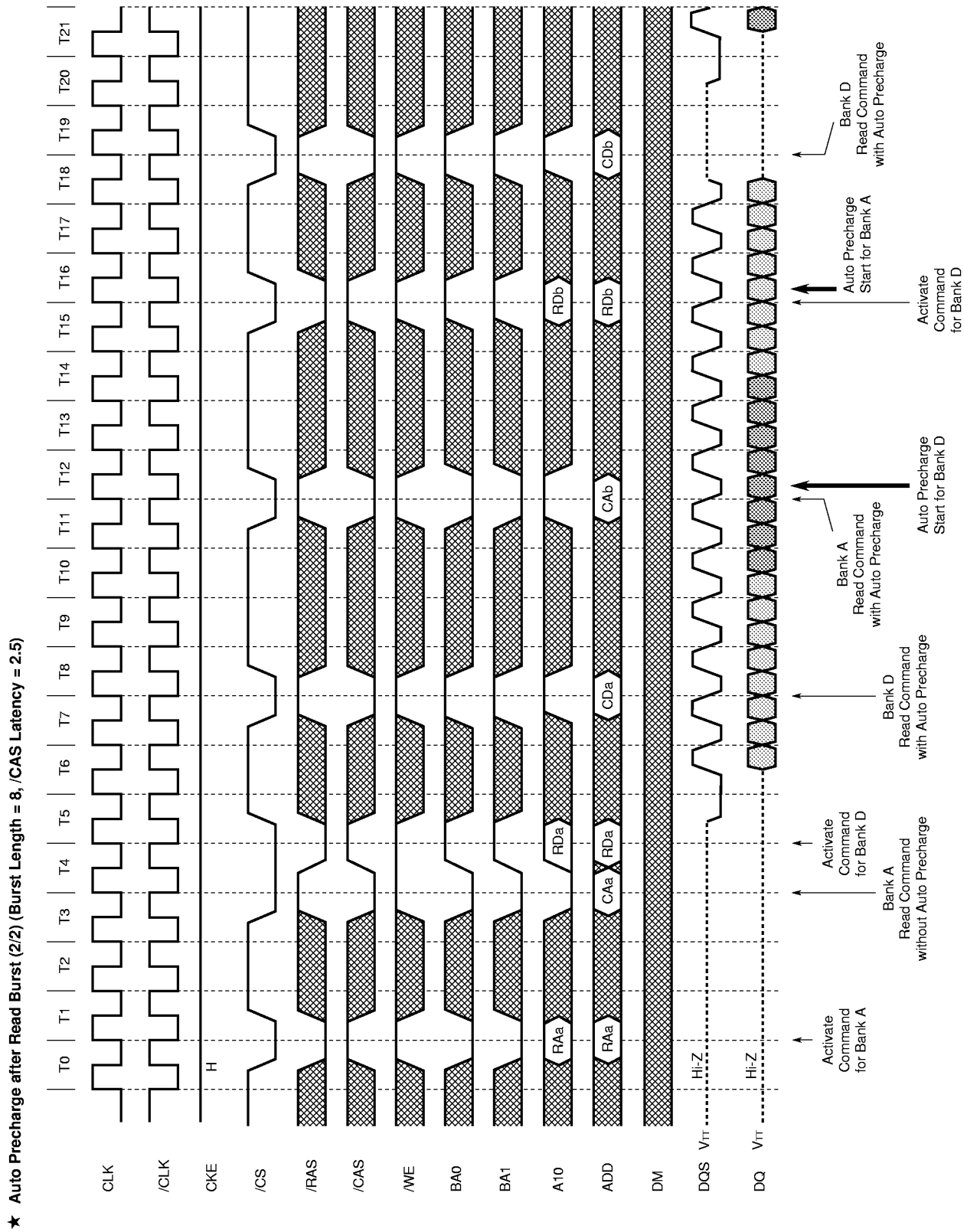
★ **Interleaved Column Write Cycle (2/2) (Burst Length = 8, /CAS Latency = 2.5)**



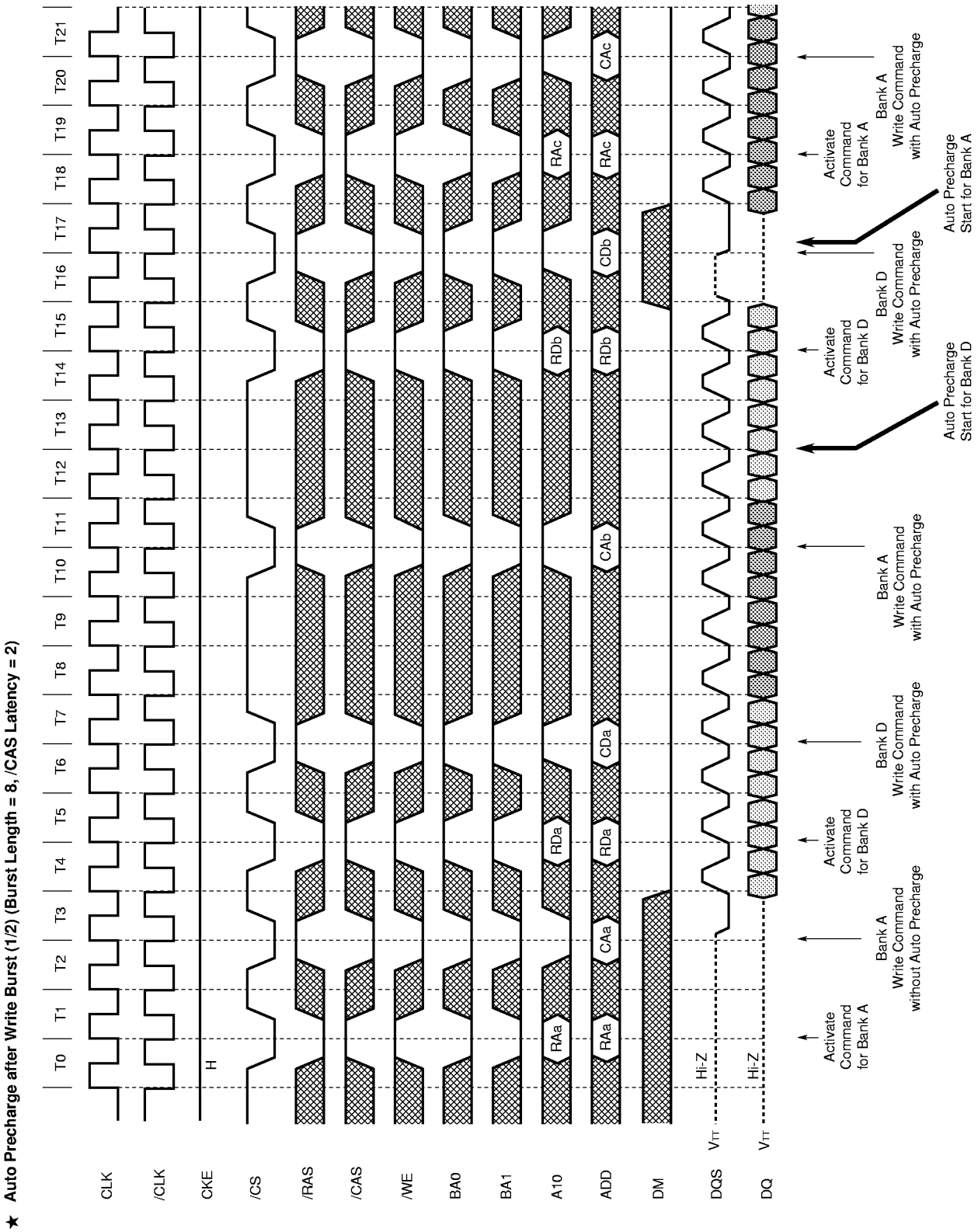
★ **Auto Precharge after Read Burst (1/2) (Burst Length = 8, /CAS Latency = 2)**



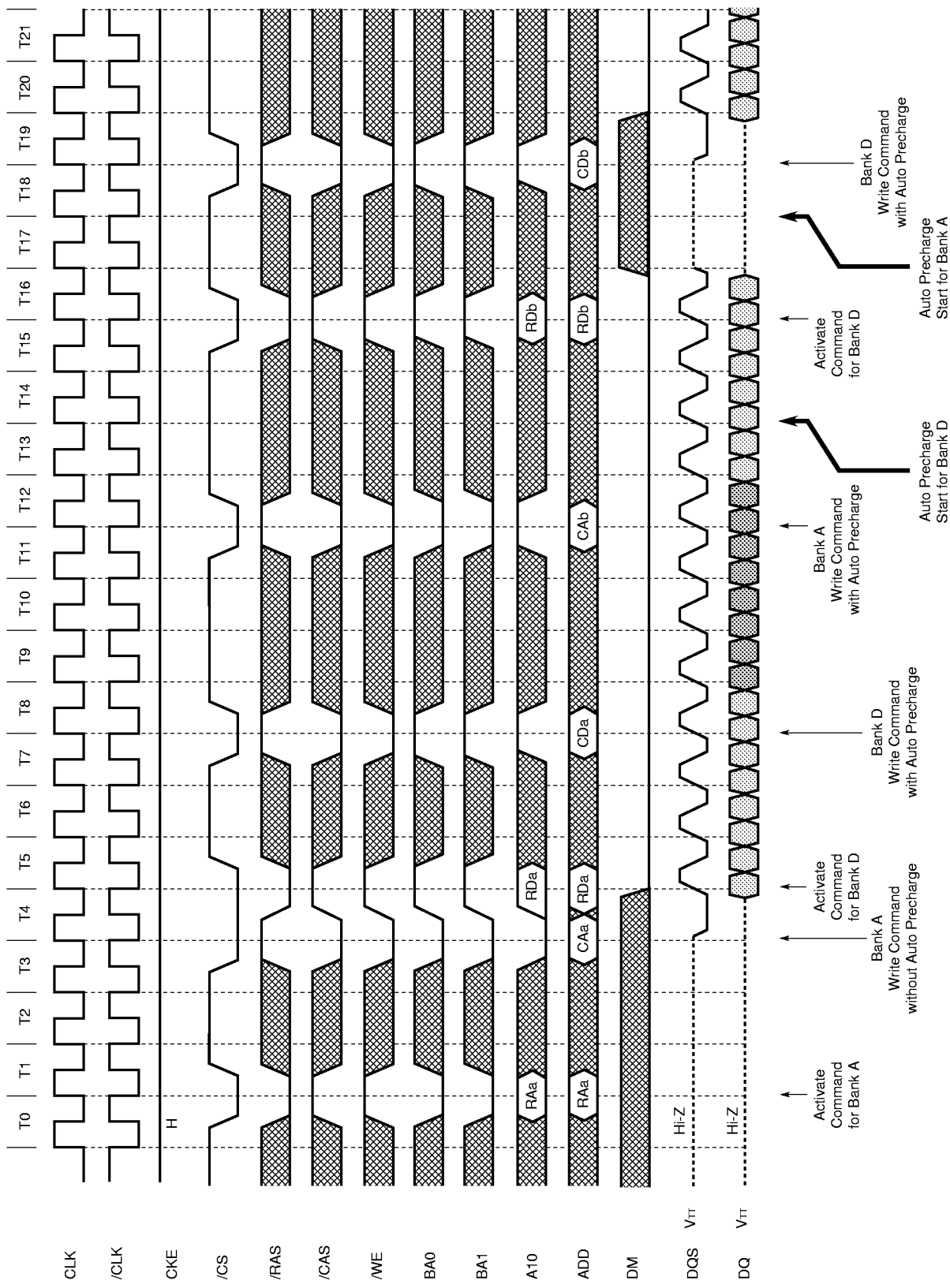
★ **Auto Precharge after Read Burst (2/2) (Burst Length = 8, /CAS Latency = 2.5)**



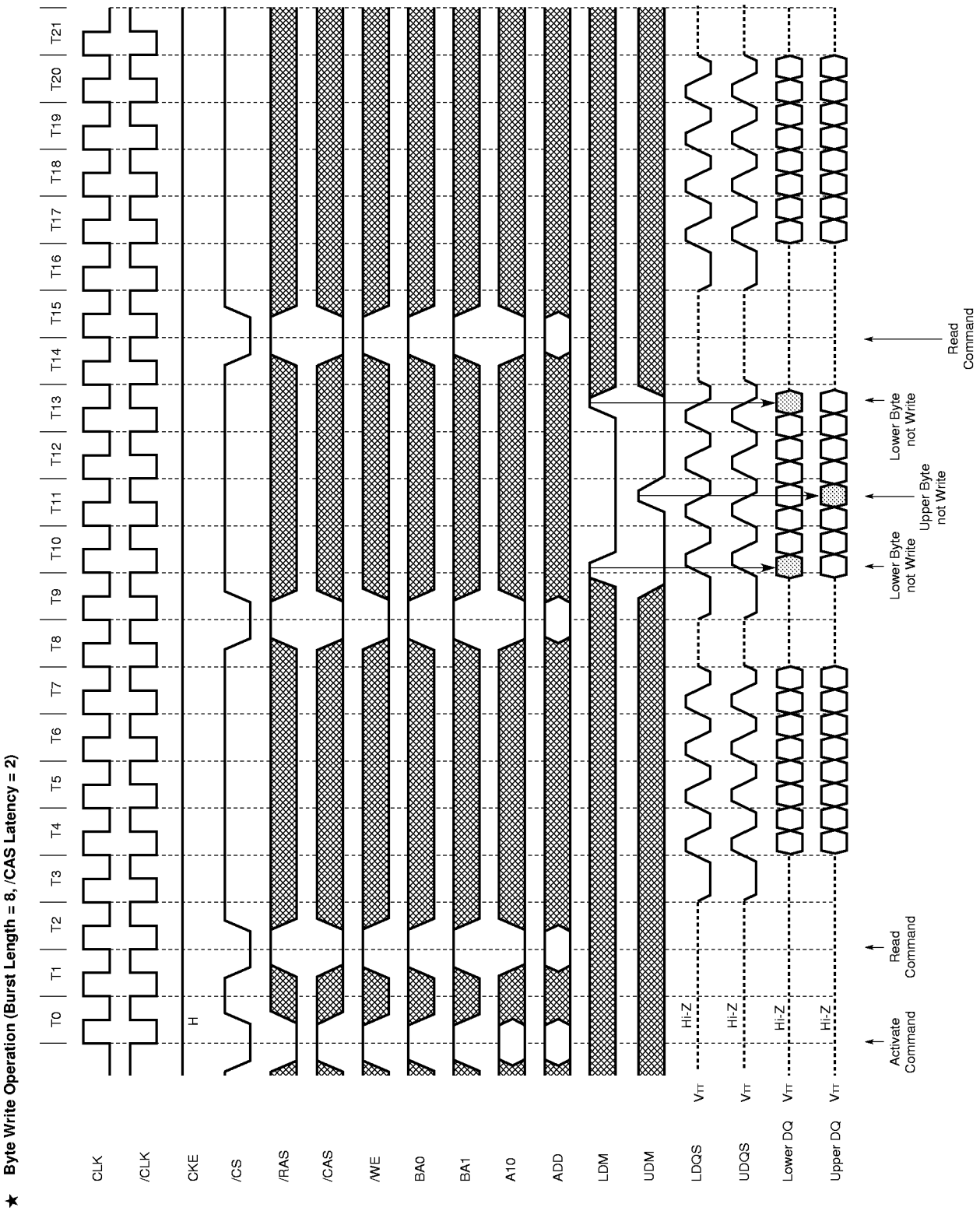
★ **Auto Precharge after Write Burst (1/2) (Burst Length = 8, /CAS Latency = 2)**



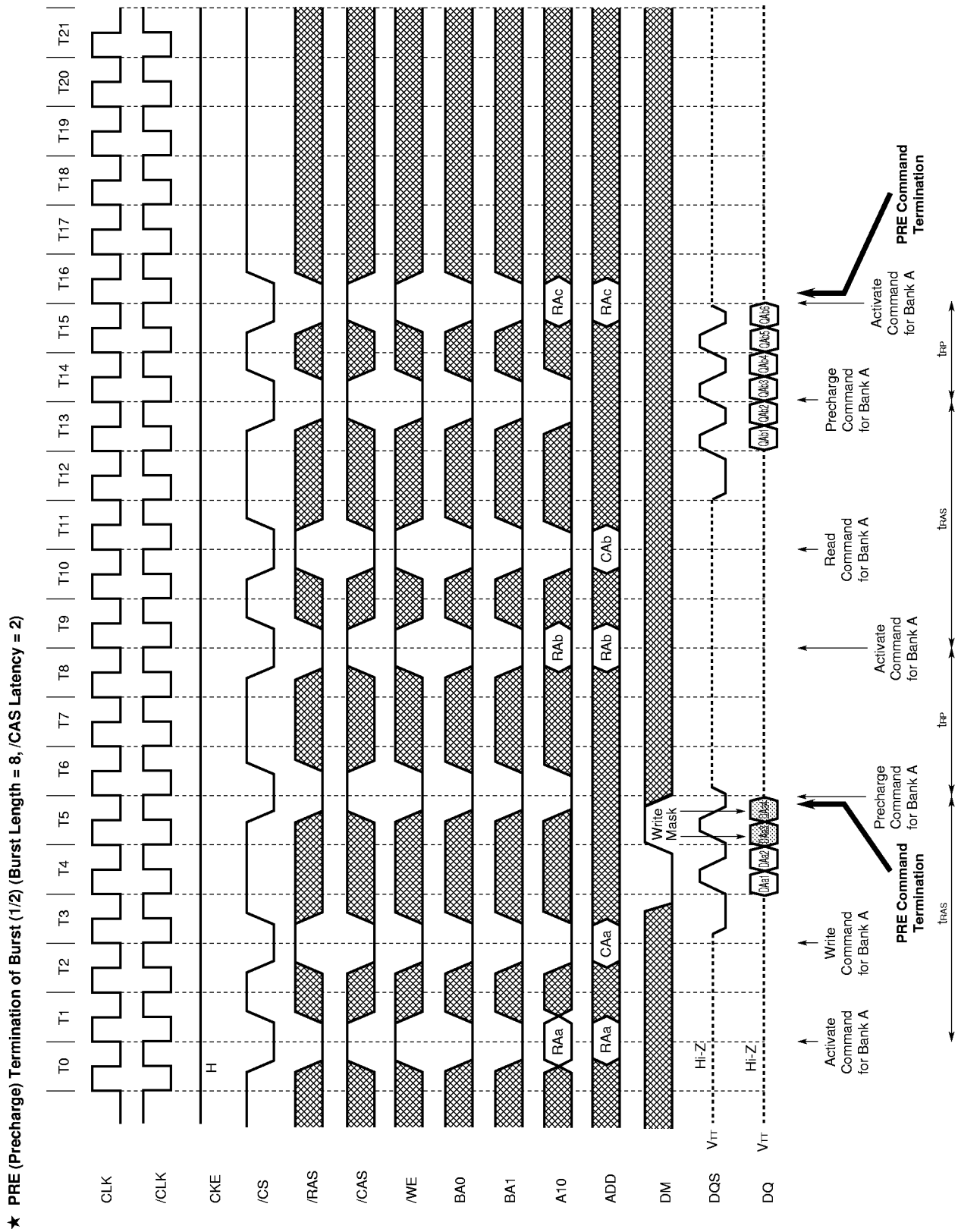
★ **Auto Precharge after Write Burst (2/2) (Burst Length = 8, /CAS Latency = 2.5)**



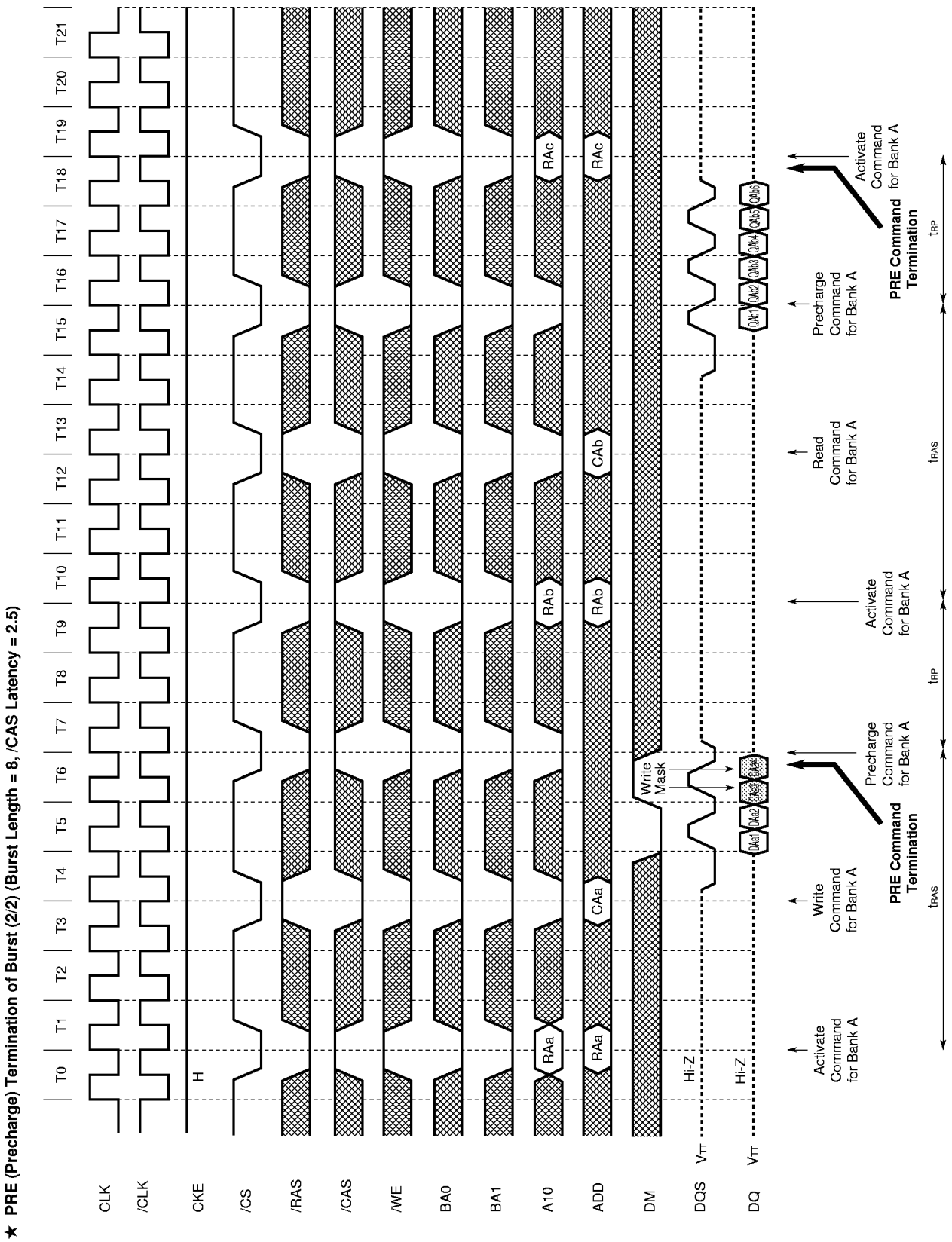
★ **Byte Write Operation (Burst Length = 8, /CAS Latency = 2)**



★ PRE (Precharge) Termination of Burst (1/2) (Burst Length = 8, /CAS Latency = 2)

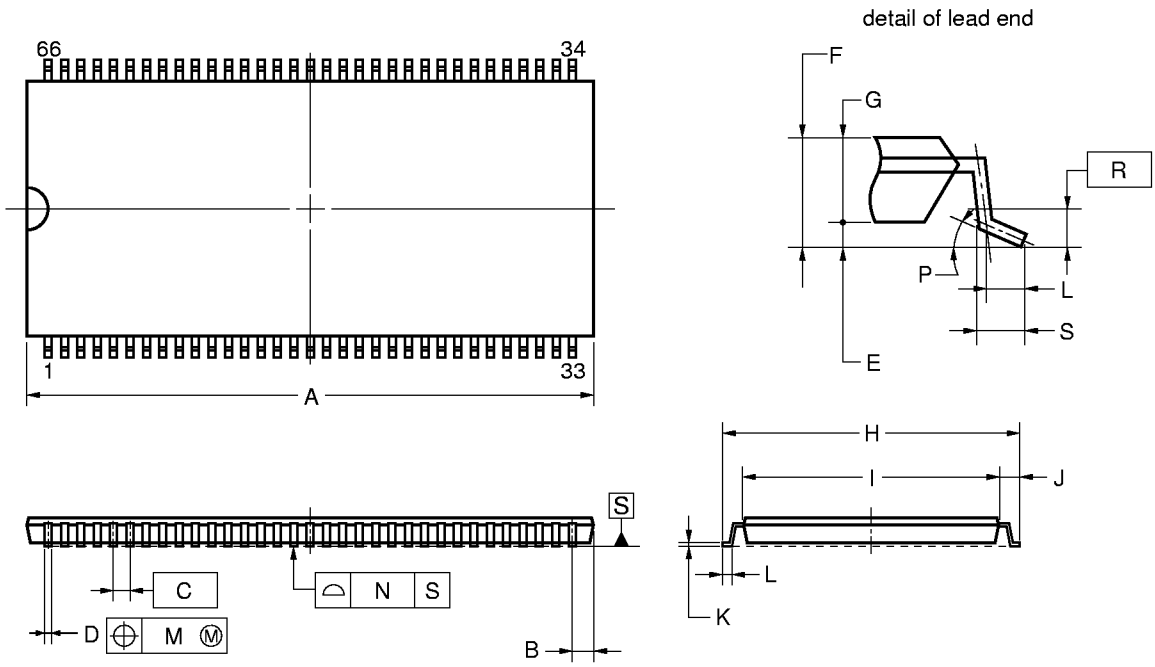


★ PRE (Precharge) Termination of Burst (2/2) (Burst Length = 8, /CAS Latency = 2.5)



14. Package Drawing

66PIN PLASTIC TSOP (II) (400mil)



NOTES

1. Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.
2. Dimension "A" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

ITEM	MILLIMETERS
A	22.22±0.05
B	0.865 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.10±0.05
F	1.1±0.1
G	1.00
H	11.76±0.20
I	10.16±0.10
J	0.80±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.50
M	0.12
N	0.10
P	$3°^{+5°}_{-3°}$
R	0.25
S	0.60±0.15

S66G5-65-9LG

15. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD45D128xxx.

Type of Surface Mount Device

μPD45D128xxxG5: 66-pin Plastic TSOP (II) (400 mil)

★ 16. Revision History

Edition / Date	Page		Description	
	This edition	Previous edition	Type of revision	Location
2nd edition / Jun. 1999	Throughout	Throughout	Modification	V_{CC} → V_{DD}, $V_{CC}Q$ → $V_{DD}Q$, I_{CC} → I_{DD}
	p.1	p.1	Modification	Power supply for V_{DD}, $V_{DD}Q$
	p.2	p.2	Modification	Ordering Information (Part Number, Clock frequency)
	p.3	p.3	Modification	Part Number (Minimum Cycle Time)
	p.10	p.10	Modification	Function (CLK, /CLK, CKE, BA0, BA1))
	p.11	p.11	Modification	Extended mode register set command, Mode register set command
	p.13	p.13	Modification	CBR (auto) refresh command
	p.15	p.15	Modification	3. Simplified State Diagram
	p.16	p.16	Modification	4.1 Command Truth Table (A0-7 → A0-9) 4.3 CKE Truth Table (SREX, PWDN, PWDN, PDEX)
	p.17	p.17	Modification	Row active(REF/SELF), Write(DESL, NOP, REF/SELF)
	p.18	p.18	Deletion	Row activating (SRS)
	p.19	p.19	Modification	Write recovering (DESL, NOP, BST), Refresh (DESL, NOP, BST), Mode register accessing (DESL, NOP)
	p.20	p.20	Modification	Self refresh (SREX), Power down (PDEX), All banks idle (Power down)
	p.21	p.21	Modification	5. Initialization
	p.22	p.22	Modification	Mode register fields
			Addition	Extended mode register fields
	p.23	p.23	Deletion	JEDEC standard test set
			Modification	Vender specific (A8)
	p.27, 29	p.27, 29	Modification	t_{DPL} → t_{WR}
	p.32	p.32	Modification	1 cycle → t_{WR}
	p.36	p.36	Modification	t_{DPL} → t_{WR}
	p.37	p.37	Modification	13.2 Recommended Operating Conditions (V_{DD}, $V_{DD}Q$, V_{REF})
			Addition	13.2 Recommended Operating Conditions ($V_{ID(DC)}$, V_{IX})
	p.38	p.38	Modification	13.4 DC Characteristics 1
			Deletion	13.5 DC Characteristics 2 (V_{OH}, V_{OL})
			Addition	13.5 DC Characteristics 2 (I_{OH}, I_{OL})
	p.39	p.39	Addition	13.6.1 Test Conditions ($V_{ID(ac)}$)
	p.40	p.40	Modification	13.6.2 Timing Diagram
	p.41	p.41	Modification	13.6.3 Synchronous Characteristics
	p.42	p.42	Modification	13.6.4 Synchronous Characteristics Example 13.6.5 Asynchronous Characteristics
	p.43, 44	p.43, 44	Modification	BA1 → BA0, BA0 → BA1, t_{DQSV} → t_{DV}
	p.45	p.45	Modification	Relationship between Frequency and Latency
	p.46-73	p.46-73	Modification	BA1 → BA0, BA0 → BA1
	p.46	p.46	Modification	t_{DQSS}, t_{DPL} → t_{WR}
	p.47	p.47	Modification	t_{RSC} → t_{MRD}
	p.48	p.48	Modification	Power On Sequence and CBR (auto) Refresh (Timing chart)
	p.51	p.51	Modification	t_{RC} → t_{RFC}
	p.52	p.52	Addition	t_{XSNR}
			Deletion	200 cycles
	p.54	p.54	Modification	DQS, DQ (T16-T19)
	p.57	p.57	Modification	DQS (T17-T21)
	p.61	p.61	Modification	Read Command for Bank A (T14-T15), DQS, DQ (T16-T21)
	p.62	p.62	Modification	Burst Length = 4 → Burst Length = 8
	p.66	p.66	Modification	Precharge Command for Bank B (T19-T22)
	p.71	p.71	Modification	Read Command (T13-T14)